DESCRIPTION

The PT16751 is a Headlight LED controller for automotive with high accuracy peak current mode. The device implements a fixed-frequency peak current mode control technique with programmable switching frequency, slope compensation, and soft-start timing. The controller is designed to support a range of step-up or step-down driver topologies. It incorporates a high voltage (65V) rail-to-rail current sense amplifier that can directly measure LED current using a high-side series sense resistor. The amplifier is designed to achieve low input offset voltage and attain better than ±4% LED current accuracy over junction temperature range of 25°C to 140°C and output common-mode voltage range of 3V to 60V.

This LED controller can independently modulate LED current using either analog or PWM dimming techniques. Linear analog dimming response with 15:1 range is obtained by varying the voltage from 140 mV to 2.25 V across the high impedance analog adjust (IADJ) input. PWM dimming of LED current is achieved by modulating the PWM/DIM input pin with the desired duty cycle or by enabling the internal PWM generator circuit. The DC input voltage at PWM/DIM pin is translated by the PWM generator, to corresponding duty cycle by comparing it to the internal triangle wave generator. PDRV gate driver output can be used to enable series FET dimming functionality to get over 1000:1 contrast ratio.

The PT16751 provides perfect protection to prevent LED lights overheating and damage. Connect IADJ2 pin to a voltage divider circuit which includes NTC thermistor to obtain the temperature of LED board. TEMPA set the derating curve of LED current when LED lights is overheat, and TEMPB set the thermal shutdown temperature.

The PT16751 supports continuous LED status check through the current monitor (IMON/FLT) output. IMON/FLT pin outputs 5.07V (typical) to indicate device overheat (typical at 175°C), LED over-current, over-voltage and under-voltage conditions.

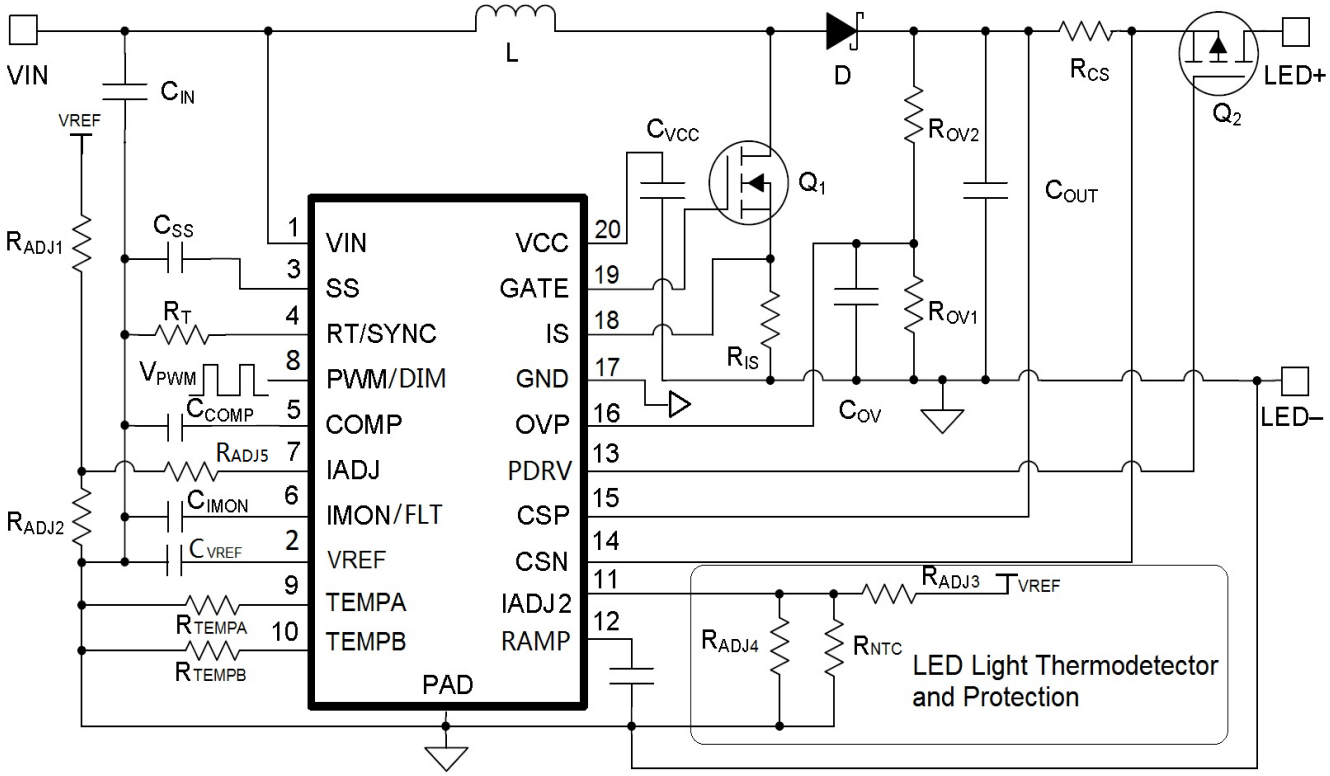
FEATURES

- Automotive AEC-Q100, Grade 1 (-40℃~+125℃) Qualified.
- Input Voltage: 4.5 V to 65 V
- Output Voltage Range: 3 V to 65 V
- Low Input Offset Rail-to-Rail Current Sense Amplifier
  – Better than ±4% LED Current Accuracy over 25°C to 140°C Junction Temperature Range
  – High-Side Current Sense Implementations
- High-Impedance Analog LED Current Adjust Input (IADJ) With over 15:1 Contrast Ratio
- Additional Analog LED Current Dimming 2 (IADJ2) for LED Lights overheat Protection with NTC Thermistor
- Over 1000:1 Series FET PWM Dimming Ratio
- Support P-Channel MOSFET drive for LED PWM dimming and LED short protection.
- Continuous LED Current Monitor Output for System Fault Detection
- Programmable Switching Frequency With External Clock Synchronization Capability
- Programmable Soft-Start
- Comprehensive Fault Protection Circuitry Including VCC Undervoltage Lockout (UVLO), Output Overvoltage Protection (OVP), Output Undervoltage Protection (UVP), Cycle-by-Cycle Switch Current Limit, Output over current protection and Thermal Protection.

APPLICATIONS

- Automotive Headlight Application
- LED General Lighting Applications
- Exit Signs and Emergency Lighting

TYPICAL APPLICATION



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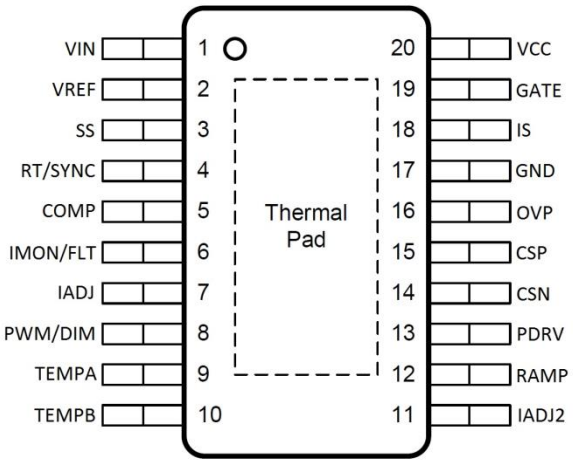
1. ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT16751-HT	20 Pins, HTSSOP	PT16751-HT

2. PIN CONFIGURATION

PT16751---HTSSOP20



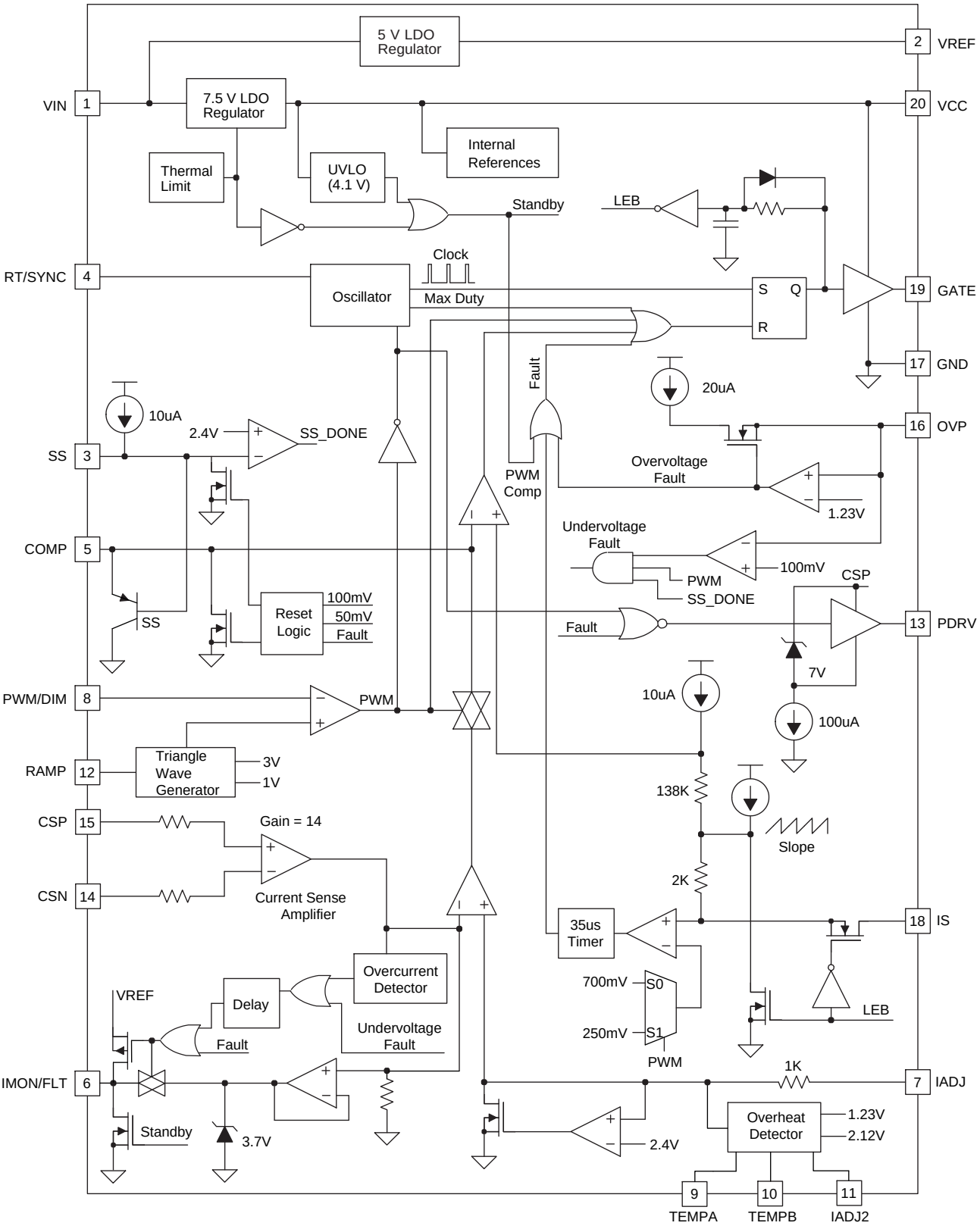
3. PIN DESCRIPTION

PIN Name	I/O	Description	PIN NO.
VIN	--	Supply voltage input. Place a 100nF capacitor close to the controller.	1
VREF	--	Support 5.07V reference voltage. Locally decouple to GND using a ceramic capacitor (with a value between 2.2-μF and 4.7-μF) located close to the controller.	2
SS	I/O	Programmable soft-start pin. Connect a capacitor to GND to set the start-up time. Short this pin to GND to disable the Gate pin work.	3
RT/SYNC	I/O	Programmable oscillator frequency pin. Connect a resistor to GND to set the switching frequency. Connect a 100nF capacitor series to this pin to synchronize the internal oscillator from an external clock pulse.	4
COMP	I/O	Error amplifier compensation. Connect compensation network to achieve desired closed loop response.	5
IMON/FLT	O	LED current report and fault indicator pin. The LED current sensed by CSP/CSN input is reported as $V_{IMON/FLT} = 14 \times I_{LED} \times R_{CS}$. Active fault signal output as VREF voltage (typical 5.07V). Bypass with a 1-nF ceramic capacitor to GND.	6
IADJ	I	Reference voltage input for LED current. To implement analog dimming, source a external voltage from 0V to 2.25V to this pin, and the current sense voltage: $V_{(CSP-CSN)} = V_{IADJ}/14$. Connecting IADJ to VCC with 100kΩ series resistor, the reference voltage would be clamped to 2.42 V and the current sense threshold, $V_{(CSP-CSN)}$ = 172 mV.	7

PIN DESCRIPTION (continued)

PIN Name	I/O	Description	PIN NO.
PWM/DIM	I	PWM dimming input. Supports analog or direct PWM signal input. The analog dimming signal (1~3V) is compared to the internal PWM generator triangle waveform to set LED current duty cycle between 0% and 100%. A direct PWM dimming signal can be applied to control the LED current duty cycle and frequency when the PWM generator disabled. The analog or PWM command is used to generate an internal PWM signal that controls the GATE and PDRV outputs. Setting the internal PWM signal to logic level low, turns off switching, idles the oscillator, disconnects the COMP pin, and sets PDRV to VCSP. Connect to VREF when not used for PWM dimming.	8
TEMPA	I	LED Current setting, programming pin. Connect a resistor to GND to set the IADJ voltage. This voltage set the constant current (X%) after derating.	9
TEMPB	I	LED Current shut down setting, programming pin. Connect a resistor to GND to set the shutdown threshold. LED Current drops to Zero when the IADJ2 voltage decreases to the set voltage.	10
IADJ2	I	LED lights overheat protection pin. Connect IADJ2 pin to a voltage divider circuit which includes NTC thermistor to obtain the temperature of LED board. The LED current will decrease linearly when IADJ2 input voltage decrease from 2.17V.	11
RAMP	I/O	Programming input for internal PWM generator. Connect a capacitor to GND to set the triangle wave frequency for PWM generator circuit. Connect a 250-kΩ resistor to GND to disable the PWM generator and to set a fixed reference for direct external PWM dimming input. Do not allow this pin to float.	12
PDRV	O	Series dimming P-channel FET gate driver output. Connect to gate of external P-channel MOSFET to implement series FET PWM dimming and LED short protection.	13
CSN	I	Current sense amplifier negative input (–). Connect directly to the negative node of LED current sense resistor R_{CS}.	14
CSP	I	Current sense amplifier positive input (+). Connect directly to the positive node of LED current sense resistor RCS.	15
OVP	I	Overvoltage protection pin. Connect resistor divider from output to set overvoltage protection threshold and hysteresis.	16
GND	--	Analog and Power ground connection pin. Connect to circuit ground to complete return path.	17
IS	I	Switching current sense pin. Connected to switching current sense resistor, R_{IS}, to monitor the peak current of the main MOSFET.	18
GATE	O	Gate driver output for switching MOSFET. Connect to gate of the main MOSFET.	19
VCC	--	VCC bias supply pin. Using a 2.2μF to 4.7μF ceramic capacitor located close to the controller.	20
Thermal PAD	--	The GND pin must be connected to the exposed thermal pad for proper operation. This PAD must be connected to PCB ground plane using multiple vias for good thermal performance.	Thermal PAD

4. FUNCTIONAL BLOCK DIAGRAM



5. FUNCTION DESCRIPTION

5.1 OVERVIEW

The PT16751 is a wide input range (4.5 V to 65 V) LED driver controller. It has all of the functions necessary to implement a compact and highly efficient LED driver, supports step-up or step-down converter topologies. It incorporates a low input offset, rail-to-rail current sense amplifier that supports a wide range of output voltages (3 V to 65 V) and is capable of powering the LED string consisting of 1 to more than 20 LEDs.

The device works at fixed-frequency, peak current mode control, provides high-side current shunt sensing technique to achieve a constant current output, and drive a single string of series-connected LEDs. The LED current sense threshold, set by the analog adjust input, IADJ, provides the capability to analog (amplitude) dim over a linear range of 15:1 by varying the voltage, V_{IADJ}, from 140 mV to 2.25 V. The IADJ input provides the means to externally program LED current and facilitates calibration, brightness correction of the LEDs.

The PT16751 provides perfect protection to prevent LED lights overheating and damage. User customize OTP point and the derating curve of LED current with a few components.

High resolution and linear dimming response is achieved by varying the duty cycle of LED current based on the PWM input. The PWM input directly controls the GATE and PDRV drive outputs, controls the internal oscillator, and enables high-speed PWM dimming with over 1000:1 contrast ratio when using an external MOSFET placed in series with the LED load.

The current monitor output, IMON/FLT, reports the instantaneous status of LED current measured by the rail-to-rail current sense amplifier. This feature is incorporated to indicate LED short and open circuit failures and enables cable harness fault detection independent of LED driver topology. Other fault protection features include cycle-by-cycle current limiting, hysteresis-based overvoltage protection, Output under voltage, Output over current limiting, VCC under voltage protection, thermal shutdown, and remote shutdown capability by pulling down the SS pin.

5.2 VREF AND VCC SUPPLY

The PT16751 incorporates a high voltage regulator (65V), generates 5.07V reference voltage, 7.5 V VCC bias supply, and other internal reference voltages. The VREF voltage is internally used to generate voltage thresholds for the RAMP generator circuit and to power some digital circuits. The VREF voltage can be used to set voltage levels for either the IADJ pin or PWM/ DIM pin to set LED current or PWM dimming duty cycle. Also can be used to bias external circuitry requiring a reference supply. Place a bypass capacitor in the range of 2.2μF to 4.7μF across the VREF output to GND to ensure proper operation.

The VCC pin is monitored to implement UVLO protection. The controller is enabled when the VCC voltage exceeds 4.2V threshold and is disabled when the voltage drops below 4V threshold. The UVLO comparator provides 0.2V hysteresis to avoid chatter during transitions. The UVLO thresholds are fixed internally and cannot be adjusted. The VCC supply powers the internal circuitry, GATE driver and PDRV driver. Place a bypass capacitor in the range of 2.2μF to 4.7μF across the VCC output and GND to ensure proper operation. The regulator operates in dropout when input voltage VIN falls below 7.5 V forcing VCC to be lower than VIN by 300 mV for a 20-mA supply current. The VCC is a regulated output of the internal regulator and cannot be driven from an external power supply.

5.3 OSCILLATOR

The switching frequency of PT16751 can be programmed by a single external resistor connected between the RT/SYNC pin and the GND pin. To set a desired frequency, f_{SW} (Hz), the resistor value can be calculated using:

$$R_T = \frac{1.432 \times 10^{10}}{(f_{sw})^{1.047}} \ (\Omega) \qquad (1)$$

Figure 1 shows a graph of switching frequency versus resistance R_T. It recommends a switching frequency setting between 80 kHz and 700 kHz for optimal performance over input and output voltage operating range and for best efficiency. Operation at higher switching frequencies requires careful selection of N-channel MOSFET characteristics as well as detailed analysis of switching losses.

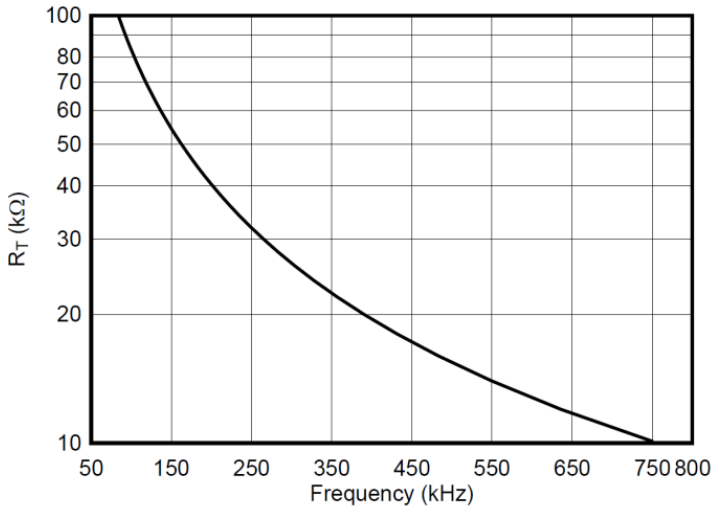


Figure 1. Timing Resistance (R_T) VS Switching Frequency

The internal oscillator can be synchronized by AC-coupled external clock pulse to RT/SYNC pin, shown as in **Figure 2.** The positive going synchronization clock at the RT/SYNC pin must exceed the RT/SYNC threshold, and the negative going synchronization clock at the RT pin must exceed the RT/SYNC falling threshold so that the internal synchronization pulse detector can be tripped.

It recommends that the frequency of the external synchronization pulse is within ±20% of the internal oscillator frequency programmed by the R_T resistor. A minimum coupling capacitor of 100 nF and typical pulse width of 100 ns for proper synchronization are recommended. In the case where external synchronization clock is lost the internal oscillator takes control of the switching rate based on the R_T resistor to maintain output current regulation. The R_T resistor is always required whether the oscillator is free running or externally synchronized.

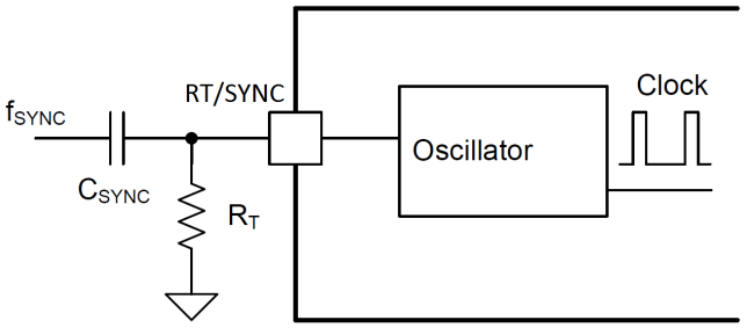


Figure 2. Oscillator Synchronization through AC Coupling

5.4 SOFT-START

The PT16751 has soft-start function to help the regulator reach the steady-state operating point gradually, thus reducing startup stresses and surges. The COMP pin is clamped to the SS pin, separated by a diode, until LED current nears the regulation threshold. The voltage of SS pin increase gradually due to the internal 10-μA soft-start current source on an external soft-start capacitor C_{SS}. This results in a gradual rise of the COMP voltage from GND.
When VCC exceeds the UVLO threshold, the internal 10-μA current source turns on. At the beginning of the soft-start sequence, the SS pull down switch is active and is released when the voltage V_{SS} drops below 25 mV. The SS pin can also be pulled down by an external switch to stop switching. When the SS pin is externally driven to enable switching, the slew-rate on the COMP pin should be controlled by choosing a compensation capacitor that avoids large startup transients. The value of C_{SS} should be large enough to charge the output capacitor during the soft-start transition period.

5.5 TRANSCONDUCTANCE ERROR AMPLIFIER

The internal transconductance amplifier generates an error signal proportional to the difference between the LED current sense feedback voltage and the external IADJ input voltage. Closed-loop regulation is achieved by connecting a compensation network to the output of the error amplifier. In most LED driver applications, a simple integral compensator consists of a capacitor across the COMP output and ground, to obtain a stable response. It recommends a capacitor value between 10 nF and 100 nF as a good starting point. Higher closed-loop bandwidth can be achieved by implementing a proportional-integral compensator consisting of a series resistor and a capacitor network connected across the COMP output and ground. Based on the converter topology, the compensation network should be tuned to achieve a minimum of 60° of phase margin and 10 dB of gain margin.

5.6 CURRENT MONITOR OUTPUT

The IMON/FLT pin voltage represents the LED current measured by the rail-to-rail current sense amplifier across the external current shunt resistor. The linear relationship between the IMON/FLT voltage and LED current includes the amplifier gain-factor of 14 (see **Figure 3**). The IMON/FLT output can be connected to an external microcontroller or comparator to facilitate LED open, short, or cable harness fault detection and mitigation based on programmable threshold V_{OCTH}. The IMON/FLT voltage is internally clamped to 3.7 V.

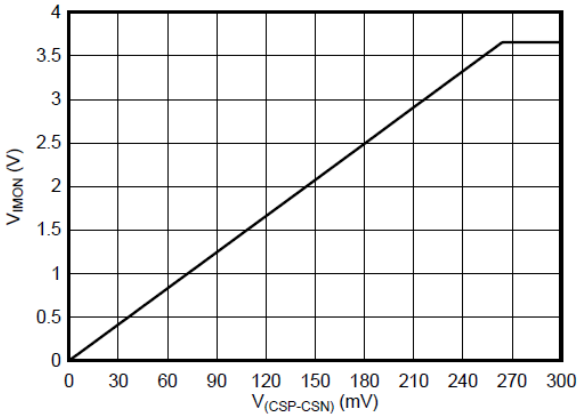


Figure 3. $V_{IMON/FLT}$ vs $V_{(CSP-CSN)}$

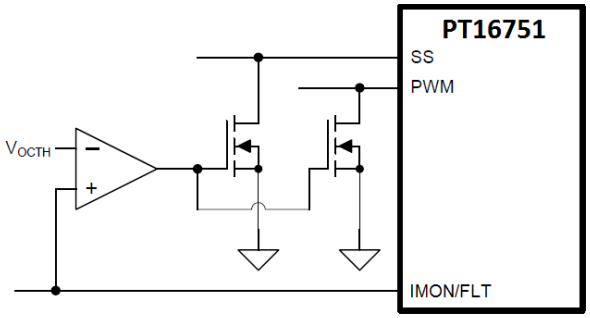


Figure 4. LED Overcurrent Protection using IMON/FLT Output

The IMON/FLT pin also can indicate the fault conditions. It outputs a voltage signal (=VREF) to indicate fault mode under the following conditions:

- Overvoltage across the LED string (V_{OV}> 1.23 V)
- Undervoltage across the LED string (V_{OV}< 100 mV)
- Overcurrent across the LED string (14 × $V_{(CSP-CSN)}$ > 1.5 × V_{IADJ})
- Cycle-by-cycle switch current limit condition (V_{IS} > 250 mV)

5.7 ANALOG ADJUST INPUT

The voltage of LED current sense resistor V_{CSP}–V_{CSN}, is regulated to the analog adjust input voltage V_{IADJ}, scaled by the current sense amplifier voltage gain of 14. Using a resistor divider from VREF or a voltage source, the LED current can be linearly adjusted by varying the voltage on IADJ pin from 140 mV to 2.25 V. The IADJ pin can be connected to VREF through an external resistor to set LED current based on the 2.4V internal reference voltage. This device offers different methods to set the IADJ voltage. **Figure 6** shows how the IADJ input can be used in conjunction with a NTC resistor to achieve the thermal protection. A PWM signal in conjunction with first- or second-order low-pass filter can be used to program the IADJ voltage as shown in **Figure 7**.

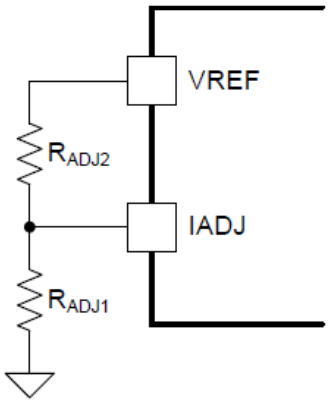


Figure 5. Static Reference Setting Resistor Divider From VREF

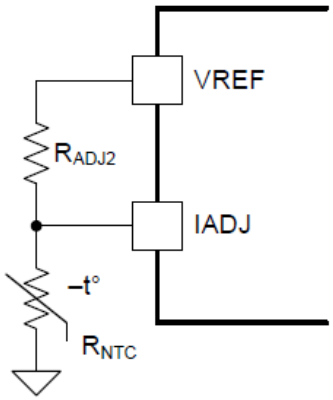


Figure 6. Thermal Fold-back Circuit Using External NTC Resistor

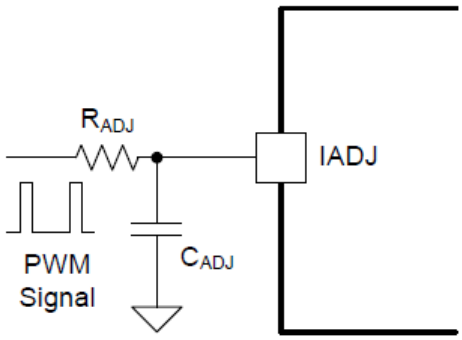


Figure 7. Analog Dimming Achieved By Low-pass Filtering External PWM Signal

5.8 PWM/DIM INPUT

The PT16751 device incorporates a PWM generator circuit to translate analog voltage to PWM duty cycle. Connecting a capacitor from RAMP pin to GND to set the dimming frequency. The dimming frequency, f_{DIM}, can be calculated as **Equation 2**:

$$f_{DIM} = \frac{10uA}{2 \text{ x } 2V \text{ x } C_{DIm}} \text{ (Hz)} \quad (2)$$

The internal PWM signal can be varied from 0% to 100% by setting the PWM/DIM pin voltage between 1V and 3V. The following equation describes the relationship between PWM/DIM pin voltage, V_{DIM} and internal PWM duty cycle, D_{PWM}.

$$D_{PWM} = \frac{V_{DIM}-1}{2}$$

To improve dimming accuracy, use the VREF pin and a resistor divider to set the PWM/DIM pin voltage, V_{DIM}, and the corresponding duty cycle, D_{PWM}. The device can be configured to step the duty cycle between 100% and the programmed value by diode connecting the external control signal, V_{CTRL}, to the PWM/DIM pin, as shown in following Figure 8. The external control signal, of amplitude 3V, is usually generated by the command module and is based on the light output required by the application.

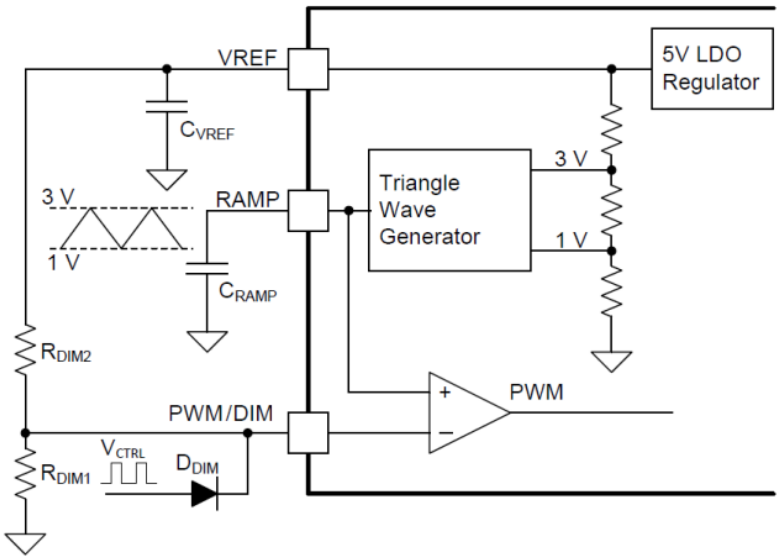


Figure 8. PWM Dimming Using Internal PWM Generator

Shown as Figure 9, the LED current also can be modulated by the external PWM input, because the device can be configured to be compatible with external PWM signal, $V_{PWM(EXT)}$. When use the external PWM signal directly, it is need to connect a 250 kΩ resistor from RAMP pin to GND to disable the internal triangle wave generator. In this case, the internal comparator threshold is set to 2.5 V and the internal PWM duty cycle, D_{PWM}, is controlled by the external PWM command. The RAMP pin cannot be left floating.

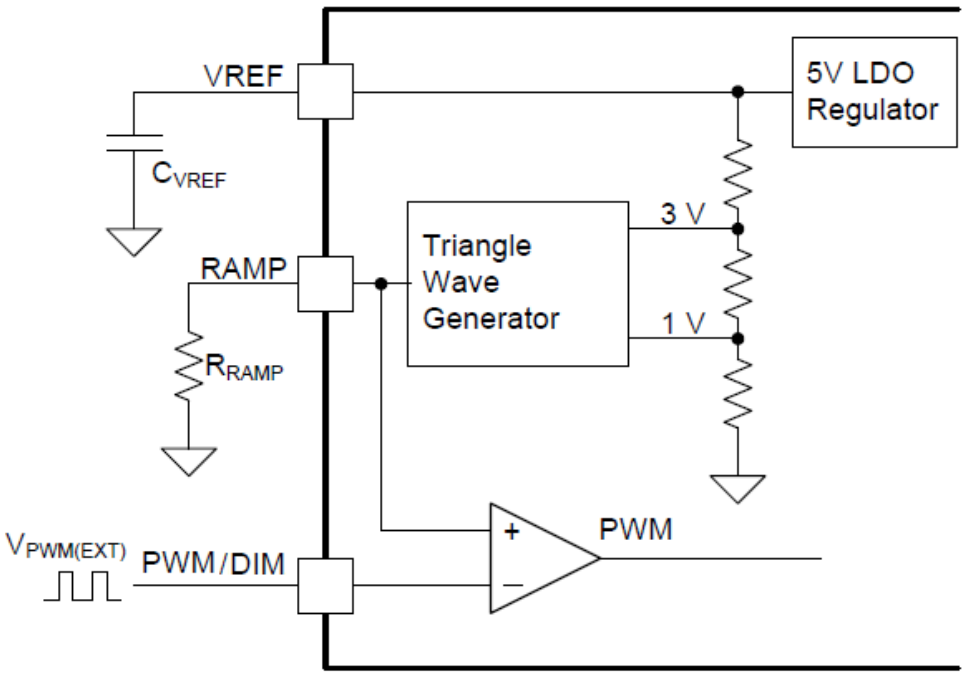


Figure 9. Direct PWM Dimming

The GATE and PDRV output are controlled by the internal PWM signal. Forcing the internal PWM signal in a logic low state turns off switching, parks the oscillator, disconnects the COMP pin, and sets the PDRV output to V_{CSP} in order to maintain the charge on the compensation network and output capacitors. On the rising edge of the PWM voltage (V_{PWM} set to logic level high), the GATE and PDRV outputs are enabled to ramp the inductor current to the previous steady-state value. The COMP pin is connected and the error amplifier and oscillator are enabled only when the switch current sense voltage V_{IS} exceeds the COMP voltage, thus immediately forcing the converter into steady-state operation with minimum LED current overshoot. Connects the PWM/ DIM pin to the VCC pin or VREF pin when dimming function is not required. An internal pull-down resistor sets the input to logic-low and disables the device when the pin is disconnected or left floating.

5.9 LED LIGHT OVERHEAT PROTECTION

The PT16751 provides advanced over temperature protection. Customized the current derating curve and the shut down point by setting R_{TEMPA} and R_{TEMPB}. A typical application is shown as Figure 10, generally, a NTC thermistor is placed on LED board to detect the temperature of the LED board. The value of NTC thermistor decreases when the temperature of LED board rises, and the voltage of IADJ2(V_{IADJ2}) also decreases. As shown in Figure 11, when the V_{IADJ2} drops to 2.17V, LED current begins to decrease, to reduce LED board heating. However, if the temperature of the LED board continues rising, the value of NTC thermistor continues decreasing, and accordingly, V_{IADJ2} continues decreasing to further reduce the LED current. When the LED current drops to X% (set by R_{TEMPA}), the current keeps constant. If the temperature of LED board continues rising, the value of NTC thermistor continues decreasing, and V_{IADJ2} continues decreasing also. When the V_{IADJ2} drops to Y [V] (set by R_{TEMPB}), the PT16751 gate driver stops working. LED current drops to Zero.

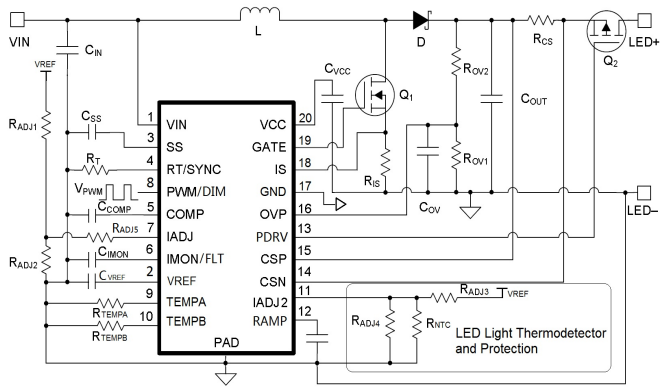


Figure 10. Typical Application

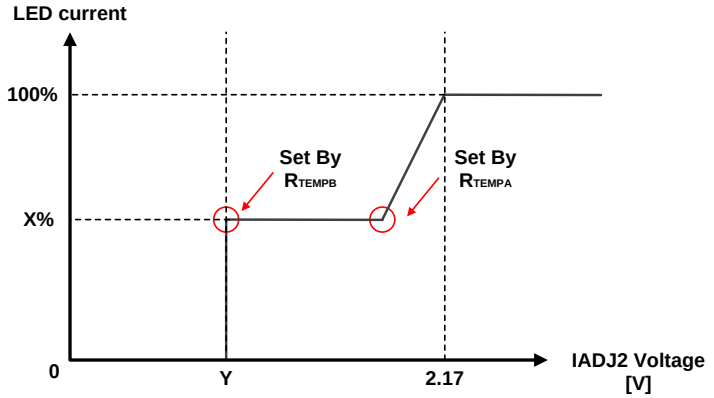


Figure 11. LED current VS IADJ2 Voltage

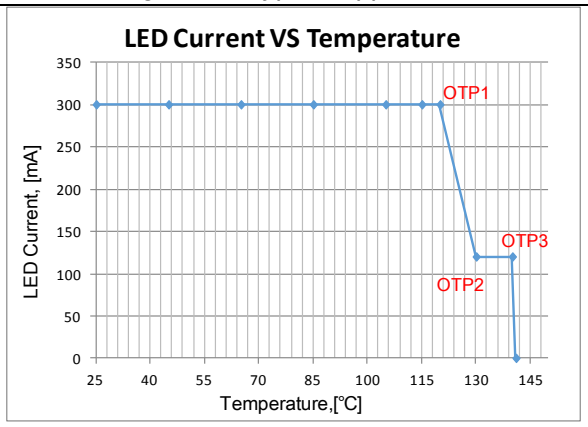


Figure 12. LED current VS LED board temperature

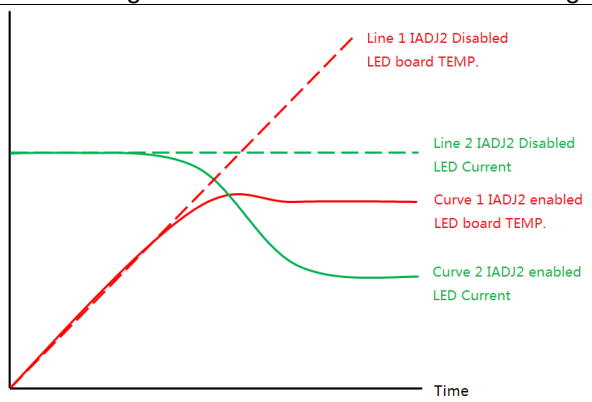


Figure 13. Effect of IADJ2 function for LED board temperature and LED current

For example, as shown in Figure 12, the rated LED current is 300mA, the first over temperature protection threshold **OTP1** is set to 120 ℃, V_{IADJ2} is 2.17V, the LED current begins to decrease. The second over temperature protection threshold **OTP2** is set to 130 ℃ (set by R_{TEMPA}), and the LED current keeps constant at 120mA (40% I_{LED}). The third over temperature protection threshold **OTP3** is set to 140 ℃ (set by R_{TEMPB}), V_{IADJ2} is Y [V], and the LED light is turned off. Figure 13 shows the effect of the IADJ2 Over Temperature Protection(OTP) function on LED board temperature and LED current. Without IADJ2 OTP function, the LED current keeps constant(Line 2), but the LED board temperature (Line 1) continues rising. As working time increase, the LEDs be burned out if the LED board heat dissipation is not good. When the IADJ2 OTP protection function is enabled, as the LED board temperature increases, the LED current will decrease and the LED board temperature keeps constant.

Refer the PT16751 design tool to calculate R_{TEMPA}, R_{TEMPB}, R_{ADJ4} and R_{ADJ5}.

5.10 RAIL-TO-RAIL CURRENT SENSE AMPLIFIER

The PT16751 incorporates a high voltage rail-to-rail current sense amplifier to measure the average current of LED string based on the differential voltage drop between the CSP and CSN inputs over a common mode range of 3 V to 65 V. The differential voltage, V_{CSP}-V_{CSN} is amplified by a voltage-gain factor of 14, and connected to the negative input of the transconductance error amplifier. Accurate LED current feedback is achieved by limiting the cumulative input offset voltage, (represented by the sum of the voltage-gain error, the intrinsic current sense offset voltage, and the transconductance error amplifier offset voltage) to less than 5 mV over the recommended common-mode voltage, and temperature range.

Figure 14 shows a recommended common-mode or differential mode low-pass filter circuit, which can be used to eliminate the effects of large output current ripple and switching current spikes caused by diode reverse recovery. PT16751 recommends that the filter resistance should be between 10 Ω and 100 Ω to limit the additional offset caused by amplifier bias current and achieve best accuracy and line regulation.

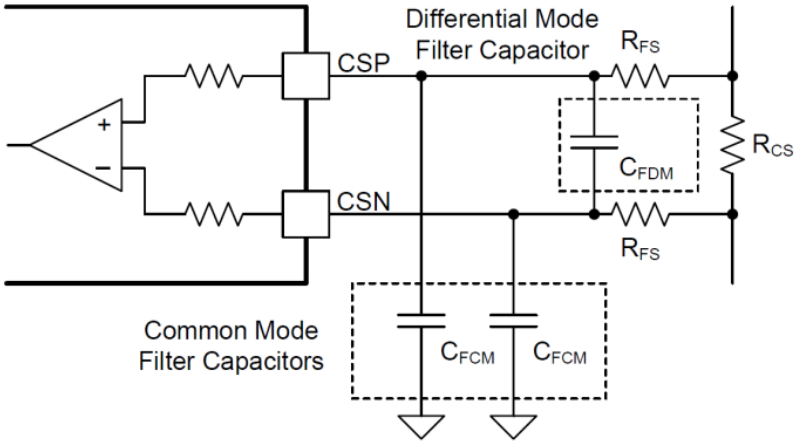


Figure 14. Current Sense Amplifier Input Filter Options

5.11 SERIES P-CHANNEL FET DIMMING GATE DRIVER OUTPUT

The PDRV output is a function of the internal PWM signal and is capable of sinking and sourcing up to 50 mA of peak current to control a high-side series connected P-channel dimming FET. The PDRV switches between V_{CSP} and (V_{CSP}– 7 V) based on the status of PWM signal to completely turn-off and turn-on the external P-channel dimming FET. The series dimming FET is required to achieve high contrast ratio as it ensures fast rise and fall times of the LED current in response to the PWM input. Without any dimming FET, the rise and fall times are limited by the inductor slew rate and the closed-loop bandwidth of the system.

The series P-channel MOSFETs can also limit the output current when the LED+ is shorted to LED-, so that the series P-channel MOSFET is necessary and do not leave the PDRV pin unconnected.

5.12 OUTPUT OVERVOLTAGE PROTECTION

The PT16751 device includes a dedicated OVP pin which can be used for either input or output overvoltage protection. This pin features a precision 1.23 V (typ) threshold with 20-μA (typ) of hysteresis current. The overvoltage threshold limit is set by a resistor divider network from the input or output terminal to GND. When the OVP pin voltage exceeds the reference threshold, the GATE pin is immediately pulled low, the PDRV output is disabled, and the SS and COMP capacitors are discharged. The GATE and PDRV outputs are enabled and a new startup sequence is initiated after the voltage drops below the hysteresis threshold set by the 20-μA source current and the external resistor divider. The overvoltage fault threshold is calculated as follows:

$$V_{OV} = 1.23 \times (1+\frac{R_{OV2}}{R_{OV1}})$$

The device also indicates a short-circuit condition when the voltage across the OVP pin and GND falls below 100 mV. In this case, the output voltage, V_O, is below the undervoltage fault threshold determined based on the resistor divider connected to the OVP pin.

$$V_{O(UV)} = 0.1 \times \frac{R_{OV1}+R_{OV2}}{R_{OV1}}$$

The undervoltage fault detection circuit is internally disable based on the SS pin voltage and internal PWM status. The fault blanking circuit is designed to prevent false undervoltage detection during the startup sequence and PWM dimming operation.

5.13 SWITCH CURRENT SENSE

The IS input pin monitors the main MOSFET current to implement peak current mode control. The GATE output duty cycle is derived by comparing the peak switch current, measured by the R_{IS} resistor, to the internal COMP voltage threshold. An internal slope signal, V_{SL}, generated by slope compensation circuit is added to the measured sense voltage, V_{IS}, to prevent sub-harmonic oscillations for duty cycles greater than 50%. An internal blanking circuit prevents MOSFET switching current spike propagation and premature termination of duty cycle by internally shunting the IS input for 150 ns after the beginning of the new switching period. For additional noise suppression connect an external low-pass RC filter with resistor values ranging from 100 Ω to 500 Ω and a 1000 pF capacitor. The external RC filter ensures proper operation when operating in the dropout region (VIN less than 7 V).

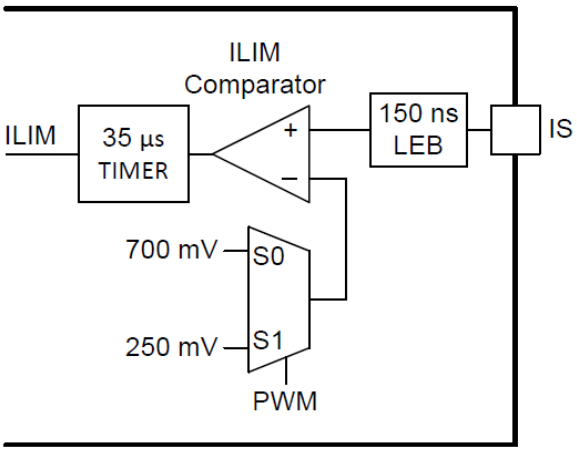


Figure 15. Switch Current Limit Circuit

Cycle-by-cycle current limit is accomplished by a redundant internal comparator. The current limit threshold is set based on the status of internal PWM signal. The current limit threshold is set to 250 mV (typ) when PWM signal is high and to 700 mV (typ) when PWM signal is low. The transition between the two thresholds work in conjunction with slope compensation and the error amplifier circuit to allow for higher inductor current immediately after the PWM transition and to improve LED current transient response during PWM dimming. Refer to the PWM/DIM Input section for details on PWM Dimming operation.

The device immediately terminates the GATE and PDRV output when the IS input voltage, V_{IS}, exceeds the threshold value. Upon a current limit event, the SS and COMP pin are internally grounded to reset the state of the controller. The GATE output is enabled after the expiration of the 35-µs internal fault timer and a new start-up sequence is initiated through the SS pin. **Equation 3** calculates the peak inductor current in the current limit.

$$I_{L(PK)} = \frac{250mV}{R_{IS}} (A) \quad (3)$$

5.14 GATE DRIVER

The PT16751 device contains a N-channel gate driver that switches the output V_{GATE} between VCC and GND. A peak source and sink current of 500 mA allows controlled slew-rate of the MOSFET gate and drain node voltages, limiting the conducted and radiated EMI generated by switching.

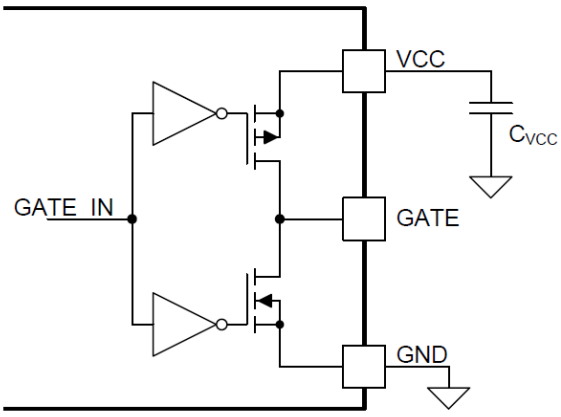


Figure 16. Push-Pull N-Channel Gate Driver Circuit

The gate driver supply current $I_{CC(GATE)}$ depends on the total gate drive charge (Q_G) of the MOSFET and the operating frequency of the converter, f_{SW}, $I_{CC(GATE)} = Q_G \times f_{SW}$. Choose a MOSFET with a low gate charge specification to limit the junction temperature rise and switch transition losses.

It is important to consider the MOSFET threshold voltage when operating in the dropout region when the input voltage, V_{IN}, is below the VCC regulation level. It recommends a logic level device with a threshold voltage below 5 V when the device is required to operate at an input voltage less than 7 V.

5.15 THERMAL PROTECTION

Internal thermal shutdown circuitry is implemented to protect the controller in the event the maximum junction temperature is exceeded. When activated, typically at 180°C, the controller is forced into a shutdown mode, disabling the internal regulator. This feature is designed to prevent overheating and damage to the device.

6. ABSOLUTE MAXIMUM RATINGS

		MIN	MAX	UNIT
Input voltage	VIN, CSP, CSN	-0.3	65	V
	PWM/DIM	-0.3	14	V
	IS, RT/SYNC	-0.3	8.8	V
	OVP, IADJ, IADJ2	-0.3	5.5	V
	CSP to CSN	-0.3	0.3	V
Output voltage	VCC, GATE	-0.3	8.8	V
	PDRV	V_{CSP} – 8.8	V_{CSP}	V
	VREF, IMON/FLT, SS, RAMP, TEMPA, TEMPB	-0.3	5.5	V
	COMP	-0.3	5.0	V
Source current	IMON/FLT	--	100	µA
	GATE (pulsed < 20 ns)	--	500	mA
	PDRV (pulsed < 10 us)	--	50	mA
Sink current	GATE (pulsed < 20 ns)	--	500	mA
	PDRV (pulsed < 10 us)	--	50	mA
Operating junction temperature, T_J		-40	150	°C
Storage temperature, T_{stg}		-40	150	°C

7. ESD RATINGS

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM)	±2000	V
		Charged-device model (CDM)	±800	
		Machine Mode (MM)	±250	

8. RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VIN	Supply input voltage	6.5	14	65	V
V_{CSP}, V_{CSN}	Current sense common mode	2		60	V
f_{SW}	Switching frequency	80		800	kHz
f_{RAMP}	Internal PWM ramp generator frequency	100		2000	kHz
V_{IADJ}	Current reference voltage	0.14		$V_{IADJ(CLAMP)}$	V
T_A	Operating ambient temperature	–40		125	°C

9. THERMAL INFORMATION

THERMAL METRIC			UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	40.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.3	°C/W

10. ELECTRICAL CHARACTERISTICS

–40°C ≤ T_J ≤ 150°C, V_{IN} = 14 V, V_{IADJ} = 2.1 V, V_{RAMP} = 500 mV, $V_{PWM/DIM}$ = 3 V, V_{OV} = 500 mV, C_{VCC} = 1 µF, C_{VREF} = 1 µF, C_{COMP} = 2.2 nF, R_{CS} = 100 mΩ, R_T = 20 kΩ, no load on GATE and PDRV (unless otherwise noted)

PARAMETE		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE (VIN)						
$I_{IN(STBY)}$	Input stand-by current	V_{PWM} = 0 V		2	3	mA
$I_{IN(SW)}$	Input switching current	V_{CC} = 7.5 V, C_{GATE} = 1 nF		5.5	6.6	mA
BIAS SUPPLY (VCC)						
$V_{CC(REG)}$	Regulation voltage	No load	7.0	7.5	8.0	V
$V_{CC(UVLO)}$	Supply undervoltage protection	VCC rising threshold, V_{IN} = 8 V		4.5	4.9	V
		VCC falling threshold, V_{IN} = 8 V	3.7	4.1		V
		Hysteresis		400		mV
$I_{CC(LIMIT)}$	Supply current limit	V_{CC} = 0 V	36	42	48	mA
V_{DO}	LDO dropout voltage	I_{CC} = 20 mA, V_{IN} = 5 V		300		mV
REFERENCE VOLTAGE (VREF)						
V_{REF}	Reference voltage	No load	4.87	5.07	5.27	V
$I_{REF(LIMIT)}$	Current limit	V_{REF} = 0 V	28	34	40	mA
OSCILLATOR (RT)						
f_{SW}	Switching frequency	R_T = 40 kΩ	160	200	240	kHz
		R_T = 20 kΩ	340	400	460	kHz
V_{RT}	RT output voltage			1		V
V_{SYNC}	SYNC rising threshold	V_{RT} rising		2.5	3.1	V
	SYNC falling threshold	V_{RT} falling	1.8	2		V
$t_{SYNC(MIN)}$	Minimum SYNC clock pulse width			100		ns
GATE DRIVER (GATE)						
R_{GH}	Gate driver high side resistance	I_{GATE} = –10 mA		5.2	11.5	Ω
R_{GL}	Gate driver low side resistance	I_{GATE} = 10 mA		4.5	11.2	Ω
CURRENT SENSE (IS)						
$V_{IS(LIMIT)}$	Current limit threshold	$V_{PWM/DIM}$ = 5 V, R_{RAMP} = 250 kΩ	235	250	265	mV
		$_{PWM/DIM}$ = 0 V, R_{RAMP} = 250 kΩ	660	700	740	mV
$t_{IS(BLANK)}$	Leading edge blanking time		85	115	155	ns
$t_{IS(FAULT)}$	Current limit fault time			33		µs
$t_{ILMT(DLY)}$	IS to GATE propagation delay	V_{IS} pulsed from 0 V to 1 V		105		ns
PWM COMPARATOR AND SLOPE COMPENSATION (SLOPE)						
D_{MAX}	Maximum duty cycle			90		%
V_{SLOPE}	Slope compensation			400		mV
V_{LV}	IS to COMP level shift voltage	No slope compensation added	1.37	1.50	1.8	V
I_{LV}	IS level shift bias current	No slope compensation added		25		µA
CURRENT SENSE AMPLIFIER (CSP, CSN)						
$V_{(CSP-CSN)}$	Current sense thresholds	V_{CSP} = 14 V, V_{IADJ} = 3 V	160	170	180	mV
		V_{CSP} = 14 V, V_{IADJ} = 1.4 V	95	100	105	mV
$CS_{(BW)}$	Current sense unity gain bandwidth			500		kHz
G_{CS}	Current sense amplifier gain	G = $V_{IADJ}/V_{(CSP-CSN)}$		14		
$K_{(OCP)}$	Ratio of over-current detection threshold to analog adjust voltage	K $_{(OCP)}$ = $V_{(OCP-THR)}/V_{IADJ}$	1.45	1.5	1.6	
$I_{CSP(BIAS)}$	CSP bias current			100		µA
$I_{CSN(BIAS)}$	CSN bias current			100		µA

Electrical Characteristics (continued)

PARAMET		TEST CONDITIONS	MIN	TYP		UNIT
CURRENT MONITOR (IMON)						
$I_{IMON(SRC)}$	IMON source current	$V_{(CSP-CSN)}$ = 150 mV, V_{IMON} = 0 V		100		µA
$V_{IMON(FLT)}$	IMON fault output voltage		4.87	5.07	5.27	V
$V_{IMON(CLP)}$	IMON output clamp voltage		3.2	3.7	4.2	V
$V_{IMON(OS)}$	IMON buffer offset voltage			0		mV
ANALOG ADJUST (IADJ)						
$V_{IADJ(CLP)}$	IADJ internal clamp voltage	I_{IADJ} = 1 µA	2.29	2.40	2.55	V
$I_{IADJ(BIAS)}$	IADJ input bias current	V_{IADJ} < 2.2 V		10.5		nA
$R_{IADJ(LMT)}$	IADJ current limiting series resistor	V_{IADJ} > 2.6 V		10		kΩ
ERROR AMPLIFIER (COMP)						
g_M	Transconductance			121		µA/V
$I_{COMP(SRC)}$	COMP current source capacity	V_{IADJ} = 1.4 V, $V_{(CSP-CSN)}$ = 0 V		130		µA
$I_{COMP(SINK)}$	COMP current sink capacity	V_{IADJ} = 0 V, $V_{(CSP-CSN)}$ = 0.1 V		130		µA
$EA_{(BW)}$	Error amplifier bandwidth	Gain = –3 dB		5		MHz
$V_{COMP(RST)}$	COMP pin reset voltage			100		mV
$R_{COMP(DCH)}$	COMP discharge FET resistance			250		Ω
SOFT-START (SS)						
I_{SS}	Soft-start source current			10		µA
$V_{SS(UVP\_EN)}$	Soft-start voltage threshold to enable output under-voltage protection			2.4		V
$V_{SS(RST)}$	Soft-start pin reset voltage			50		mV
$R_{SS(DCH)}$	SS discharge FET resistance			250		Ω
OUTPUT VOLTAGE INPUT (OV)						
$V_{OVP(THR)}$	Overvoltage protection threshold		1.2	1.23	1.26	V
$V_{UVP(THR)}$	Undervoltage protection threshold		85	100	115	mV
$t_{(UVP-BLANK)}$	Undervoltage protection blanking			4		µs
$I_{OVP(HYS)}$	OVP hysteresis current		12	20	27.5	µA
INTERNAL PWM RAMP GENERATOR (RAMP)						
I_{RAMP}	Ramp generator source current		7.5	10	12.5	µA
	Ramp generator sink current		8.5	10	11.5	µA
V_{RAMP}	Ramp signal peak (high)			3		V
	Ramp signal valley (low)			1		V
PWM INPUT (PWM/DIM)						
$V_{PWM(HIGH)}$	Trigger logic level (high threshold)	V_{RAMP} = 2.0 V		2.0	2.2	V
$V_{PWM(LOW)}$	Trigger logic level (low threshold)	V_{RAMP} = 2.0 V	1.8	2.0		V
$R_{PWM(PD)}$	PWM pull-down resistance			10		MΩ
$t_{DLY(RISE)}$	PWM rising to PDRV delay	C_{PDRV} = 1 nF		300		ns
$t_{DLY(FALL)}$	PWM falling to PDRV delay	C_{PDRV} = 1 nF		330		ns
SERIES P-CHANNEL PWM FET GATE DRIVE OUTPUT (PDRV)						
$V_{PDRV(OFF)}$	P-channel gate driver off-state voltage	V_{CSP} = 14 V		14		V
$V_{PDRV(ON)}$	P-channel gate driver on-state voltage	V_{CSP} = 14 V		7.4		V
$I_{PDRV(SRC)}$	PDRV sink current	Pulsed		50		mA
$R_{PDRV(L)}$	PDRV driver pull up resistance			86		Ω
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown temperature			180		°C
$T_{SD(HYS)}$	Thermal shutdown hysteresis			30		°C

11. DESIGN GUIDE

APPLICATION CIRCUIT

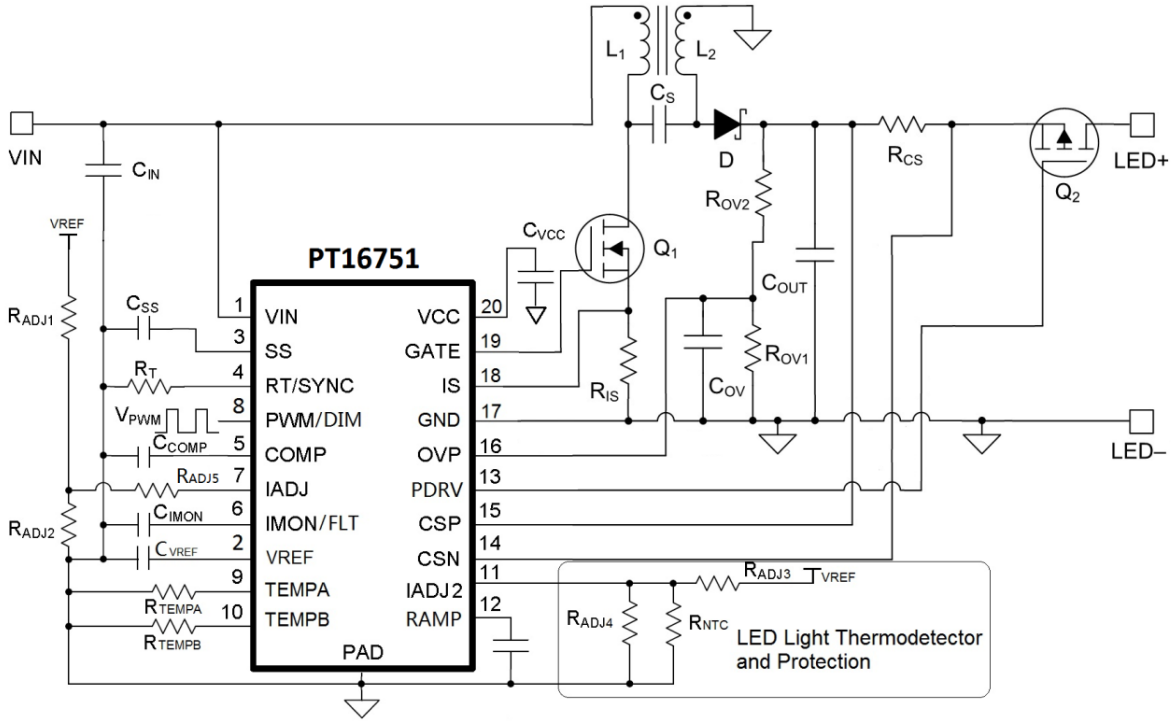


Figure 17. SEPIC LED Driver

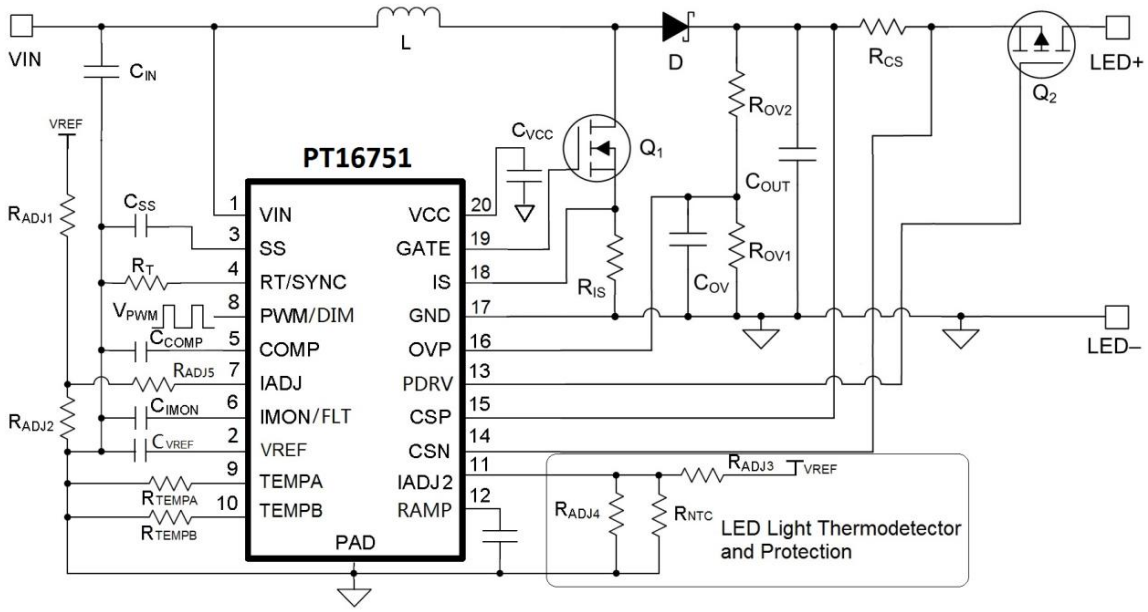


Figure 18. Boost LED Driver

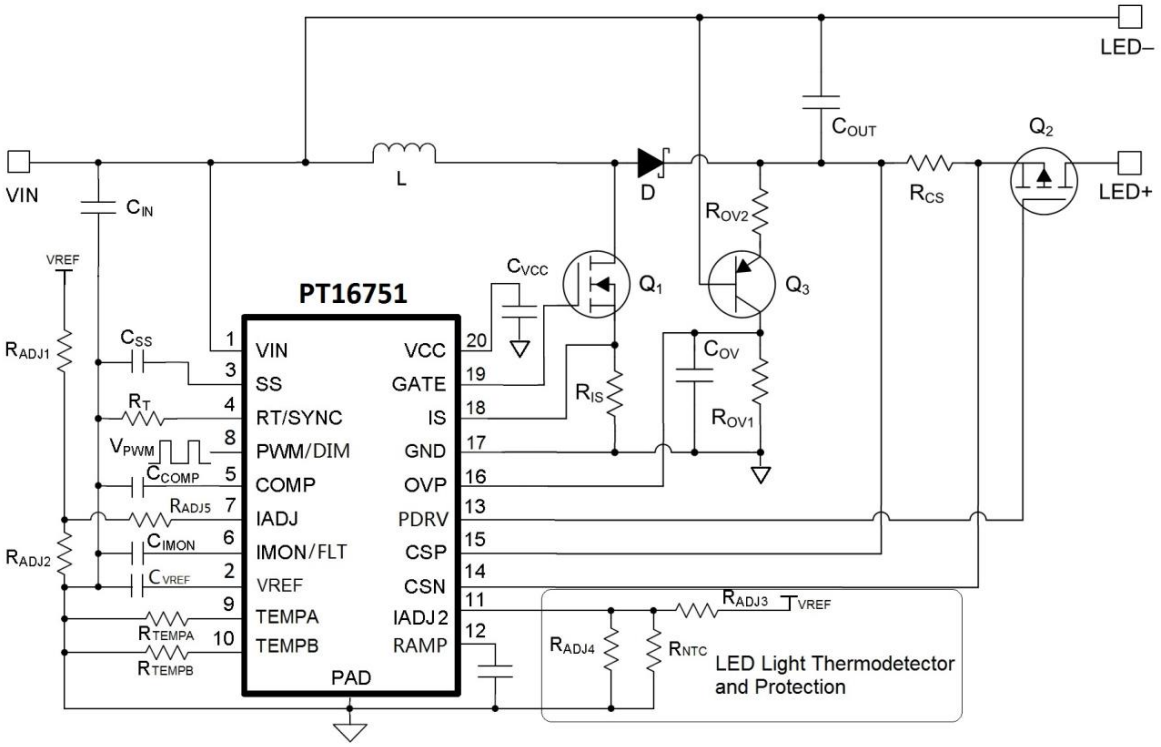


Figure 19. Buck-Boost LED Driver

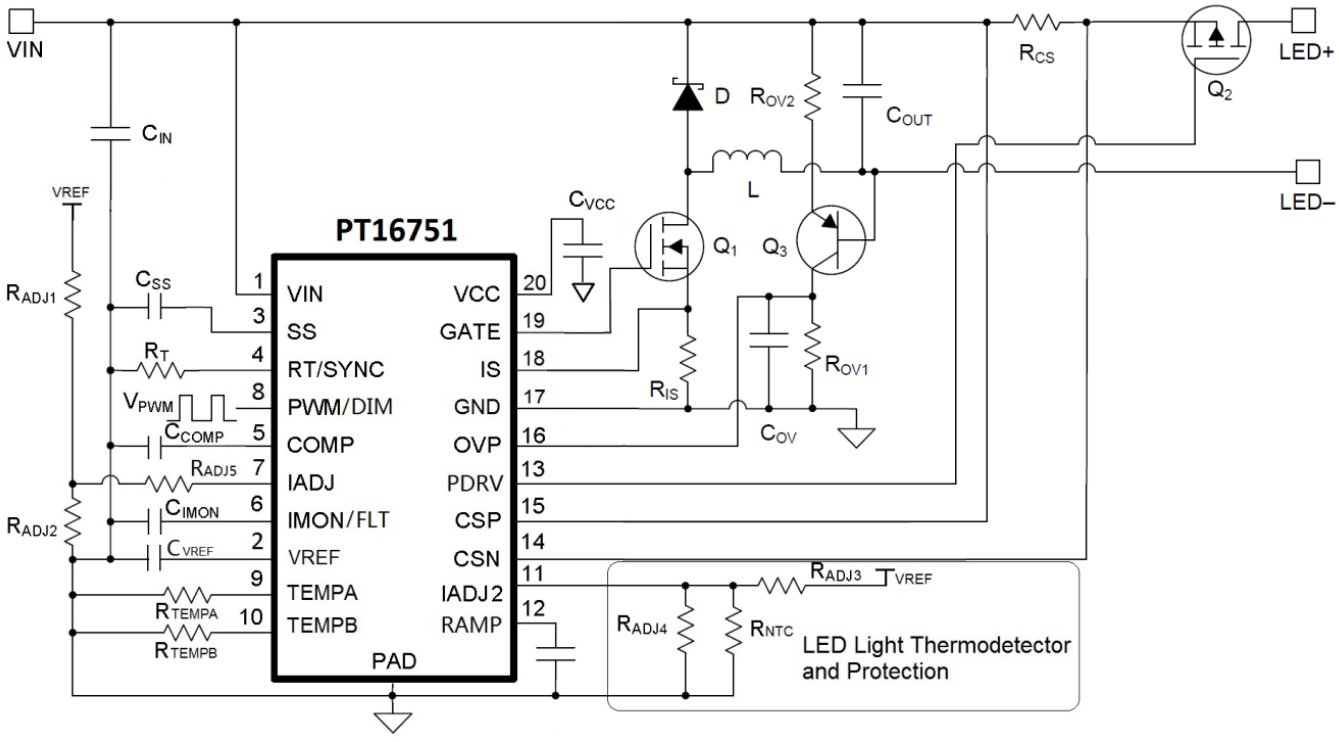


Figure 20. Buck LED Driver

DESIGN PROCEDURE

1. Duty Cycle Calculation

The switching duty cycle (D) defines the converter operation, and is related to the input and output voltages. In steady state, the duty cycle is calculated using following expression:

Buck:	Boost:	SEPIC/Buck-Boost:
$D = \frac{V_O}{V_{IN}}$	$D = \frac{V_O - V_{IN}}{V_O}$	$D = \frac{V_O}{V_O + V_{IN}}$
$D_{MIN} = \frac{V_O}{V_{IN(MAX)}}$	$D_{MIN} = \frac{V_O - V_{IN(MAX)}}{V_O}$	$D_{MIN} = \frac{V_O}{V_O + V_{IN(MAX)}}$
$D_{MAX} = \frac{V_O}{V_{IN(MIN)}}$	$D_{MAX} = \frac{V_O - V_{IN(MIN)}}{V_O}$	$D_{MAX} = \frac{V_O}{V_O + V_{IN(MIN)}}$

The duty cycle must be within the operating range of the controller to ensure that the closed-loop LED current regulation is in the specified input and output voltage range.

2. Inductance Calculation

Consider a good compromise between core loss and copper loss of the inductor, the inductor peak-to-peak ripple current, $\Delta i_{L\text{-}PP}$, is typically set between 20% and 80% of the maximum inductor current, I_L. Higher ripple inductor current allows a smaller inductor size, but needs more capacitors on the output to smooth the LED current ripple. Knowing the desired ripple ratio RR, switching frequency f_{SW}, maximum duty cycle D_{MAX}, and the typical LED current I_{LED}, the inductor value can be calculated as follows:

Buck:

$$\Delta i_{L(PP)} = RR \times I_L = RR \times I_{LED}$$

$$L = \frac{(V_{IN(MIN)} - V_O) \times D_{MAX}}{\Delta i_{L(PP)} \times f_{SW}}$$

Boost and Buck-Boost (SEPIC):

$$\Delta i_{L(PP)} = RR \times I_L = RR \times \frac{I_{LED}}{1 - D_{MAX}}$$

$$L = \frac{V_{IN(MIN)} \times D_{MAX}}{\Delta i_{L(PP)} \times f_{SW}}$$

As an alternative, the inductor can be selected based on CCM-DCM boundary condition specified based on output power, $P_{O(BDRY)}$. This approach ensures CCM operation in battery-powered LED driver applications that are required to support different LED string configurations with a wide range of programmable LED current set points. The CCM-DCM boundary condition can be estimated based on the lowest LED current and the lowest output voltage requirements for a given application.

$$P_{O(BDRY)} \leqslant I_{LED(MIN)} \text{ X } V_{O(MIN)}$$

Buck:

$$L = \frac{V_{O(MAX)}^2}{2 \times P_{O(BDRY)} \times f_{SW}} \times (1 - \frac{V_{OUT(MAX)}}{V_{IN}})$$

Boost:

$$L = \frac{V_{IN}^2}{2 \times P_{O(BDRY)} \times f_{SW}} \times (1 - \frac{V_{IN}}{V_{O(MAX)}})$$

Buck-Boost and SEPIC:

$$L = \frac{1}{2 \times P_{O(BDRY)} \times f_{SW} \times (\frac{1}{V_{O(MAX)}} + \frac{1}{V_{IN}})^2}$$

Select inductor with saturation current rating greater than the peak inductor current, $I_{L(PK)}$, at the maximum operating temperature.

$$I_{L(PK)} = I_L + \frac{V_{IN(MIN)} \times D_{MAX}}{2 \times L \times f_{SW}}$$

3. Input Capacitor Value Calculation

The input capacitors, C_{IN}, smooth the input voltage ripple and store energy to supply input current during input voltage drop or PWM dimming transients. In the Boost, SEPIC, and Cuk topology, the series inductor provides continuous input current so that requires a smaller input capacitor to achieve desired input ripple voltage, $\Delta v_{IN(PP)}$.

The Buck and Buck-Boost topology have discontinuous input current, and larger capacitors are required to achieve the same input voltage ripple. Based on the switching frequency, f_{SW}, and the maximum duty cycle, D_{MAX}, the input capacitor value can be calculated as follows:

Buck:

$$C_{IN} = \frac{I_{LED} \times D_{MAX} \times (1 - D_{MAX})}{f_{SW} \times \Delta v_{IN(PP)}}$$

Boost:

$$C_{IN} = \frac{\Delta i_{L(PP)}}{8 \times f_{SW} \times \Delta v_{IN(PP)}}$$

Buck-Boost:

$$C_{IN} = \frac{I_{LED} \times D_{MAX}}{f_{SW} \times \Delta v_{IN(PP)}}$$

For most applications, it highly recommends to select X7R dielectric-based ceramic capacitors due to their low ESR, high ripple current rating, and good temperature performance. For PWM dimming application, aluminum electrolytic capacitor and ceramic capacitor are recommended to minimize the voltage deviation due to large input current transients generated in conjunction with the rising and falling edges of the LED current.

Decouple VIN pin with a 0.1-μF ceramic capacitor, placed as close as possible to the device and a series 10Ω resistor to create a 150-kHz low-pass filter and eliminate undesired high-frequency noise.

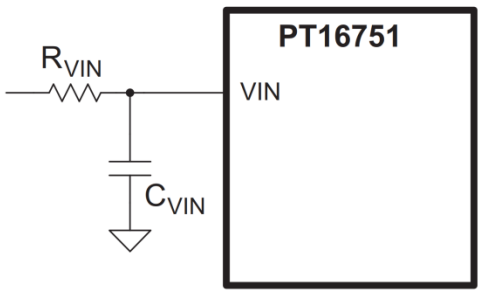


Figure 21. VIN Filter

4. Output Capacitor Value Calculation

Using the output capacitors to attenuate the discontinuous or large ripple current generated by switching and achieve the desired LED output current ripple, $\Delta i_{LED(PP)}$. The capacitor value depends on the total series resistance of the LED string, rD and the switching frequency, f_{SW}. The capacitance required for the target LED ripple current can be calculated based on following equations.

Buck:

$$C_{OUT} = \frac{\Delta i_{L(PP)}}{8 \times f_{SW} \times r_D \times \Delta i_{LED(PP)}}$$

Boost and Buck-Boost:

$$C_{OUT} = \frac{I_{LED} \times D_{MAX}}{f_{SW} \times r_D \times \Delta i_{LED(PP)}}$$

For the Buck topology, the inductor is in series with LED load and requires a smaller capacitor than the Boost, Buck-Boost, and SEPIC topologies to achieve the same LED ripple current.

The ESR and the ESL characteristics must be considered when selecting the output capacitors, as they directly impact the LED current ripple. Ceramic capacitors are the best choice because of its low ESR, high ripple current rating, long lifetime, and good temperature performance. When selecting ceramic capacitors, it is important to consider the derating factors associated with higher temperature and DC bias operating conditions.

It is recommended to use X7R dielectric with rated voltage greater than the maximum LED voltage. Aluminum electrolytic capacitors can be used in parallel with ceramic capacitors to provide large capacity energy storage. The aluminum capacitors must have the necessary RMS current and temperature ratings to ensure extended operating lifetime. The minimum allowable output capacitor RMS current rating, $I_{COUT(RMS)}$, can be approximated

Buck:

$$I_{COUT(RMS)} = \frac{\Delta i_{LED(PP)}}{\sqrt{12}}$$

Boost and Buck-Boost:

$$I_{COUT(RMS)} = I_{LED} \times \sqrt{\frac{D_{MAX}}{1 - D_{MAX}}}$$

For applications that need to support different LED string configurations with a wide range of programmable LED current set points, rearrange the previous expressions based on the maximum output power to reflect output capacitance, to ensure that LED current ripple meets the requirements over the entire range of operation.

5. LED Current Programming

The LED current is set by the current sense resistor, R_{CS}, and the analog adjust voltage, V_{IADJ}. The current sense resistor is placed in series with the LED load. The CSP and CSN inputs of the internal rail-to-rail current sense amplifier are connected to the RCS resistor to achieve closed-loop regulation. When VIADJ > 2.42 V, the internal reference clamps the $V_{(CSP-CSN)}$ to 0.173V, the LED current is set by flowing equation:

$$I_{LED} = \frac{0.173}{R_{CS}}$$

The LED current can be programmed by varying V_{IADJ} between 140 mV to 2.25 V. The LED current can be calculated using:

$$I_{LED} = \frac{V_{IADJ}}{14 \times R_{CS}}$$

Using a low-pass common-mode filter consisting of 10Ω resistors in series with CSP and CSN inputs, and place 0.01uF capacitor to ground to the minimize the impact of voltage ripple and noise on LED current accuracy (see Figure 14). A 0.1μF capacitor across CSP and CSN is included to filter high-frequency differential noise.

6. PWM Dimming Suggestion

The device can be configured to implement dimming function based on external PWM command by disabling the internal ramp generator, as explained in PWM/ DIM Input section. The internal comparator reference is set to 2.5 V by connecting a 250-kΩ resistor, RRAMP, from the RAMP pin to GND. The internal PWM duty cycle is controlled by an external 5 V or 3.3 V signal, generated by a command module or a microcontroller.

When PWM dimming, the device requires another P-channel MOSFET placed in series with the LED load. Select a P-channel MOSFET with gate-to-source voltage rating of 10 V or higher and with a drain-to-source breakdown voltage rating greater than the output voltage. Ensure that the drain current rating of the P-channel MOSFET exceeds the programmed LED current by at least 10%.
It is important to consider the FET input capacitance and on-resistance as it impacts the accuracy and efficiency of the LED driver. It recommends a FET with lower input capacitance and gate charge to minimize the errors caused by rise and fall times when PWM dimming at low duty cycles.

7. Main Power MOSFET Selection

The power MOSFET should be able to endure the maximum switch node voltage, VSW, and switch RMS current derived based on the converter topology. In order to ensure safe operation, the drain voltage VDS is at least 20% greater than the maximum switch node voltage. The MOSFET Drain-Source breakdown voltage, VDS, and RMS current ratings are calculated using the following expressions.
Buck:

$$V_{DS} = V_{IN(MAX)} \times 1.2$$

$$I_{Q(RMS)} = I_{LED} \times \sqrt{D_{MAX}}$$

Boost:

$$V_{DS} = V_{O(OV)} \times 1.2$$

$$I_{Q(RMS)} = I_{LED} \times \frac{\sqrt{D_{MAX}}}{1 - D_{MAX}}$$

Buck-Boost:

$$V_{DS} = (V_{IN(MAX)} + V_{O(OV)}) \times 1.2$$

$$I_{Q(RMS)} = I_{LED} \times \frac{\sqrt{D_{MAX}}}{1 - D_{MAX}}$$

Where the voltage, $V_{O(OV)}$, is the overvoltage protection threshold and the worst-case output voltage under fault conditions.
A MOSFET with low total gate charge, Q_g is selected to minimize gate drive and switching losses. The R_{DS} resistance of MOSFET is usually an unimportant parameter because the switch conduction losses are not a significant part of the total converter losses at high operation frequency. The switching and conduction losses are calculated as follows:

$$P_{COND} = R_{DS} \times I_{Q(RMS)}^2$$

$$P_{SW} = \frac{I_L \times V_{SW}^2 \times C_{RSS} \times f_{SW}}{I_{GATE}}$$

C_{RSS} is the MOSFET reverse transfer capacitance. I_L is the average inductor current. I_{GATE} is gate drive output current, typically 500 mA. The MOSFET power rating and package should be selected based on the total calculated loss, the ambient operating temperature, and maximum allowable temperature rise.

8. Rectifier Diode Selection

It suggest that use a Schottky diode as rectifier diode, because it provides the best efficiency due to the low forward voltage drop and near-zero reverse recovery time. Choose a diode with a reverse breakdown voltage, $V_{D(BR)}$, greater than or equal to MOSFET drain-to-source voltage, V_{DS}, for reliable performance. It is important to understand the leakage current characteristics of the Schottky diode, especially at high operating temperatures because it impacts the overall converter operation and efficiency.
The current through the diode, I_D, is given by:

$$I_D = I_L \times (1 - D_{MAX})$$

The diode power rating and package is selected based on the calculated current, the ambient temperature and the maximum allowable temperature rise.

9. Switch Current Sense Resistor

The switch current sense resistor, RIS, is used for peak current mode control and to set the peak current limit. The value of R_{IS} is selected to protect the main switching MOSFET under fault conditions. The R_{IS} can be calculated based on peak inductor current, $I_{L(PK)}$, and switch current limit threshold, $V_{IS(LIMIT)}$.

$$R_{IS} = \frac{V_{IS(LIMT)}}{I_{L(PK)}}$$

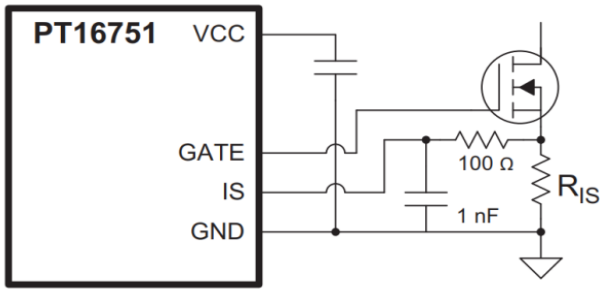


Figure 22. IS Input Filter

The use of a 1nF and 100Ω low-pass filter is optional. If used, the resistor value should be less than 500 Ω to limit its influence on the internal slope compensation signal.

10. Feedback Compensation

The open-loop response is the product of the modulator transfer function and the feedback transfer function. Using a first-order approximation, the modulator transfer function can be modeled as a single pole created by the output capacitor, and in the boost and buck-boost topologies, a right half-plane zero created by the inductor, where both have a dependence on the LED string dynamic resistance, r_D. Because it recommends a ceramic capacitor, the ESR of the output capacitor is neglected in the analysis. The small-signal modulator model also includes a DC gain factor that is dependent on the duty cycle, output voltage, and LED current.

$$\frac{\hat{i}_{LED}}{\hat{v}_{COMP}} = G_0 \frac{\left(1-\frac{s}{\omega_Z}\right)}{\left(1+\frac{s}{\omega_P}\right)}$$

Table 1 summarizes the expression for the small-signal model parameters.

	DC GAIN (G_0)	POLE FREQUENCY (ω_P)	ZERO FREQUENCY (ω_Z)
Buck	1	$\frac{1}{r_D \times C_{OUT}}$	/
Boost	$\frac{(1-D)\times V_O}{R_{IS}\times(V_O+(r_D\times I_{LED}))}$	$\frac{V_O+(r_D\times I_{LED})}{V_O\times r_D\times C_{OUT}}$	$\frac{V_O\times(1-D)^2}{L\times I_{LED}}$
Buck-Boost	$\frac{(1-D)\times V_O}{R_{IS}\times(V_O+(D\times r_D\times I_{LED}))}$	$\frac{V_O+(D\times r_D\times I_{LED})}{V_O\times r_D\times C_{OUT}}$	$\frac{V_O\times(1-D)^2}{D\times L\times I_{LED}}$

The feedback transfer function includes the current sense resistor and the loop compensation of the transconductance amplifier. A compensation network at the output of the error amplifier is used to configure loop gain and phase characteristics. A simple capacitor, C_{COMP}, from COMP to GND (as shown in Figure 23) provides integral compensation and creates a pole at the origin. Alternatively, a network of R_{COMP}, C_{COMP}, and C_{HF}, shown in Figure 24, can be used to implement proportional and integral (PI) compensation and to create a pole at the origin, a low-frequency zero, and a high-frequency pole.

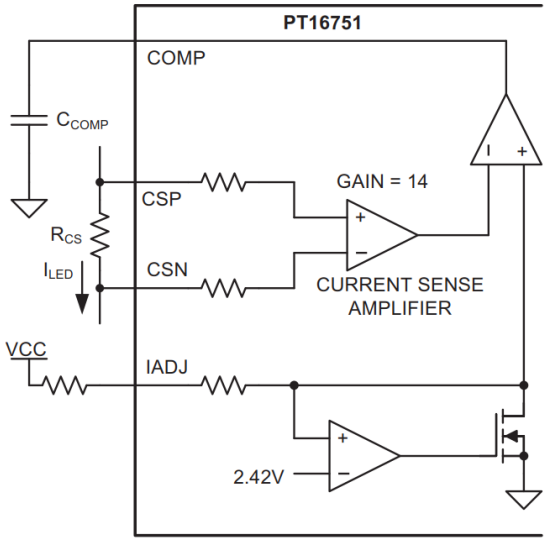


Figure 23. Integral Compensation

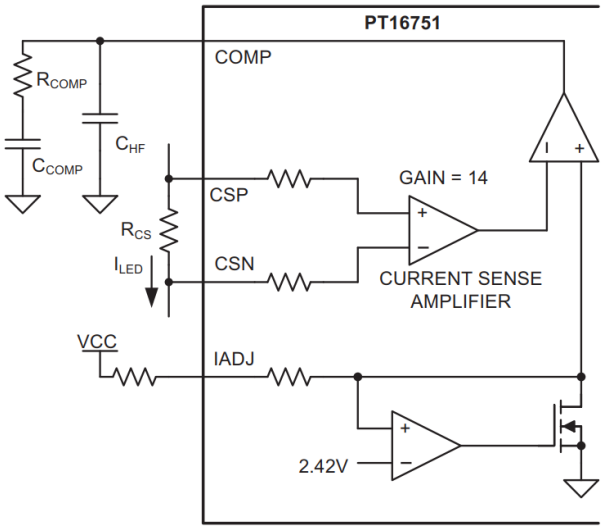


Figure 24. Proportional-Integral Compensation

The feedback transfer function is defined as follows.
Feedback transfer function with integral compensation:

$$-\frac{\hat{v}_{COMP}}{\hat{i}_{LED}} = \frac{14 \times g_M \times R_{CS}}{s \times C_{COMP}}$$

Feedback transfer function with proportional integral compensation:

$$-\frac{\hat{v}_{COMP}}{\hat{i}_{LED}} = \frac{14 \times g_M \times R_{CS}}{s \times (C_{COMP} + C_{HF})} \frac{(1 + s \times R_{COMP} \times C_{COMP})}{\left(1 + s \times R_{COMP} \times \left(\frac{C_{COMP} \times C_{HF}}{C_{COMP} + C_{HF}}\right)\right)}$$

The pole at the origin minimizes output steady-state error. High bandwidth is achieved with the PI compensator by placing the low-frequency zero an order of magnitude less than the crossover frequency. Use the following expressions to calculate the compensation network.
Buck with integral compensator:

$$C_{COMP} = \frac{8.75 \times 10^{-3} \times R_{CS}}{\omega_P}$$

Boost and Buck-Boost with proportional integral compensator:

$$C_{COMP} = 8.75 \times 10^{-3} \times \left(\frac{R_{CS} \times G_0}{\omega_Z}\right)$$

$$C_{HF} = \frac{C_{COMP}}{100}$$

$$R_{COMP} = \frac{1}{\omega_P \times C_{COMP}}$$

The loop response is verified by applying step input voltage transients. The goal is to minimize LED current overshoot and undershoot with a damped response. Additional tuning of the compensation network may be necessary to optimize PWM dimming performance.

11. Soft-Start

The time required for the LED current to reach the target setpoint is named the soft-start time (t_{SS}). Using a capacitor C_{SS} (from SS pin to GND) to set the required soft-start time, t_{SS}. C_{SS} can be calculated by following equation.

$$C_{SS} = 12.5 \times 10^{-6} \times t_{SS}$$

12. Overvoltage and Undervoltage Protection

The controller includes a dedicated OVP pin which can be used for output overvoltage protection. For Boost and SEPIC topologies, as shown in Figure 17 and Figure 18, the overvoltage threshold is programmed using a resistor divider, R_{OV1} and R_{OV2}, from the output voltage(V_O) to GND. In the Buck-Boost or Buck configuration, as shown in Figure 19 and Figure 20, if the LEDs are referenced to a potential other than ground, the output voltage is sensed and translated to ground by using a PNP transistor and level-shift resistors.

The overvoltage turn-off threshold, $V_{O(OV)}$, is:

Boost:

$$V_{O(OV)} = V_{OVP(THR)} \times \left(\frac{R_{OV1} + R_{OV2}}{R_{OV1}}\right)$$

Buck and Buck-Boost:

$$V_{O(OV)} = V_{OVP(THR)} \times \frac{R_{OV2}}{R_{OV1}} + 0.7$$

The overvoltage hysteresis, $V_{OV(HYS)}$ is:

$$V_{OV(HYS)} = I_{OVP(HYS)} \times R_{OV2}$$

The corresponding undervoltage fault threshold, $V_{O(UV)}$ is:

$$V_{O(UV)} = 0.1 \times \left(\frac{R_{OV1} + R_{OV2}}{R_{OV1}}\right)$$

13. Current derating calculation during overheating

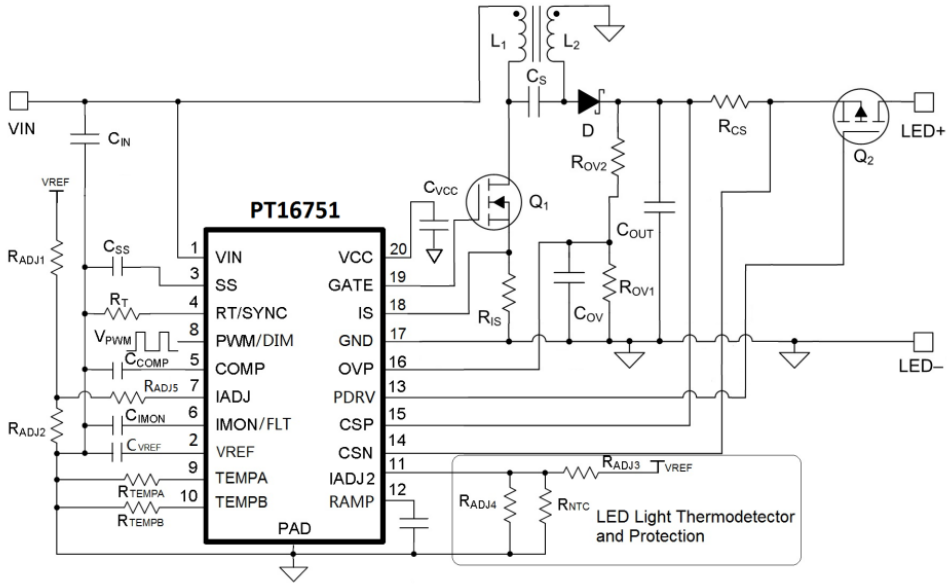


Figure 25. Typical Application Circuit

Step 1. Select the appropriate resistance R_{ADJ3} and NTC resistance. It recommends using 100K NTC resistance with B value ≈ 4100K.

Step 2. Set the temperature (T1) as the temperature corresponding to the LED current derating start. The corresponding V_{IADJ2} is 2.17V, and the NTC resistance value is R_{NTC_T1}. The resistor R_{ADJ4} can be calculated as follow:

$$R_{ADJ4} = \frac{\frac{R_{ADJ3} * 2.17}{V_{VREF} - 2.17} * R_{NTC\_T1}}{R_{NTC\_T1} - \frac{R_{ADJ3} * 2.17}{V_{VREF} - 2.17}}$$

Step 3. After the LED current is derated, if the temperature continues rising to T2 (the point OTP2 shown in Figure 12), the LED current changes to constant current. The value of NTC resistor corresponding to this temperature is R_{NTC_T2}, and the IADJ2 voltage (V_{IADJ2_T2}) corresponding to this temperature is calculated according to the voltage divider circuit (R_{ADJ3}, R_{ADJ4} and R_{NTC}).

$$V_{IADJ2\_T2} = \left(\frac{V_{VREF}}{R_{ADJ3} + \frac{R_{ADJ4} * R_{NTC\_T2}}{R_{ADJ4} + R_{NTC\_T2}}}\right) * \left(\frac{R_{ADJ4} * R_{NTC\_T2}}{R_{ADJ4} + R_{NTC\_T2}}\right)$$

Step 4. Set the constant current as I_{LED_T2}, calculates the IADJ voltage (V_{IADJ_T2}) as follow:

$$V_{IADJ\_T2} = \frac{I_{LED\_T2}}{R_{CS} * 14}$$

then, calculates the resistance of R_{TEMPA}:

$$R_{TEMPA} = \frac{1.28}{V_{IADJ\_T2}} \text{ X } 22$$

Step 5. Calculates R_{ADJ2} voltage:

$$V_{RADJ2} = \frac{V_{VREF} * R_{ADJ2} * 1000 - (V_{IADJ\_T2} - 2.17) * (-18) * R_{ADJ1} * R_{ADJ2}}{(R_{ADJ1} + R_{ADJ2}) * 1000}$$

Step 6. Calculates the resistance of R_{ADJ5}:

$$R_{ADJ5} = \frac{V_{RADJ2} - V_{IADJ\_T2}}{(V_{IADJ\_T2} - 2.17) * (-18 * 10^{-3})}$$

Step 7. If the temperature continues rising to T3 (the point OTP3 shown in Figure 12), the LED current is shutdown. The value of NTC resistor corresponding to this temperature is R_{NTC_T3}, and the IADJ2 voltage (V_{IADJ2_T3}) corresponding to this temperature is calculated according to the voltage divider circuit (R_{ADJ3}, R_{ADJ4} and R_{NTC}).

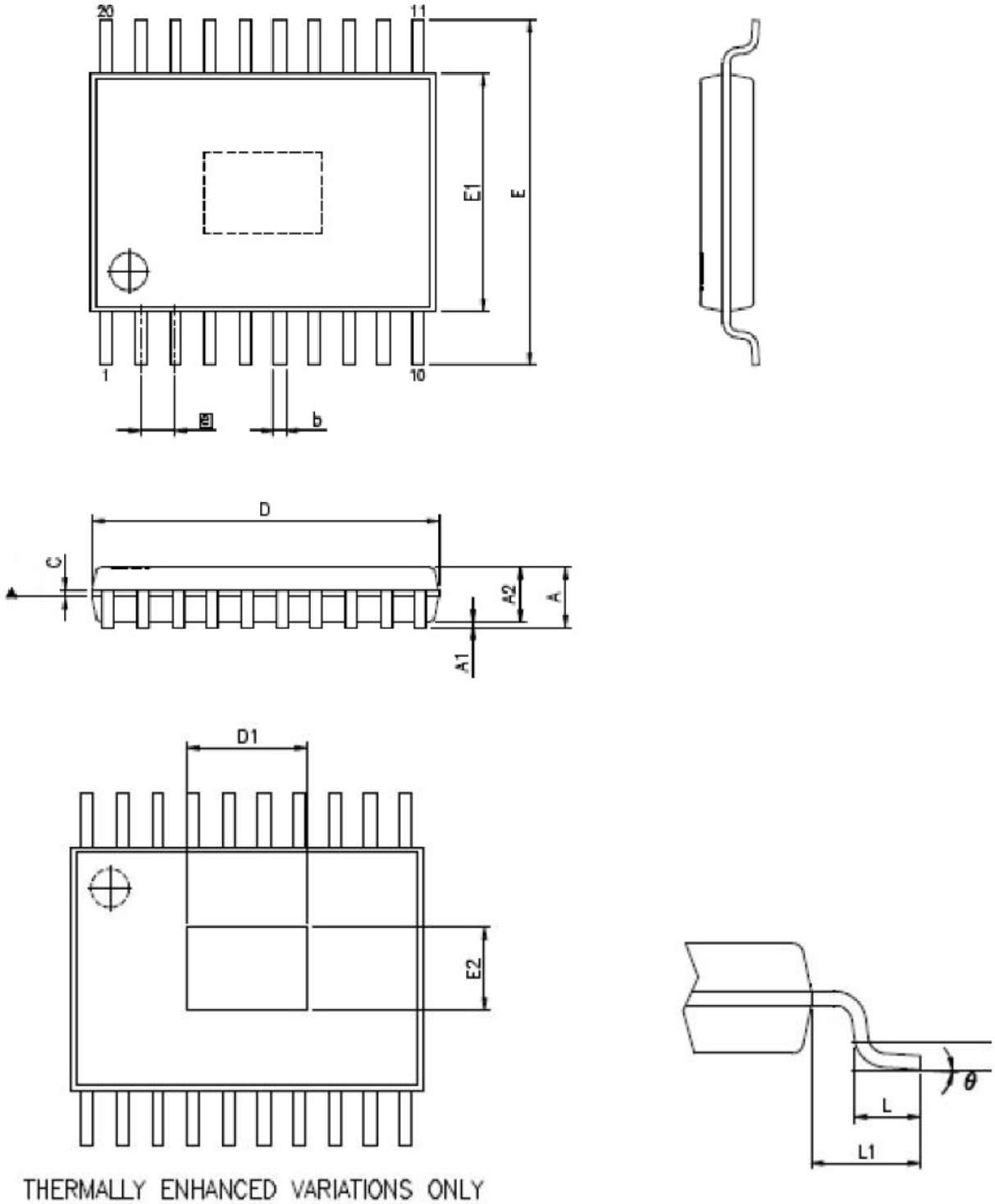
$$V_{IADJ2\_T3} = \left(\frac{V_{VREF}}{R_{ADJ3} + \frac{R_{ADJ4} * R_{NTC\_T3}}{R_{ADJ4} + R_{NTC\_T3}}}\right) * \left(\frac{R_{ADJ4} * R_{NTC\_T3}}{R_{ADJ4} + R_{NTC\_T3}}\right)$$

then, calculates the resistance of R_{TEMPB}:

$$R_{TEMPB} = \frac{1.28}{V_{IADJ\_T3}} \text{ X } 85$$

12. PACKAGE INFORMATION

20PINS, HTSSOP, 173MIL



Refer to JEDEC MO-153 ACT

Symbol	Dimensions (mm)		
	Min.	Nom.	Max..
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
b	0.19	—	0.30
c	0.09	—	0.20
e	0.65 BSC		
D	6.40	6.50	6.60
D1	2.20	—	—
E	6.40 BSC		
E1	4.30	4.40	4.50
E2	1.50	—	—
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	—	8°

13. IMPORTANT NOTICE

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