DESCRIPTION

The PT16752 is a Headlight LED controller for automotive with high accuracy peak current mode. The device implements a fixed-frequency peak current mode control technique with programmable switching frequency, slope compensation, and soft-start timing. A unique spread-spectrum modulation (SSM) can reduce emission (EMI) at the switching frequency and its harmonics.

The controller is designed to support a range of step-up or step-down driver topologies. It incorporates a high voltage (65V) rail-to-rail current sense amplifier that can directly measure LED current using a high-side series sense resistor. The amplifier is designed to achieve low input offset voltage and attain better than ±4% LED current accuracy over junction temperature range of -40°C to 140°C and output voltage range of 3V to 65V.

This LED controller can independently modulate LED current using either analog or PWM dimming techniques (PT16752 only). Linear analog dimming response with 15:1 range is obtained by varying the voltage from 286mV to 2.29V across the high impedance analog adjust (IADJ) input. PWM dimming of LED current is achieved by modulating the DIM input pin with the desired duty cycle. PDRV gate driver output can be used to enable series FET dimming functionality to get over 1000:1 contrast ratio (f_{PWM}=400Hz).

The PT16752 supports continuous LED status check through the current monitor (IMON) output. It also includes an open drain fault indicator output to indicate LED overcurrent, output overvoltage and output under-voltage conditions.

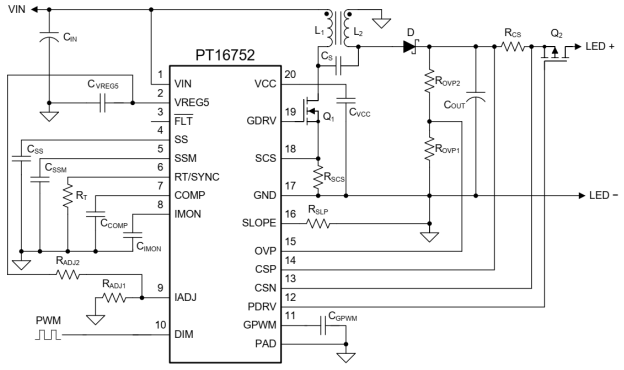
FEATURES

- Automotive AEC-Q100, Grade 1 (-40℃~+125℃) Qualified
- Input Voltage: 4.5V to 65V
- Output Voltage Range: 3V to 65V
- Low Input Offset Rail-to-Rail Current Sense Amplifier
  – Better than ±4% LED Current Accuracy over -40°C to 140°C Junction Temperature Range
  –High-Side Current Sense
- High-Impedance Analog LED Current Adjust Input (IADJ) With over 15:1 Contrast Ratio
- Integrated P-Channel MOSFET Driver for LED PWM Dimming, Compatible with Direct PWM Input with over 1000:1 Dimming Range (f_{PWM}=400Hz).
- Spread Spectrum Modulation for Improved EMI
- Continuous LED Current Monitor Output for System Fault Detection
- Programmable Switching Frequency with External Clock Synchronization Capability
- Programmable Soft-Start
- Comprehensive Fault Protection Circuitry Including VCC Under-Voltage Lockout (UVLO), Output Over-voltage Protection (OVP), Output Under-voltage Protection (UVP), Cycle-by-Cycle Switch Current Limit, Output over current protection and Thermal Protection.

APPLICATIONS

- Automotive High(Low) Beam Application
- Automotive Daytime Running Lights
- Automotive Position Lights
- LED General Lighting Applications
- Exit Signs and Emergency Lighting

TYPICAL APPLICATION

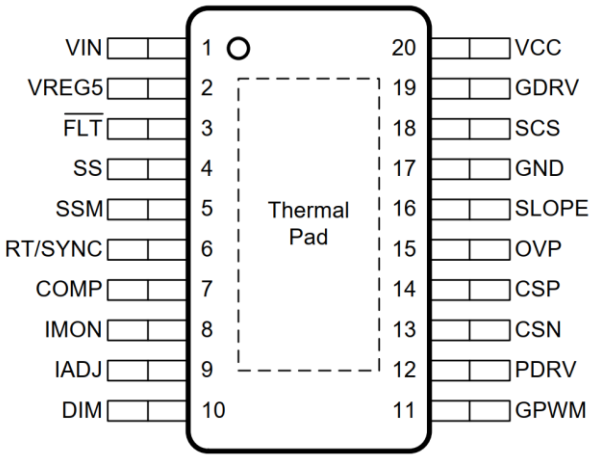


1. ORDER INFORMATION

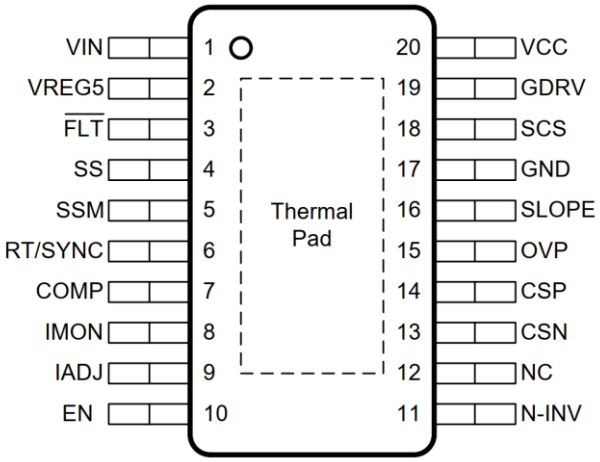
Part Number	Package	Top Code	PWM Dimming
PT16752	20-Pin, HTSSOP	PT16752	Yes
PT16752-HT	20-Pin, HTSSOP	PT16752-HT	No

2. PIN CONFIGURATION

PT16752—HTSSOP20



PT16752-HT—HTSSOP20



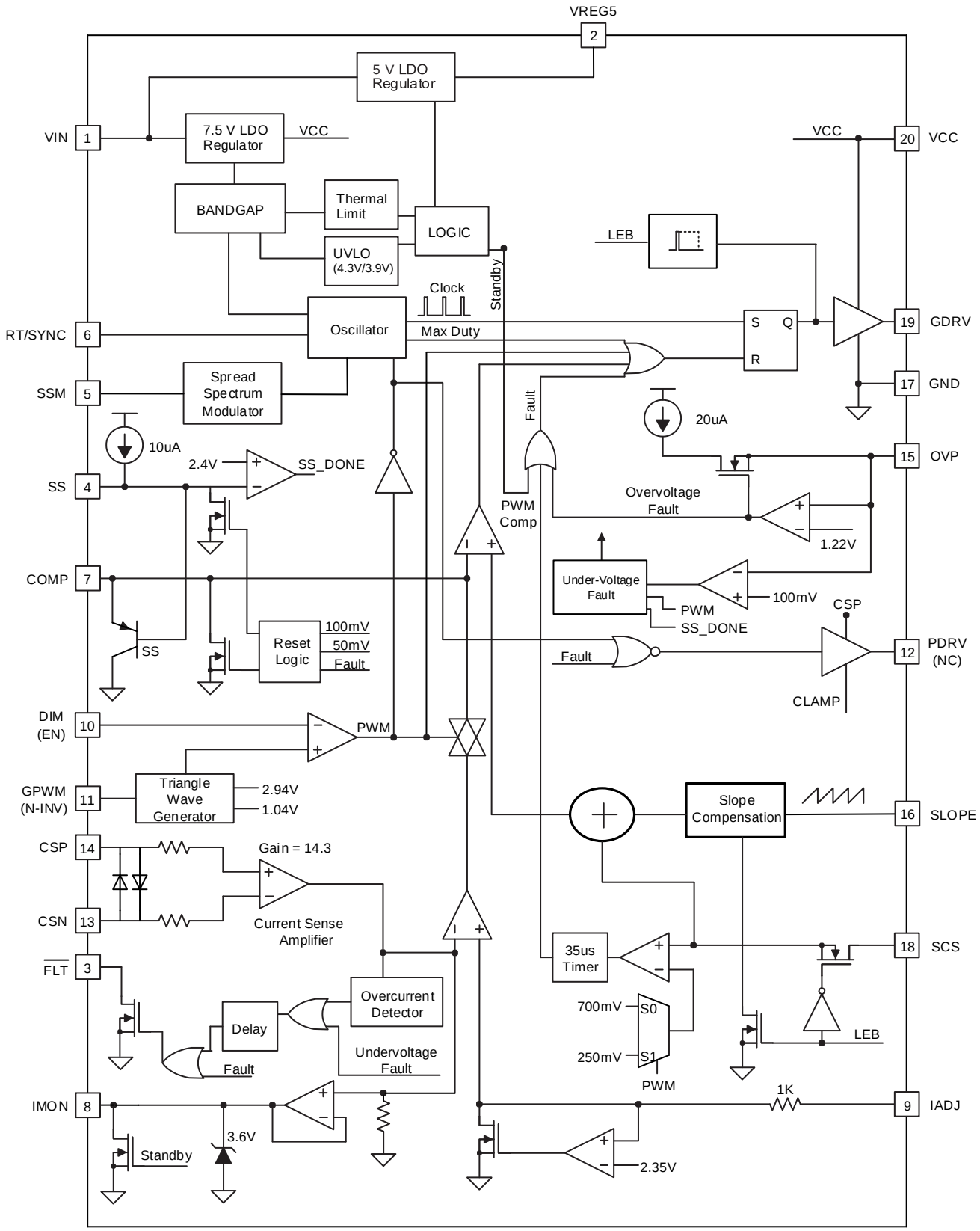
3. PIN DESCRIPTION

PIN Name	I/O	Description	PIN NO.
VIN	--	Supply voltage input. Bypass with a low-pass filter using a series 10Ω resistor and 100nF capacitor connected to GND. Locate the capacitor close to the VIN pin.	1
VREG5	--	Support 5V reference voltage. Locally decouple to GND using a ceramic capacitor (with a value between 2.2μF and 4.7μF) located close to the VREG5 pin.	2
/FLT	O	Open-drain fault indicator. Connect to VREG5 with a resistor to create active **low** fault signal output. Internal LED short circuit protection and auto-restart timer can enabled by directly connecting the pin to SS input.	3
SS	I/O	Programmable soft-start pin. Connect a capacitor to GND to set the start-up time. Short this pin to GND to disable the switching.	4
SSM	I/O	Spread spectrum modulation frequency programming pin. Connect a capacitor to GND to set the spread spectrum modulating frequency. Short this pin to GND to disable spread spectrum modulation function.	5
RT/SYNC	I/O	Programmable oscillator frequency pin. Connect a resistor to GND to set the switching frequency. Connect a 100pF capacitor series to this pin to synchronize the internal oscillator from an external clock pulse.	6
COMP	I/O	Error amplifier compensation. Connect compensation network to achieve desired closed loop response.	7
IMON	O	LED current report pin. The LED current sensed by CSP/CSN input is reported as $14.3 \times I_{LED} \times R_{CS}$. Bypass with a 1nF ceramic capacitor to GND.	8

PIN DESCRIPTION (continued)

PIN Name	I/O	Description	PIN NO.
IADJ	I	Reference voltage input for LED current. To implement analog dimming, source external voltage from 286mV to 2.29V to this pin, and the current sense voltage: $V_{(CSP-CSN)} = V_{IADJ}/14.3$. If IADJ input voltage is higher than internal clamp voltage, the reference voltage would be clamped to 2.4V(typ.). This internal clamp voltage is not recommended to use as a reference voltage.	9
DIM/EN	I	LED dimming input. Supports analog or direct PWM signal input. A direct PWM dimming signal can be applied to control the LED current duty cycle and frequency when the PWM generator disabled. The analog or PWM command is used to generate an internal PWM signal that controls the GDRV and PDRV outputs. Setting the internal PWM signal to logic level low, turns off switching, idles the oscillator, disconnects the COMP pin, and sets PDRV to V_{CSP}. Connect to VREG5 when not used for PWM dimming. The analog dimming signal (1.04~2.94V) is compared to the internal PWM generator triangle waveform to set LED current duty cycle between 0% and 100%. Globe enable input (PT16752-HT only), setting input signal to logic-high, turns on the PDRV and GDRV drivers. The logic-high level threshold is set by N-INV pin.	10
GPWM/ N-INV	I/O	Internal PWM generator input. Connect a capacitor to GND to set the triangle wave frequency. Connect a 250kΩ resistor to GND to disable the PWM generator and to set a fixed reference for direct external PWM dimming input or enable input (PT16752-HT only). Do not allow this pin to float.	11
PDRV/NC	O	Series dimming P-channel FET gate driver output. Connect to gate of external P-channel MOSFET to implement series PWM dimming. This pin is not connected for PT16752-HT.	12
CSN	I	Current sense amplifier negative input (–). Connect directly to the negative node of LED current sense resistor R_{CS}.	13
CSP	I	Current sense amplifier positive input (+). Connect directly to the positive node of LED current sense resistor R_{CS}.	14
OVP	I	Overvoltage protection input. Connect resistor divider from output to GND to set overvoltage protection threshold and hysteresis.	15
SLOPE	I/O	Slope compensation input. Connect a resistor to GND to set the desired slope compensation.	16
GND	--	Analog and Power ground connection pin. Connect to circuit ground to complete return path.	17
SCS	I	Switching current sense pin. Connected to switching current sense resistor, R_{SCS}, to monitor the peak current of the main MOSFET.	18
GDRV	O	Gate driver output for switching MOSFET. Connect to gate of the main MOSFET.	19
VCC	--	VCC bias supply pin. Using a 2.2μF to 4.7μF ceramic capacitor located close to the controller.	20
Thermal PAD	--	The GND pin must be connected to the exposed thermal pad for proper operation. This PAD must be connected to PCB ground plane using multiple vias for good thermal performance.	Thermal PAD

4. FUNCTIONAL BLOCK DIAGRAM



5. FUNCTION DESCRIPTION

5.1 OVERVIEW

The PT16752 is a wide input range (4.5V to 65V) LED driver controller. It has all of the functions necessary to implement a compact and highly efficient LED driver, supports step-up or step-down converter topologies. The devices implement a fixed-frequency, peak current mode control technique to achieve constant output current and fast transient response. It incorporates a low input offset, rail-to-rail current sense amplifier that supports a wide range of output voltages (3V to 65 V) and is capable of powering the LED string consisting of 1 to 20 LEDs while maintaining better than 4% current accuracy over the operating temperature range.

The LED current sense threshold, set by the analog adjust input, IADJ, provides the capability to analog (amplitude) dim over a linear range of 15:1 by varying the voltage, V_{IADJ}, from 286mV to 2.29V. The IADJ input provides the means to externally program LED current and facilitates calibration, brightness correction of the LEDs. High resolution and linear dimming response is achieved by varying the duty cycle of LED current based on the DIM input (PT16752 only). The PWM duty cycle can be varied from 0% to 100% by modulating the analog voltage on DIM input from 1.04V to 2.94V. The PWM dimming frequency is externally programmable and is set by the capacitor connected to GPWM input. PT16752 can also be configured to implement direct PWM dimming based on the duty cycle of external PWM signal by connecting a 250kΩ resistor across GPWM pin and GND. The input PWM signal directly controls the GDRV and PDRV drive outputs, controls the internal oscillator, and enables high-speed PWM dimming with over 1000:1 contrast ratio when using an external MOSFET placed in series with the LED load.

The PT16752 provides the instantaneous status of LED current report by the current monitor output, IMON. This feature indicates instantaneous current as a result of LED short circuit and cable harness failure. An open-drain fault indicator (/FLT) is also provided to report faults including cycle-by-cycle current limit, output overvoltage, and output undervoltage conditions. LED driver protection with auto-restart (hiccup) mode is enabled by connecting the fault pin (/FLT) to the SS pin. Other protection features include VCC undervoltage protection and thermal shutdown. A remote signal can force the device in to shutdown by pulling down on the SS pin

5.2 VREG5 AND VCC SUPPLY

The PT16752 incorporates a high voltage regulator (65V), generates 5V reference voltage, 7.5V VCC bias supply, and other internal reference voltages. The VREG5 voltage is internally used to generate voltage thresholds for the PWM generator circuit and to power some digital circuits. The VREG5 voltage can be used to set voltage levels for either the IADJ pin or DIM pin to set LED current or PWM dimming duty cycle. Also it can be used to bias external circuitry requiring a reference supply. Place a bypass capacitor in the range of 2.2μF to 4.7μF across the VREG5 output to GND to ensure proper operation.

The VCC pin is monitored to implement UVLO protection. The controller is enabled when the VCC voltage exceeds 4.3V threshold and is disabled when the voltage drops below 3.9V threshold. The UVLO comparator provides 0.4V hysteresis to avoid chatter during transitions. The UVLO thresholds are fixed internally and cannot be adjusted. The VCC supply powers the internal circuitry, GDRV driver and PDRV driver. Place a bypass capacitor in the range of 2.2μF to 4.7μF across the VCC output and GND to ensure proper operation. The regulator operates in dropout when input voltage VIN falls below 7.5V forcing VCC to be lower than VIN by 300mV for a 20mA supply current. The VCC is a regulated output of the internal regulator and cannot be driven from an external power supply.

5.3 OSCILLATOR

The switching frequency of PT16752 can be programmed by a single external resistor connected between the RT/SYNC pin and the GND pin. To set a desired frequency, f_{SW} (Hz), the resistor value can be calculated using:

$$R_T = \frac{1.432 \times 10^{10}}{(f_{sw})^{1.047}} \ (\Omega) \qquad (1)$$

Figure 1 shows a graph of switching frequency versus resistance R_T. It recommends a switching frequency setting between 80kHz and 700kHz for optimal performance over input and output voltage operating range and for best efficiency. Operation at higher switching frequencies requires careful selection of N-channel MOSFET characteristics as well as detailed analysis of switching losses.

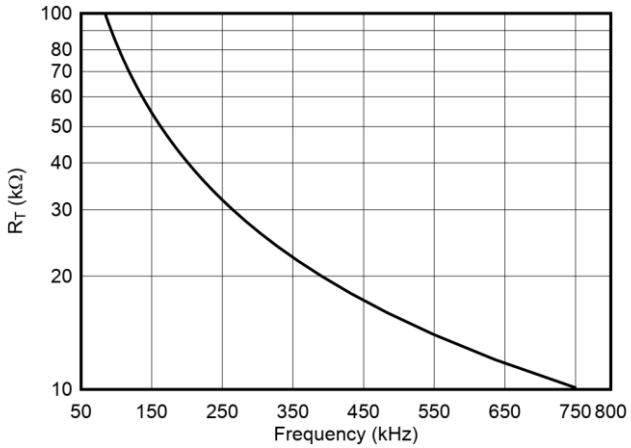


Figure 1. Timing Resistance (R_T) VS Switching Frequency

The internal oscillator can be synchronized by AC-coupled external clock pulse to RT/SYNC pin, shown as in Figure 2. The positive going synchronization clock at the RT/SYNC pin must exceed the RT/SYNC threshold, and the negative going synchronization clock at the RT/SYNC pin must exceed the RT/SYNC falling threshold so that the internal synchronization pulse detector can be tripped.

It recommends that the frequency of the external synchronization pulse is within ±20% of the internal oscillator frequency programmed by the R_T resistor. A minimum coupling capacitor of 100pF and typical pulse width of 100ns for proper synchronization are recommended. In the case where external synchronization clock is lost the internal oscillator takes control of the switching rate based on the R_T resistor to maintain output current regulation. The R_T resistor is always required whether the oscillator is free running or externally synchronized.

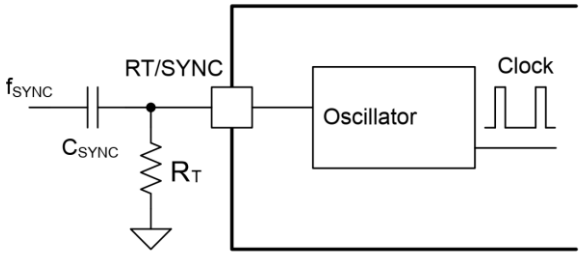


Figure 2. Oscillator Synchronization Configuration

5.4 SOFT-START

The PT16752 has soft-start function to help the regulator reach the steady-state operating point gradually, thus reducing startup stresses and surges. The COMP pin is clamped to the SS pin, separated by a diode, until LED current nears the regulation threshold. The voltage of SS pin increase gradually due to the internal 10μA soft-start current source on an external soft-start capacitor C_{SS}. This results in a gradual rise of the COMP voltage from GND. When VCC exceeds the UVLO threshold, the internal 10μA current source turns on. At the beginning of the soft-start sequence, the SS pull down switch is active and is released when the voltage V_{SS} drops below 50mV. The SS pin can also be pulled down by an external switch to stop switching. When the SS pin is externally driven to enable switching, the slew-rate on the COMP pin should be controlled by choosing a compensation capacitor that avoids large startup transients. The value of C_{SS} should be large enough to charge the output capacitor during the soft-start transition period.

The soft-start time (t_{SS}) is defined as the period between power on and LED current reaches rated value. It is programmed using a capacitor, C_{SS}, from SS pin to GND. C_{SS} can be calculated as Equation 2:

$$C_{SS} = 9 \times 10^{-6} \times t_{SS}\ (\mu F) \quad (2)$$

t_{SS}: s

5.5 SPREAD SPECTRUM MODULATION

The PT16752 provides a frequency dithering option that is enabled by connecting a capacitor from the SSM pin to GND. A triangle waveform centered at 1V is generated across the C_{SSM} capacitor. The triangle waveform modulates the oscillator frequency by ± 15% of the nominal frequency generated by internal oscillator. The C_{SSM} capacitance value sets the rate of the low frequency modulation.

To achieve maximum attenuation in average EMI scan set modulation frequency ranging from 100Hz to 1.2kHz. The low modulating frequency has little impact on the quasi-peak EMI scan. Set the modulation frequency to 10kHz or higher to achieve attenuation for quasi-peak EMI measurements. The modulation frequency higher than the receiver resolution bandwidth (RBW) of 9kHz only impacts the quasi-peak EMI scan and has little impact on the average measurement. The device simplifies EMI compliance by providing the means to tune the modulation frequency based on measured EMI signature. Equation 3 calculates the C_{SSM} capacitance required to set the modulation frequency.

$$C_{SSM} = \frac{10uA}{2 \times f_{MOD} \times 0.3V}\ (F) \quad (3)$$

f_{MOD}(Hz): Modulation Frequency.

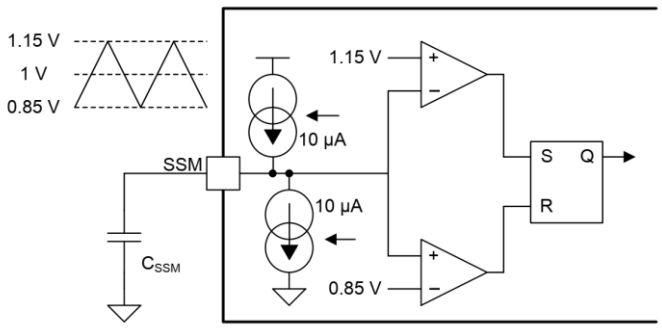


Figure 3. Spread Spectrum Modulation

Connect the SSM pin to GND to disable frequency dither circuit operation. Internal frequency dithering is not supported when the devices are synchronized based on an external clock signal.

5.6 TRANSCONDUCTANCE ERROR AMPLIFIER

The internal transconductance amplifier generates an error signal proportional to the difference between the LED current sense feedback voltage and the external IADJ input voltage. Closed-loop regulation is achieved by connecting a compensation network to the output of the error amplifier. In most LED driver applications, a simple integral compensator consists of a capacitor across the COMP output and ground, to obtain a stable response. It recommends a capacitor value between 10nF and 100nF as a good starting point. Higher closed-loop bandwidth can be achieved by implementing a proportional-integral compensator consisting of a series resistor and a capacitor network connected across the COMP output and ground. Based on the converter topology, the compensation network should be tuned to achieve a minimum of 60° of phase margin and 10dB of gain margin.

5.7 CURRENT MONITOR OUTPUT

The IMON pin voltage represents the LED current measured by the rail-to-rail current sense amplifier across the external current shunt resistor. The linear relationship between the IMON voltage and LED current includes the amplifier gain-factor of 14.3 (Figure 4). The IMON output can be connected to an external microcontroller or comparator to facilitate LED open, short, or cable harness fault detection and mitigation based on programmable threshold V_{OCTH}. The IMON voltage is internally clamped to 3.6V.

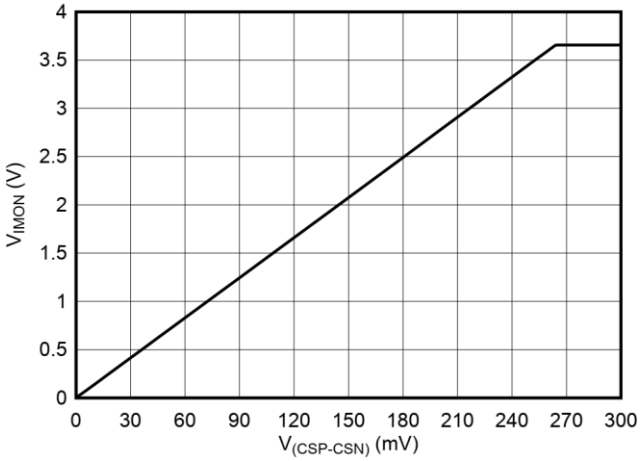


Figure 4. V_{IMON} vs $V_{(CSP-CSN)}$

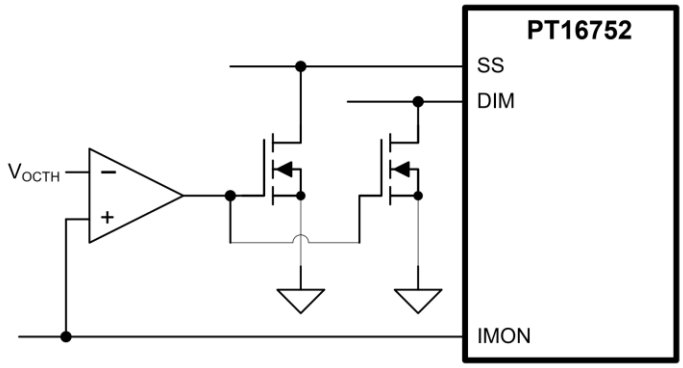


Figure 5. LED Overcurrent Protection using IMON Output

5.8 ANALOG ADJUST INPUT

The voltage of LED current sense resistor V_{CSP}–V_{CSN}, is regulated to the analog adjust input voltage V_{IADJ}, scaled by the current sense amplifier voltage gain of 14.3. Using a resistor divider from VREG5 or a voltage source, the LED current can be linearly adjusted by varying the voltage on IADJ pin from 286mV to 2.29V. The IADJ pin can be connected to VREG5 through an external resistor to set LED current based on the 2.35V internal reference voltage. This device offers different methods to set the IADJ voltage. Figure 7 shows how the IADJ input can be used in conjunction with a NTC resistor to achieve the thermal protection. A PWM signal in conjunction with first- or second-order low-pass filter can be used to program the IADJ voltage as shown in Figure 8.

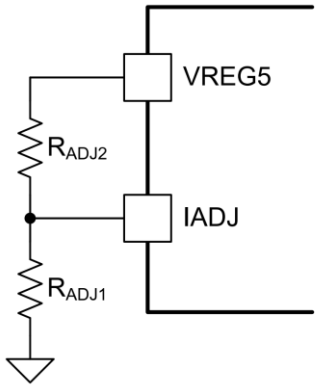


Figure 6. Setting Resistor Divider From VREG5

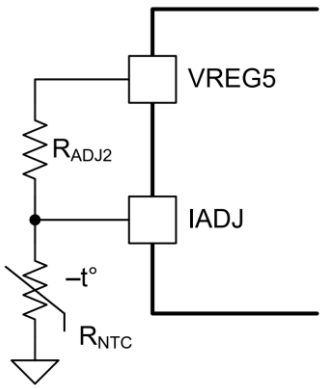


Figure 7. Thermal Fold-back Circuit Using External NTC Resistor

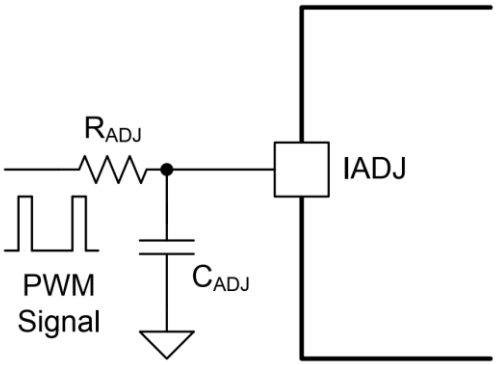


Figure 8. Analog Dimming Achieved By Low-pass Filtering External PWM Signal

5.9 DIM(EN) INPUT

The PT16752 device incorporates a PWM generator circuit to translate analog voltage to PWM duty cycle. Connecting a capacitor from GPWM pin to GND to set the dimming frequency. The dimming frequency, f_{DIM}, can be calculated as Equation 4:

$$f_{DIM} = \frac{10uA}{2\ x\ 2V\ x\ C_{DIm}}\ (Hz) \quad (4)$$

The internal PWM signal can be varied from 0% to 100% by setting the DIM pin voltage between 1.04V and 2.94V. Equation 5 describes the relationship between DIM pin voltage, V_{DIM} and internal PWM duty cycle, D_{PWM}.

$$D_{PWM} = \frac{V_{DIM} - 1.04}{1.9} \quad (5)$$

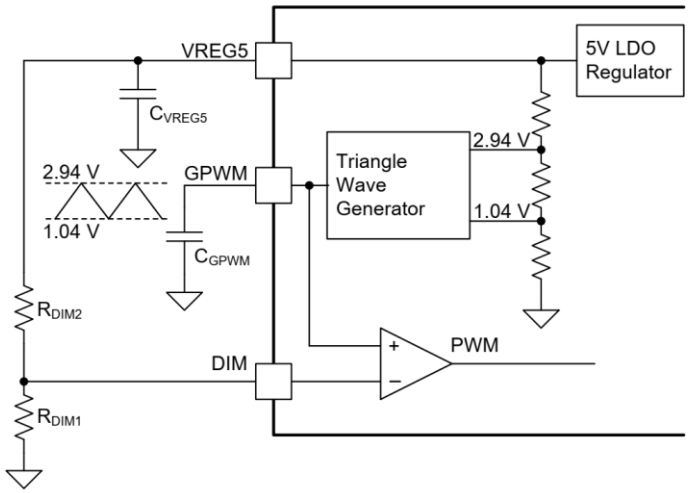


Figure 9. PWM Dimming Using Internal PWM Generator

Shown as Figure 10, the LED current also can be modulated by the external PWM input, because the device can be configured to be compatible with external PWM signal, $V_{PWM(EXT)}$. When use the external PWM signal directly, it is need to connect a 250kΩ (typ.) resistor from GPWM pin to GND to disable the internal triangle wave generator. In this case, the internal comparator threshold is set to 2.5V and the internal PWM duty cycle, D_{PWM}, is controlled by the external PWM command. The GPWM pin cannot be left floating.

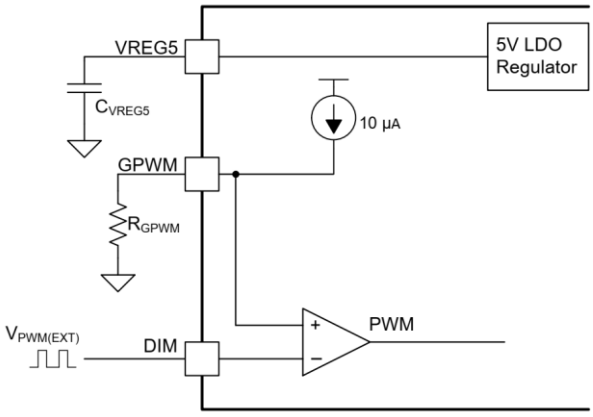


Figure 10. Direct PWM dimming

The GDRV and PDRV output are controlled by the internal PWM signal. Forcing the internal PWM signal in a logic low state turns off switching, parks the oscillator, disconnects the COMP pin, and sets the PDRV output to V_{CSP} in order to maintain the charge on the compensation network and output capacitors. On the rising edge of the PWM voltage (V_{PWM} set to logic level high), the GDRV and PDRV outputs are enabled to ramp the inductor current to the previous steady-state value. The COMP pin is connected and the error amplifier and oscillator are enabled only when the switch current sense voltage V_{SCS} exceeds the COMP voltage, thus immediately forcing the converter into steady-state operation with minimum LED current overshoot. Connects the DIM pin to the VCC pin or VREG5 pin when dimming

function is not required. An internal pull-down resistor sets the input to logic-low and disables the device when the pin is disconnected or left floating.

PT16752-HT includes an enable input(EN). Setting input signal to logic-high, turns on the PDRV and GDRV drivers; Setting input signal to logic-low, turns off switching, idles the oscillator, disconnects the COMP pin. Connect to VREG5 when not used for enable function. An internal pull-down resistor sets the input to logic-low and disables the device when the pin is disconnected or left floating
Connects a 250kΩ (typ.) resistor from N-INV pin to GND to set the enable function threshold by internal 10uA current source generating the comparator threshold. In this case, the internal comparator threshold is set to 2.5V. The N-INV pin cannot be left floating.

5.10 RAIL-TO-RAIL CURRENT SENSE AMPLIFIER

The PT16752 incorporates a high voltage rail-to-rail current sense amplifier to measure the average current of LED string based on the differential voltage drop between the CSP and CSN inputs over a common mode range of 3V to 65V. The differential voltage, V_{CSP}-V_{CSN} is amplified by a voltage-gain factor of 14.3, and connected to the negative input of the transconductance error amplifier. Accurate LED current feedback is achieved by limiting the cumulative input offset voltage, (represented by the sum of the voltage-gain error, the intrinsic current sense offset voltage, and the transconductance error amplifier offset voltage) to less than 5mV over the recommended common-mode voltage, and temperature range.
Figure 11 shows a recommended common-mode or differential mode low-pass filter circuit, which can be used to eliminate the effects of large output current ripple and switching current spikes caused by diode reverse recovery. PT16752 recommends that the filter resistance should be between 10Ω and 100Ω to limit the additional offset caused by amplifier bias current and achieve best accuracy and line regulation.

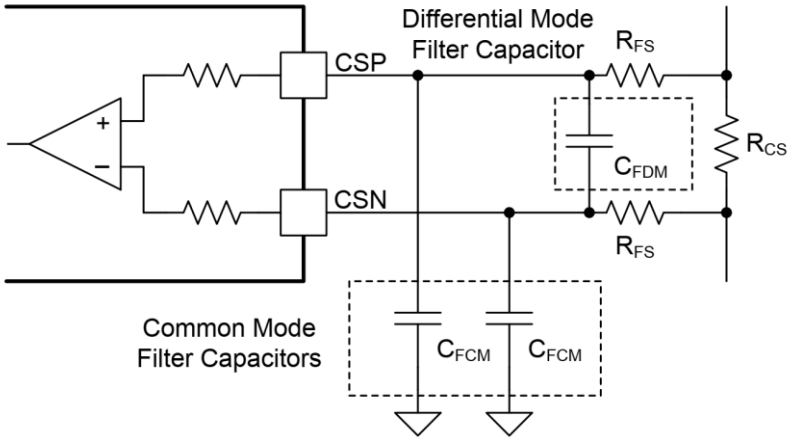


Figure 11. Current Sense Amplifier Input Filter Options

5.11 OUTPUT OVERVOLTAGE AND SHORT-CIRCUIT PROTECTION

The PT16752 includes a dedicated OVP pin which can be used for either input or output overvoltage protection. This pin features a precision 1.22V threshold with 20μA of hysteresis current. The overvoltage threshold limit is set by a resistor divider network from the output terminal to GND. When the OVP pin voltage exceeds the reference threshold, the GDRV pin is immediately pulled low, the PDRV output is disabled, and the SS and COMP capacitors are discharged. The GDRV and PDRV outputs are enabled and a new startup sequence is initiated after the voltage drops below the hysteresis threshold set by the 20μA source current and the external resistor divider.
The overvoltage fault threshold is calculated by equation 6:

$$V_{OV} = 1.22 \times \left(1 + \frac{R_{OV2}}{R_{OV1}}\right) \quad (6)$$

The OVP pin also indicates a short-circuit condition when the voltage across the OVP pin and GND falls below 100 mV. In this case, the output voltage, V_O, is below the undervoltage fault threshold determined based on the resistor divider connected to the OVP pin. The undervoltage fault threshold can be calculated by equation 7:

$$V_{O(UV)} = 0.1 \times (1 + \frac{R_{OV2}}{R_{OV1}}) \quad (7)$$

5.12 SLOPE COMPENSATION

Peak current mode based regulators are subject to sub-harmonic oscillations for duty cycle greater than 50%. To avoid this instability problem, the control scheme is modified by the addition of an artificial ramp to the sensed switch current waveform. The slope of the artificial ramp required is dependent on the input voltage (V_{IN}), output voltage (V_O), inductor (L), and switch current sense resistor (R_{SCS}). The device incorporates an adaptive slope compensation technique that modifies the slope of the artificial ramp generated based on the input voltage and output voltage measured at CSP pin (V_{CSP}), thus greatly simplifying the design for common LED driver topologies, such as boost, buck-boost, and boost-to-battery. The magnitude of the internal ramp signal can be calculated equation 8:

$$R_{SL} = 216 \times 10^6 \times \frac{L}{R_{SCS}} (\Omega) \quad (8)$$

L: μH

The resistor, R_{SLOPE} provides the flexibility to set the slope of the internal artificial ramp based on the inductance (L) and the LED driver topology. The SLOPE pin cannot be left floating.

5.13 SWITCH CURRENT SENSE

The SCS pin monitors the main MOSFET current to implement peak current mode control. The GDRV output duty cycle is derived by comparing the peak switch current, measured by the R_{SCS} resistor, to the internal COMP voltage threshold. An internal slope signal, V_{SL}, generated by slope compensation circuit is added to the measured sense voltage, V_{SCS}, to prevent sub-harmonic oscillations for duty cycles greater than 50%. An internal blanking circuit prevents MOSFET switching current spike propagation and premature termination of duty cycle by internally shunting the SCS input for 150ns after the beginning of the new switching period. For additional noise suppression connect an external low-pass RC filter with resistor values ranging from 100Ω to 500Ω and a 1000pF capacitor. The external RC filter ensures proper operation when operating in the dropout region (VIN less than 7V).

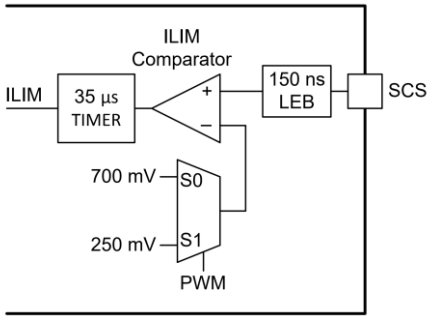


Figure 12. Switch Current Limit Circuit

Cycle-by-cycle current limit is accomplished by a redundant internal comparator. The current limit threshold is set based on the status of internal PWM signal. The current limit threshold is set to 250mV (typ) when PWM signal is high and to 700mV (typ) when PWM signal is low. The transition between the two thresholds work in conjunction with slope compensation and the error amplifier circuit to allow for higher inductor current immediately after the PWM transition and to improve LED current transient response during PWM dimming.

The device immediately terminates the GDRV and PDRV output when the SCS input voltage, V_{SCS}, exceeds the threshold value. Upon a current limit event, the SS and COMP pin are internally grounded to reset the state of the controller. The GDRV output is enabled after the expiration of the 35μs internal fault timer and a new start-up sequence is initiated through the SS pin. Equation 9 calculates the peak inductor current in the current limit.

$$I_{L(PK)} = \frac{250mV}{R_{SCS}} (A) \quad (9)$$

5.14 GATE DRIVER

The PT16752 contains a N-channel gate driver that switches the output V_{GDRV} between VCC and GND. A peak source and sink current of 500mA allows controlled slew-rate of the MOSFET gate and drain node voltages, limiting the conducted and radiated EMI generated by switching.

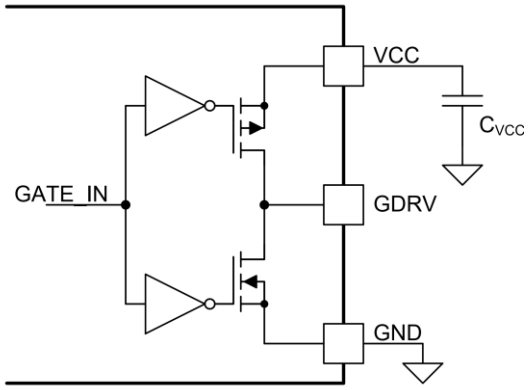


Figure 13. N-Channel Gate Driver Circuit

The gate driver supply current I_{GDRV} depends on the total gate drive charge (Q_G) of the MOSFET and the operating frequency of the converter, f_{SW}, $I_{GDRV} = Q_G \times f_{SW}$. Choose a MOSFET with a low gate charge specification to limit the junction temperature rise and switch transition losses.
It is important to consider the MOSFET threshold voltage when operating in the dropout region when the input voltage is below the VCC regulation level. It recommends a logic level device with a threshold voltage below 5V when the device is required to operate at an input voltage less than 7V.

5.15 FAULT INDICATOR

The PT16752 includes a fault indicator (/FLT) pin with an open-drain output to indicate fault conditions. The /FLT pin goes **LOW** under the following conditions:

- **Overvoltage across the LED string** (V_{OVP}> 1.22V): *GDRV and PDRV outputs are disabled, SS and COMP capacitors are discharged. A soft-start sequence is initiated once the output voltage drops below the hysteresis threshold set by the 20μA current source.*
- **Under voltage across the LED string** (V_{OVP} < 100mV): *The /FLT pin is forced to LOW state, and is released after timer expires (36ms). Device continues to operate while in this condition.*
- **Overcurrent across the LED string** (14.3 × $V_{(CSP-CSN)}$ > 1.5 × V_{IADJ}): *The /FLT pin is forced to LOW state when the LED current exceeds 1.5 times the regulation set point. The /FLT pin is released after timer expires (36ms). Device continues to operate while in this condition.*
- **LED string light load** (PT16752-HT only) (14.3 × $V_{(CSP-CSN)}$ < 0.5 × V_{IADJ}): *The /FLT pin is forced to LOW state when the LED current less than 0.5 times the regulation set point. The /FLT pin is released after timer expires (36ms). Device continues to operate while in this condition.*
- **Cycle-by-cycle switch current limit condition** (V_{SCS} > 250mV): *Cycle-by-cycle current limit is activated when the SCS pin voltage exceeds 250mV. The GDRV and PDRV outputs are disabled, the SS and COMP pin capacitors are discharged and /FLT pin is forced to LOW state. An internal 35μs timer is activated. Soft-start sequence is initiated after expiration of the 35μs timer period.*

The /FLT pin goes high when the fault conditions ends or when the internal 36ms timer expires. But under the following fault conditions, the /FLT pin remains in high-impedance states.

- **Input undervoltage** (UVLO) (V_{CC}< 3.9V): *The device enters the standby state when the VCC voltage falls below the UVLO threshold. In standby state, GDRV and PDRV outputs are disabled, the SS and COMP capacitors are discharged. /FLT pin remains in high-impedance state.*
- **VREG5 pin short to ground** (VREG5< 2V): *The device enters standby state when the* VREG5 *pin is shorted to ground. In the standby state, GDRV and PDRV outputs are disabled and the SS and COMP capacitors are discharged. The /FLT pin will remain in a high-impedance state.*
- **COMP pin short to ground** (V_{COMP}< 1.6V): *Switching is disabled when COMP voltage falls below 1.6V. The /FLT pin remains in a high-impedance state.*

5.16 HICCUP MODE SHORT-CIRCUIT PROTECTION

Connecting the /FLT pin to the SS pin enables hiccup mode operation under output short-circuit conditions.

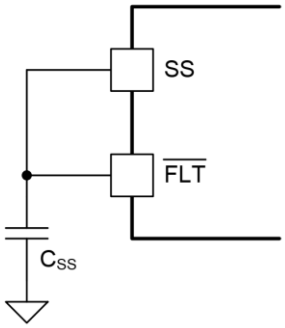


Figure 14. Hiccup Mode Short-Circuit Protection

On detection of output short-circuit fault, the /FLT pin forces the SS pin to GND (VSS < 50mV) and disables GDRV and PDRV outputs for 36ms. After the timer expires, the /FLT pin is released and a new soft start sequence is initiated. Under sustained fault conditions the device operates in hiccup mode, attempting to recover after every 36ms period.

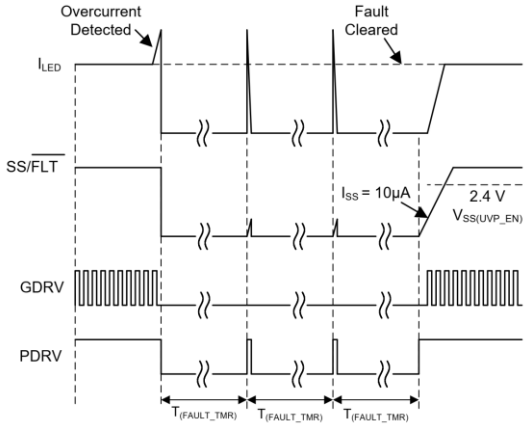


Figure 15. Output Overcurrent Fault Protection

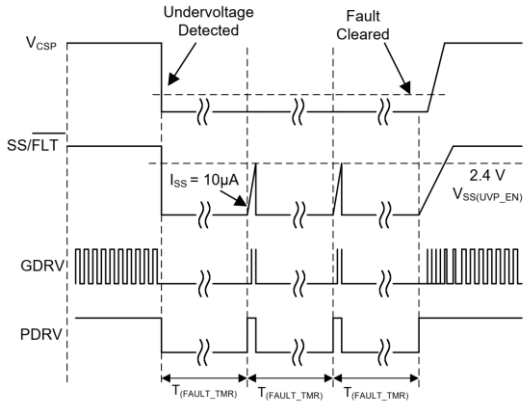


Figure 16. Output Undervoltage Fault Protection

5.17 FAULT INDICATION MODE

The /FLT pin output can be setup to indicate fault status to a microcontroller and aid in fault diagnostics and protection. In case of a fault, the /FLT pin is forced low when biased through an external resistor connected either to reference voltage output, VREG5, or an external bias supply. When connected to VREG5, the /FLT pin is driven low when the device enters standby mode during UVLO, thermal shutdown, or VREG5 short-circuit conditions.

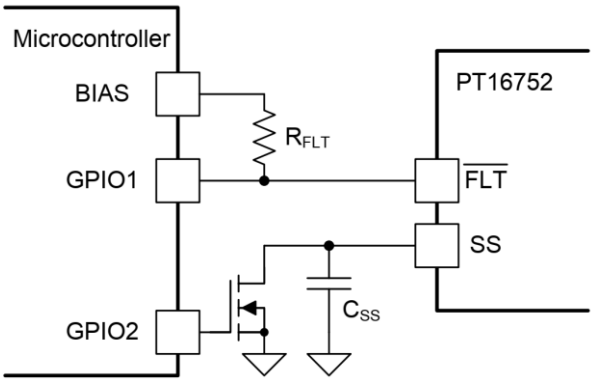


Figure 17. /FLT Pin Interface connects BIAS output

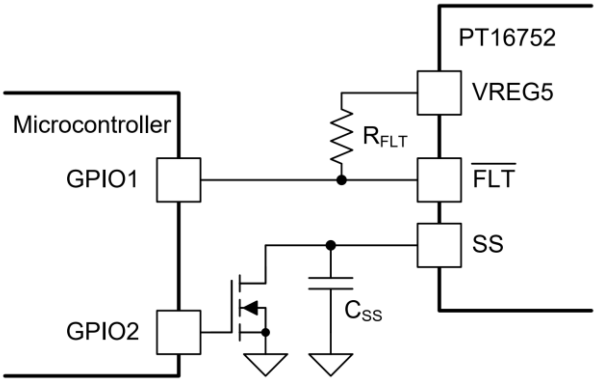


Figure 18. /FLT Pin Interface connects VREG5 output

5.18 THERMAL PROTECTION

Internal thermal shutdown circuitry is implemented to protect the controller in the event the maximum junction temperature is exceeded. When activated, typically at 175°C, the controller is forced into a shutdown mode, disabling the internal regulator. This feature is designed to prevent overheating and damage to the device.
A startup sequence is initiated when the junction temperature falls below 155˚C. The /FLT pin remains in a high-impedance state when the thermal protection occurs.

6. ABSOLUTE MAXIMUM RATINGS

		MIN	MAX	UNIT
Input voltage	VIN, CSP, CSN	-0.3	65	V
	DIM(EN)	-0.3	14	V
	SCS, RT/SYNC, /FLT	-0.3	8.8	V
	SS, SSM,GPWM(N-INV), OVP, SLOPE, IADJ, VREG5	-0.3	5.5	V
	CSP to CSN	-0.3	0.3	V
Output voltage	VCC, GDRV	-0.3	8.8	V
	IMON	-0.3	5.5	V
	COMP	-0.3	5.0	V
Source current	IMON	--	100	µA
	GDRV (pulsed < 20ns)	--	500	mA
Sink current	GDRV (pulsed < 20ns)	--	500	mA
Operating junction temperature, T_J		-40	150	°C
Storage temperature, T_{stg}			165	°C

7. ESD RATINGS

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM)		±2000	V
		Charged-device model (CDM)	All pins except 2, 17	±1000	
			Pins 2, 17	±500	

8. RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VIN	Supply input voltage	6.5	14	60	V
V_{CSP}, V_{CSN}	Current sense common mode	6.5		60	V
$f$sw	Switching frequency	80		700	kHz
f_{SSM}	Spread spectrum modulation frequency	0.1		12	kHz
V_{IADJ}	Current reference voltage	0.286		2.29	V
T_A	Operating ambient temperature	-40		125	°C

9. THERMAL INFORMATION

THERMAL METRIC			UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	41.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.6	°C/W

10. ELECTRICAL CHARACTERISTICS

$-40°C \le T_J \le 140°C$, V_{IN} = 14V, V_{IADJ} = 2.1V, V_{GPWM} = 2.5V, V_{DIM} = 5V, V_{OVP} = 500mV, C_{VCC} = 1µF, C_{VREG5} = 1µF, C_{COMP} = 2.2 nF, R_{CS} = 100 mΩ, R_T = 20 kΩ, no load on GDRV and PDRV (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE (VIN)						
$I_{IN(STBY)}$	Input stand-by current	V_{PWM} = 0V		2	3	mA
$I_{IN(SW)}$	Input switching current	V_{CC} = 7.5 V, C_{GDRV} = 1 nF		5.6	6	mA
BIAS SUPPLY (VCC)						
$V_{VCC(REG)}$	Regulation voltage	No load	7	7.5	8	V
$V_{VCC(UVLO)}$	Supply undervoltage protection	VCC rising threshold, V_{IN} = 8V		4.3	4.9	V
		VCC falling threshold, V_{IN} = 8V	3.5	3.9		V
		Hysteresis		400		mV
$I_{VCC(LIMIT)}$	Supply current limit	V_{VCC} = 0V	36	42	48	mA
V_{DO}	LDO dropout voltage	I_{VCC} = 20mA, V_{IN} = 5V		300		mV
REFERENCE VOLTAGE (VREG5)						
VREG5	Reference voltage	No load	4.77	4.98	5.15	V
$I_{VREG5(LIMIT)}$	Current limit	VREG5 = 0V	36	46	50	mA
OSCILLATOR (RT)						
f_{SW}	Switching frequency	R_T = 40 kΩ	175	204	225	kHz
		R_T = 20 kΩ	341	394	439	kHz
V_{RT}	RT output voltage			1		V
V_{SYNC}	SYNC rising threshold	V_{RT} rising	2.5	2.86	3.1	V
	SYNC falling threshold	V_{RT} falling	1.8	2		V
$t_{SYNC(MIN)}$	Minimum SYNC clock pulse width			100		ns
SPREAD SPECTRUM FREQUENCY MODULATION (SSM)						
$V_{SSM(TR)}$	Triangle wave voltage peak (High)			1.15		V
$V_{SSM(TR)}$	Triangle wave voltage peak (Low)			0.85		V
$V_{SSM(EN)}$	Spread spectrum modulation threshold		0.65	0.7	0.75	V
$V_{SSM(Clamp)}$	Internal clamp voltage		1.22	1.24	1.28	V
GDRV DRIVER (GDRV)						
R_{GH}	Gate driver high side resistance	I_{GDRV} = –10 mA	3	3.9	11.2	Ω
R_{GL}	Gate driver low side resistance	I_{GDRV} = 10 mA	3	3.8	10.5	Ω
CURRENT SENSE (SCS)						
$V_{SCS(LIMIT)}$	Current limit threshold	V_{DIM} = 5 V, R_{GPWM} = 250 kΩ	235	250	265	mV
		V_{DIM} = 0 V, R_{GPWM} = 250 kΩ	674	700	726	mV
$t_{SCS(BLANK)}$	Leading edge blanking time		85	115	155	ns
$t_{SCS(FAULT)}$	Current limit fault time			33		µs
$t_{ILMT(DLY)}$	SCS to GDRV propagation delay	V_{SCS} pulsed from 0 V to 1 V		75		ns
PWM COMPARATOR AND SLOPE COMPENSATION (SLOPE)						
D_{MAX}	Maximum duty cycle		90	94.3	96	%
V_{SLOPE}	Slope compensation		390	411.7	420	mV
V_{LV}	SCS to COMP level shift voltage	No slope compensation added	1.42	1.6	1.8	V
I_{LV}	SCS level shift bias current	No slope compensation added	16	19	22	µA

CURRENT SENSE AMPLIFIER (CSP, CSN)						
$V_{(CSP-CSN)}$	Current sense thresholds	V_{CSP} = 14 V, V_{IADJ} = 2.29 V	154.5	160.1	165.7	mV
		V_{CSP} = 14 V, V_{IADJ} = 1.43 V	96.5	100	103.5	mV
$CS_{(BW)}$	Current sense unity gain bandwidth			500		kHz
G_{CS}	Current sense amplifier gain	$G = V_{IADJ}/V_{(CSP-CSN)}$		14.3		
$K_{(OCP)}$	Ratio of over-current detection threshold to analog adjust voltage	$K_{(OCP)} = V_{(OCP-THR)}/V_{IADJ}$	1.42	1.52	1.56	
$I_{CSP(BIAS)}$	CSP bias current		146	159	170	µA
$I_{CSN(BIAS)}$	CSN bias current		135	146	160	µA
CURRENT MONITOR (IMON)						
$I_{IMON(SRC)}$	IMON source current	$V_{(CSP-CSN)}$ = 150 mV, V_{IMON} = 0 V	66	87.5	111	µA
$V_{IMON(CLP)}$	IMON output clamp voltage		3.3	3.6	4.1	V
$V_{IMON(OS)}$	IMON buffer offset voltage		-10	0	10	mV
FAULT INDICATOR (/FLT)						
$R_{(/FLT)}$	Open-drain pull down resistance			300		Ω
$t_{(FAULT\_TIMER)}$	Fault timer		28.5	36	43.5	ms
ANALOG ADJUST (IADJ)						
$V_{IADJ(CLP)}$	IADJ internal clamp voltage	I_{IADJ} = 1 µA	2.25	2.4	2.55	V
$I_{IADJ(BIAS)}$	IADJ input bias current	V_{IADJ} < 2.2 V	-10	3.1	10	nA
$R_{IADJ(LMT)}$	IADJ current limiting series resistor	V_{IADJ} > 2.6 V	13	14.5	16	kΩ
ERROR AMPLIFIER (COMP)						
g_M	Transconductance		78	86	96	µA/V
$I_{COMP(SRC)}$	COMP current source capacity	V_{IADJ} = 1.4 V, $V_{(CSP-CSN)}$ = 0 V	110	121	134	µA
$I_{COMP(SINK)}$	COMP current sink capacity	V_{IADJ} = 0 V, $V_{(CSP-CSN)}$ = 0.1 V	87	97	107	µA
$EA_{(BW)}$	Error amplifier bandwidth	Gain = –3 dB		5		MHz
$V_{COMP(RST)}$	COMP pin reset voltage		100	112	125	mV
$R_{COMP(DCH)}$	COMP discharge FET resistance		264	294	323	Ω
SOFT-START (SS)						
I_{SS}	Soft-start source current		7.7	10.7	12.8	µA
$V_{SS(UVP\_EN)}$	Soft-start voltage threshold to enable output under-voltage protection			2.4		V
$V_{SS(RST)}$	Soft-start pin reset voltage		50	58	70	mV
$R_{SS(DCH)}$	SS discharge FET resistance		275	300	337	Ω
OUTPUT VOLTAGE PROTECTION (OVP)						
$V_{OVP(THR)}$	Overvoltage protection threshold		1.189	1.22	1.251	V
$V_{UVP(THR)}$	Undervoltage protection threshold		83.7	100	113.1	mV
$t_{(UVP-BLANK)}$	Undervoltage protection blanking period			4		µs
$I_{OVP(HYS)}$	OVP hysteresis current		15	20	27.5	µA
INTERNAL PWM RAMP GENERATOR (GPWM)						
$I_{GPWM-source}$	GPWM generator source current		8.2	10	11	µA
$I_{GPWM-sink}$	GPWM generator sink current		8.2	10	11	µA
$V_{GPWM-peak}$	GPWM signal peak (high)			2.94		V
$V_{GPWM-valley}$	GPWM signal valley (low)			1.04		V

DIM INPUT (DIM/EN)						
$V_{DIM(HIGH)}$	Trigger logic level (high threshold)	V_{GPWM} = 2.0 V	1.9	2.0	2.2	V
$V_{DIM (LOW)}$	Trigger logic level (low threshold)	V_{GPWM} = 2.0 V	1.8	2.0	2.1	V
R_{DIM}	PWM pull-down resistance		7	10	20	MΩ
$t_{DLY (RISE)}$	PWM rising to PDRV delay		170	227.7	360	ns
$t_{DLY (FALL)}$	PWM falling to PDRV delay		170	238.8	360	ns
SERIES P-CHANNEL MOSFET DRIVE OUTPUT (PDRV)						
$V_{PDRV(OFF)}$	P-channel gate driver off-state voltage	V_{CSP} = 14V	13.7	14	14.3	V
$V_{PDRV(ON)}$	P-channel gate driver on-state voltage	V_{CSP} = 14V	7.5	7.7	8.5	V
$I_{PDRV(SINK)}$	PDRV sink current	Pulsed		50		mA
R_{PDRV}	PDRV driver pull up resistance		65	75	85	Ω
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown temperature			175		°C
$T_{SD(HYS)}$	Thermal shutdown hysteresis			20		°C

11. DESIGN GUIDE

APPLICATION CIRCUIT

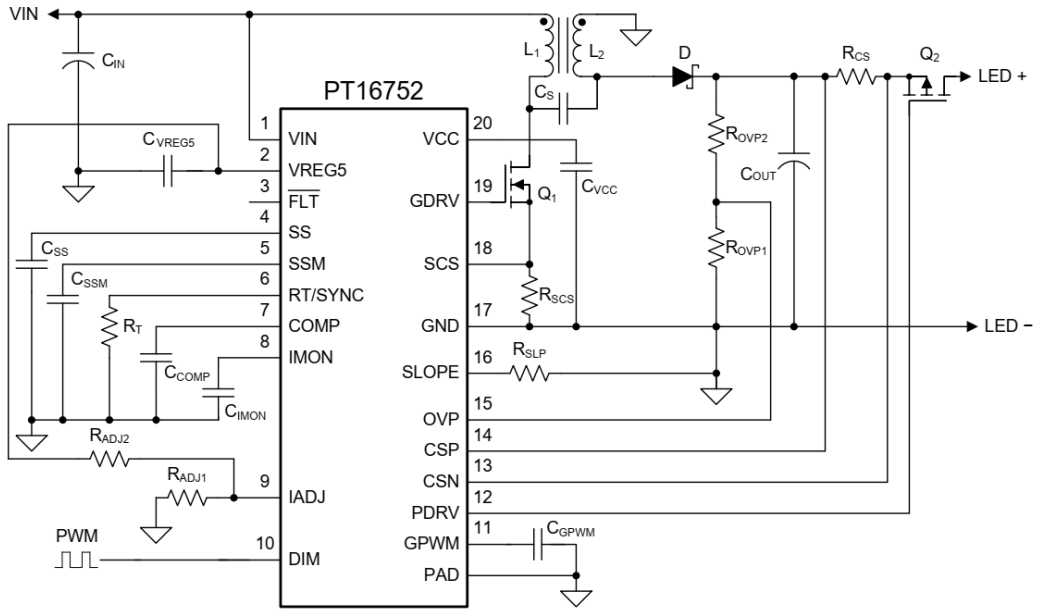


Figure 19. SEPIC LED Driver

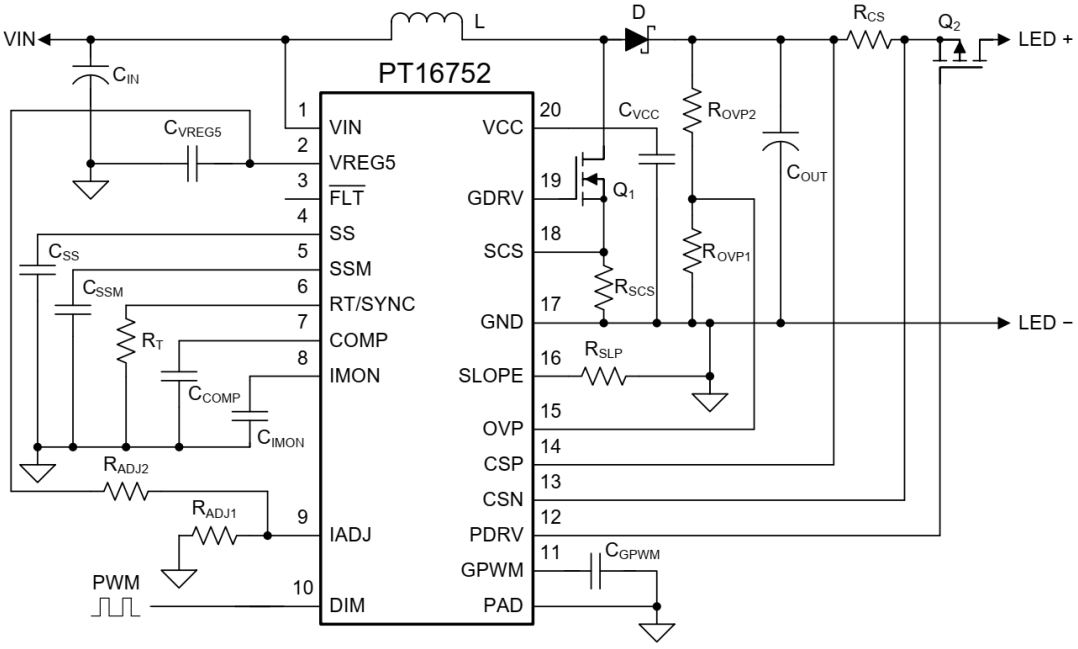


Figure 20. Boost LED Driver

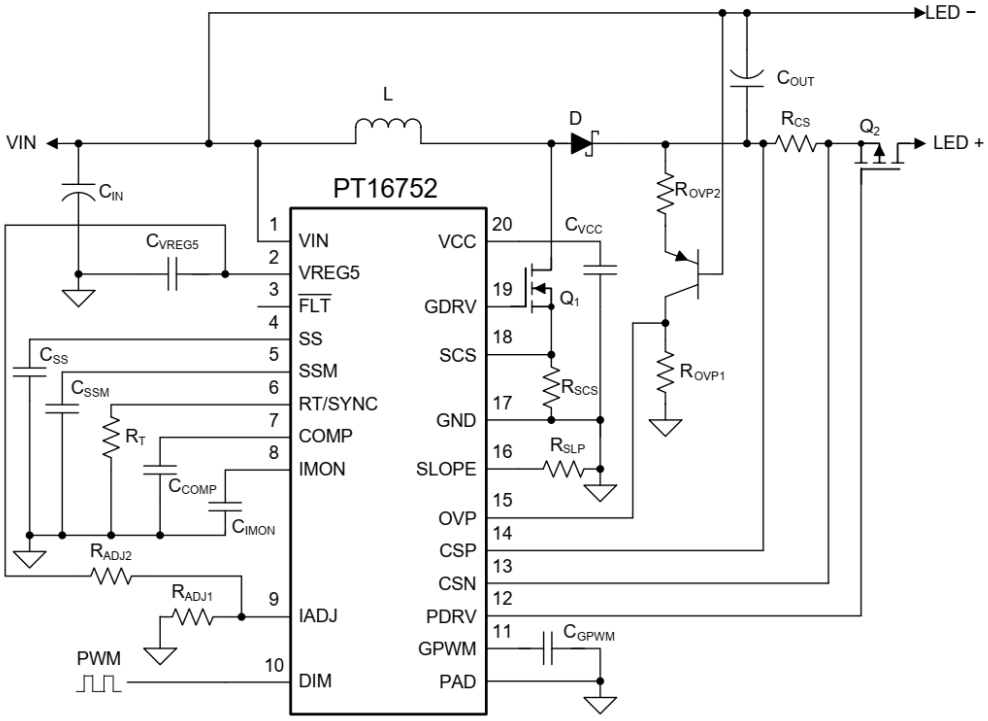


Figure 21. Buck-Boost LED Driver

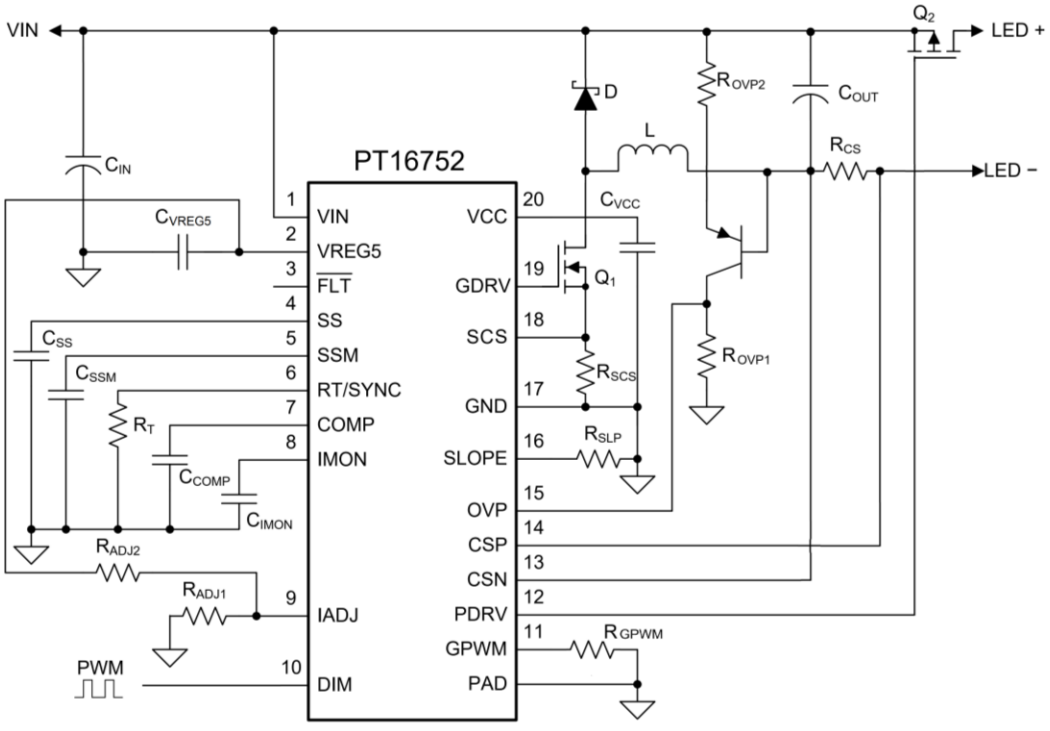


Figure 22. Buck LED Driver

DESIGN PROCEDURE

1. Duty Cycle Calculation

The switching duty cycle (D) defines the converter operation, and is related to the input and output voltages. In steady state, the duty cycle is calculated using following expression:

Buck:	Boost:	SEPIC/Buck-Boost:
$D = \frac{V_O}{V_{IN}}$	$D = \frac{V_O - V_{IN}}{V_O}$	$D = \frac{V_O}{V_O + V_{IN}}$
$D_{MIN} = \frac{V_O}{V_{IN(MAX)}}$	$D_{MIN} = \frac{V_O - V_{IN(MAX)}}{V_O}$	$D_{MIN} = \frac{V_O}{V_O + V_{IN(MAX)}}$
$D_{MAX} = \frac{V_O}{V_{IN(MIN)}}$	$D_{MAX} = \frac{V_O - V_{IN(MIN)}}{V_O}$	$D_{MAX} = \frac{V_O}{V_O + V_{IN(MIN)}}$

The duty cycle must be within the operating range of the controller to ensure that the closed-loop LED current regulation is in the specified input and output voltage range.

2. Inductance Calculation

Consider a good compromise between core loss and copper loss of the inductor, the inductor peak-to-peak ripple current, $\Delta i_{L\text{-}PP}$, is typically set between 20% and 80% of the maximum inductor current, I_L. Higher ripple inductor current allows a smaller inductor size, but needs more capacitors on the output to smooth the LED current ripple. Knowing the desired ripple ratio RR, switching frequency f_{SW}, maximum duty cycle D_{MAX}, and the typical LED current I_{LED}, the inductor value can be calculated as follows:

Buck:

$$\Delta i_{L(PP)} = RR \times I_L = RR \times I_{LED}$$

$$L = \frac{(V_{IN(MIN)} - V_O) \times D_{MAX}}{\Delta i_{L(PP)} \times f_{SW}}$$

Boost and Buck-Boost (SEPIC):

$$\Delta i_{L(PP)} = RR \times I_L = RR \times \frac{I_{LED}}{1 - D_{MAX}}$$

$$L = \frac{V_{IN(MIN)} \times D_{MAX}}{\Delta i_{L(PP)} \times f_{SW}}$$

As an alternative, the inductor can be selected based on CCM-DCM boundary condition specified based on output power, $P_{O(BDRY)}$. This approach ensures CCM operation in battery-powered LED driver applications that are required to support different LED string configurations with a wide range of programmable LED current set points. The CCM-DCM boundary condition can be estimated based on the lowest LED current and the lowest output voltage requirements for a given application.

$$P_{O(BDRY)} \leqslant I_{LED(MIN)} \text{ X } V_{O(MIN)}$$

Buck:

$$L = \frac{V_{O(MAX)}^2}{2 \times P_{O(BDRY)} \times f_{SW}} \times (1 - \frac{V_{OUT(MAX)}}{V_{IN}})$$

Boost:

$$L = \frac{V_{IN}^2}{2 \times P_{O(BDRY)} \times f_{SW}} \times (1 - \frac{V_{IN}}{V_{O(MAX)}})$$

Buck-Boost and SEPIC:

$$L = \frac{1}{2 \times P_{O(BDRY)} \times f_{SW} \times (\frac{1}{V_{O(MAX)}} + \frac{1}{V_{IN}})^2}$$

Select inductor with saturation current rating greater than the peak inductor current, $I_{L(PK)}$, at the maximum operating temperature.

$$I_{L(PK)} = I_L + \frac{V_{IN(MIN)} \times D_{MAX}}{2 \times L \times f_{SW}}$$

3. Input Capacitor Value Calculation

The input capacitors, C_{IN}, smooth the input voltage ripple and store energy to supply input current during input voltage drop or PWM dimming transients. In the Boost, SEPIC, and Cuk topology, the series inductor provides continuous input current so that requires a smaller input capacitor to achieve desired input ripple voltage, $\Delta v_{IN(PP)}$.

The Buck and Buck-Boost topology have discontinuous input current, and larger capacitors are required to achieve the same input voltage ripple. Based on the switching frequency, f_{SW}, and the maximum duty cycle, D_{MAX}, the input capacitor value can be calculated as follows:

Buck:

$$C_{IN} = \frac{I_{LED} \times D_{MAX} \times (1 - D_{MAX})}{f_{SW} \times \Delta v_{IN(PP)}}$$

Boost:

$$C_{IN} = \frac{\Delta i_{L(PP)}}{8 \times f_{SW} \times \Delta v_{IN(PP)}}$$

Buck-Boost:

$$C_{IN} = \frac{I_{LED} \times D_{MAX}}{f_{SW} \times \Delta v_{IN(PP)}}$$

For most applications, it highly recommends to select X7R dielectric-based ceramic capacitors due to their low ESR, high ripple current rating, and good temperature performance. For PWM dimming application, aluminum electrolytic capacitor and ceramic capacitor are recommended to minimize the voltage deviation due to large input current transients generated in conjunction with the rising and falling edges of the LED current.

Decouple VIN pin with a 0.1μF ceramic capacitor, placed as close as possible to the device and a series 10Ω resistor to create a 150kHz low-pass filter and eliminate undesired high-frequency noise.

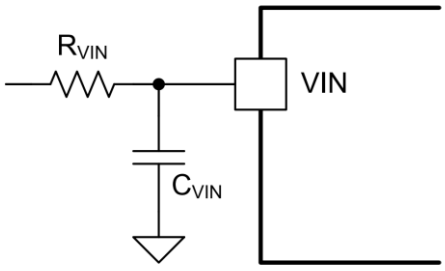


Figure 23. VIN Filter

4. Output Capacitor Value Calculation

Using the output capacitors to attenuate the discontinuous or large ripple current generated by switching and achieve the desired LED output current ripple, $\Delta i_{LED(PP)}$. The capacitor value depends on the total series resistance of the LED string, r_D and the switching frequency, f_{SW}. The capacitance required for the target LED ripple current can be calculated based on following equations.

Buck:

$$C_{OUT} = \frac{\Delta i_{L(PP)}}{8 \times f_{SW} \times r_D \times \Delta i_{LED(PP)}}$$

Boost and Buck-Boost:

$$C_{OUT} = \frac{I_{LED} \times D_{MAX}}{f_{SW} \times r_D \times \Delta i_{LED(PP)}}$$

For the Buck topology, the inductor is in series with LED load and requires a smaller capacitor than the Boost, Buck-Boost, and SEPIC topologies to achieve the same LED ripple current.

The ESR and the ESL characteristics must be considered when selecting the output capacitors, as they directly impact the LED current ripple. Ceramic capacitors are the best choice because of its low ESR, high ripple current rating, long lifetime, and good temperature performance. When selecting ceramic capacitors, it is important to consider the derating factors associated with higher temperature and DC bias operating conditions.

It is recommended to use X7R dielectric with rated voltage greater than the maximum LED voltage. Aluminum electrolytic capacitors can be used in parallel with ceramic capacitors to provide large capacity energy storage. The aluminum capacitors must have the necessary RMS current and temperature ratings to ensure extended operating lifetime. The minimum allowable output capacitor RMS current rating, $I_{COUT(RMS)}$, can be approximated

Buck:

$$I_{COUT(RMS)} = \frac{\Delta i_{LED(PP)}}{\sqrt{12}}$$

Boost and Buck-Boost:

$$I_{COUT(RMS)} = I_{LED} \times \sqrt{\frac{D_{MAX}}{1 - D_{MAX}}}$$

For applications that need to support different LED string configurations with a wide range of programmable LED current set points, rearrange the previous expressions based on the maximum output power to reflect output capacitance, to ensure that LED current ripple meets the requirements over the entire range of operation.

5. LED Current Programming

The LED current is set by the current sense resistor, R_{CS}, and the analog adjust voltage, V_{IADJ}. The current sense resistor is placed in series with the LED load. The CSP and CSN inputs of the internal rail-to-rail current sense amplifier are connected to the RCS resistor to achieve closed-loop regulation. When VIADJ > 2.29V, the internal reference clamps the $V_{(CSP-CSN)}$ to 0.168V, the LED current is set by flowing equation:

$$I_{LED} = \frac{0.168}{R_{CS}}$$

The LED current can be programmed by varying V_{IADJ} between 286mV to 2.29V. The LED current can be calculated using:

$$I_{LED} = \frac{V_{IADJ}}{14.3 \times R_{CS}}$$

Using a low-pass common-mode filter consisting of 10Ω resistors in series with CSP and CSN inputs, and place 0.01uF capacitor to ground to the minimize the impact of voltage ripple and noise on LED current accuracy (see Figure 11). A 0.1μF capacitor across CSP and CSN is included to filter high-frequency differential noise.

6. Main Power MOSFET Selection

The power MOSFET should be able to endure the maximum switch node voltage, V_{SW}, and switch RMS current derived based on the converter topology. In order to ensure safe operation, the drain voltage V_{DS} is at least 20% greater than the maximum switch node voltage. The MOSFET Drain-Source breakdown voltage, V_{DS}, and RMS current ratings are calculated using the following expressions.

Buck:

$$V_{DS} = V_{IN(MAX)} \times 1.2$$

$$I_{Q(RMS)} = I_{LED} \times \sqrt{D_{MAX}}$$

Boost:

$$V_{DS} = V_{O(OV)} \times 1.2$$

$$I_{Q(RMS)} = I_{LED} \times \frac{\sqrt{D_{MAX}}}{1 - D_{MAX}}$$

Buck-Boost:

$$V_{DS} = (V_{IN(MAX)} + V_{O(OV)}) \times 1.2$$

$$I_{Q(RMS)} = I_{LED} \times \frac{\sqrt{D_{MAX}}}{1 - D_{MAX}}$$

Where the voltage, $V_{O(OV)}$, is the overvoltage protection threshold and the worst-case output voltage under fault conditions.

A MOSFET with low total gate charge, Q_g is selected to minimize gate drive and switching losses. The R_{DS} resistance of MOSFET is usually an unimportant parameter because the switch conduction losses are not a significant part of the total converter losses at high operation frequency. The switching and conduction losses are calculated as follows:

$$P_{COND} = R_{DS} \times I_{Q(RMS)}^2$$

$$P_{SW} = \frac{I_L \times V_{SW}^2 \times C_{RSS} \times f_{SW}}{I_{GDRV}}$$

C_{RSS} is the MOSFET reverse transfer capacitance. I_L is the average inductor current. I_{GDRV} is gate drive output current, typically 500mA. The MOSFET power rating and package should be selected based on the total calculated loss, the ambient operating temperature, and maximum allowable temperature rise.

7. Rectifier Diode Selection

It suggests that use a Schottky diode as rectifier diode, because it provides the best efficiency due to the low forward voltage drop and near-zero reverse recovery time. Choose a diode with a reverse breakdown voltage, $V_{D(BR)}$, greater than or equal to MOSFET drain-to-source voltage, V_{DS}, for reliable performance. It is important to understand the leakage current characteristics of the Schottky diode, especially at high operating temperatures because it impacts the overall converter operation and efficiency.

The current through the diode, I_D, is given by:

$$I_D = I_L \times (1 - D_{MAX})$$

The diode power rating and package is selected based on the calculated current, the ambient temperature and the maximum allowable temperature rise.

8. Switch Current Sense Resistor

The switch current sense resistor, R_{SCS}, is used for peak current mode control and to set the peak current limit. The value of R_{SCS} is selected to protect the main switching MOSFET under fault conditions. The R_{SCS} can be calculated based on peak inductor current, $I_{L(PK)}$, and switch current limit threshold, $V_{SCS(LIMIT)}$.

$$R_{SCS} = \frac{V_{SCS(LIMT)}}{I_{L(PK)}}$$

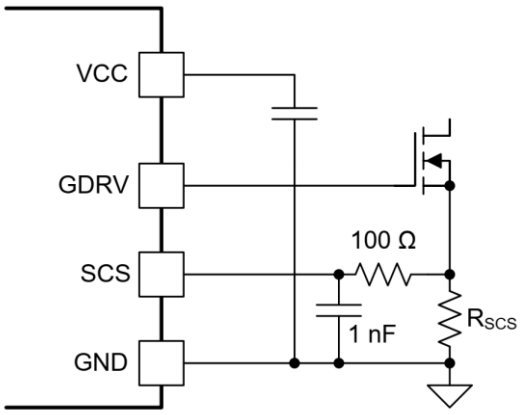


Figure 24. SCS Input Filter

The use of a 1nF and 100Ω low-pass filter is optional. If used, the resistor value should be less than 500Ω to limit its influence on the internal slope compensation signal.

9. Feedback Compensation

The open-loop response is the product of the modulator transfer function and the feedback transfer function. Using a first-order approximation, the modulator transfer function can be modeled as a single pole created by the output capacitor, and in the boost and buck-boost topologies, a right half-plane zero created by the inductor, where both have a dependence on the LED string dynamic resistance, r_D. Because it recommends a ceramic capacitor, the ESR of the output capacitor is neglected in the analysis. The small-signal modulator model also includes a DC gain factor that is dependent on the duty cycle, output voltage, and LED current.

$$\frac{\hat{i}_{LED}}{\hat{v}_{COMP}} = G_0 \frac{\left(1-\frac{s}{\omega_Z}\right)}{\left(1+\frac{s}{\omega_P}\right)}$$

Table 1. The small-signal model parameters.

	DC GAIN (G_0)	POLE FREQUENCY (ω_P)	ZERO FREQUENCY (ω_Z)
Buck	1	$\frac{1}{r_D \times C_{OUT}}$	/
Boost	$\frac{(1-D)\times V_O}{R_{SCS}\times(V_O+(r_D\times I_{LED}))}$	$\frac{V_O+(r_D\times I_{LED})}{V_O\times r_D\times C_{OUT}}$	$\frac{V_O\times(1-D)^2}{L\times I_{LED}}$
Buck-Boost	$\frac{(1-D)\times V_O}{R_{SCS}\times(V_O+(D\times r_D\times I_{LED}))}$	$\frac{V_O+(D\times r_D\times I_{LED})}{V_O\times r_D\times C_{OUT}}$	$\frac{V_O\times(1-D)^2}{D\times L\times I_{LED}}$

The feedback transfer function includes the current sense resistor and the loop compensation of the transconductance amplifier. A compensation network at the output of the error amplifier is used to configure loop gain and phase characteristics. A simple capacitor, C_{COMP}, from COMP to GND (as shown in Figure 25) provides integral compensation and creates a pole at the origin. Alternatively, a network of R_{COMP}, C_{COMP}, and C_{HF}, shown in Figure 26, can be used to implement proportional and integral (PI) compensation and to create a pole at the origin, a low-frequency zero, and a high-frequency pole.

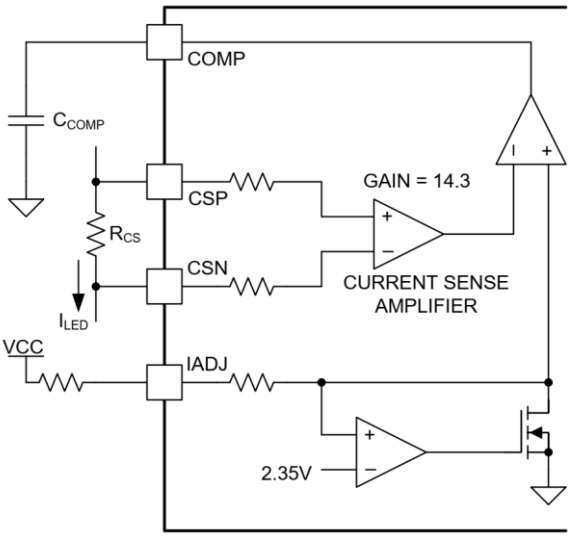


Figure 25. Integral Compensation

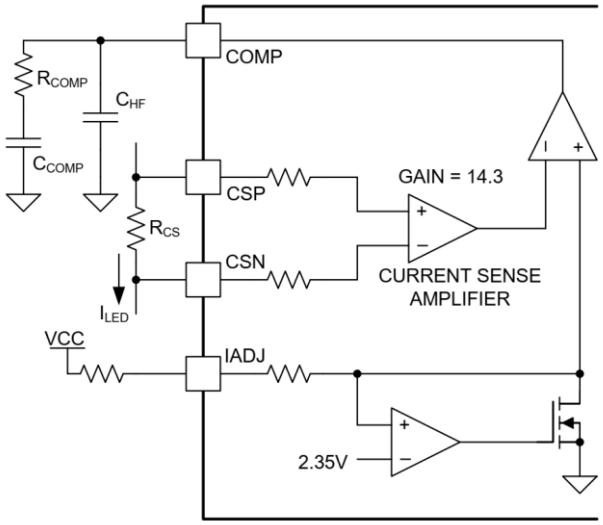


Figure 26. Proportional-Integral Compensation

The feedback transfer function is defined as follows.
Feedback transfer function with integral compensation:

$$-\frac{\hat{v}_{COMP}}{\hat{i}_{LED}} = \frac{14.3 \times g_M \times R_{CS}}{s \times C_{COMP}}$$

Feedback transfer function with proportional integral compensation:

$$-\frac{\hat{v}_{COMP}}{\hat{i}_{LED}} = \frac{14.3 \times g_M \times R_{CS}}{s \times (C_{COMP} + C_{HF})} \frac{(1 + s \times R_{COMP} \times C_{COMP})}{\left(1 + s \times R_{COMP} \times \left(\frac{C_{COMP} \times C_{HF}}{C_{COMP} + C_{HF}}\right)\right)}$$

The pole at the origin minimizes output steady-state error. High bandwidth is achieved with the PI compensator by placing the low-frequency zero an order of magnitude less than the crossover frequency. Use the following expressions to calculate the compensation network.
Buck with integral compensator:

$$C_{COMP} = \frac{8.75 \times 10^{-3} \times R_{CS}}{\omega_P}$$

Boost and Buck-Boost with proportional integral compensator:

$$C_{COMP} = 8.75 \times 10^{-3} \times \left(\frac{R_{CS} \times G_0}{\omega_Z}\right)$$

$$C_{HF} = \frac{C_{COMP}}{100}$$

$$R_{COMP} = \frac{1}{\omega_P \times C_{COMP}}$$

The loop response is verified by applying step input voltage transients. The goal is to minimize LED current overshoot and undershoot with a damped response. Additional tuning of the compensation network may be necessary to optimize PWM dimming performance.

10. Soft-Start

The time required for the LED current to reach the target setpoint is named the soft-start time (t_{SS}). Using a capacitor C_{SS} (from SS pin to GND) to set the required soft-start time, t_{SS}. C_{SS} can be calculated by following equation.

$$C_{SS} = 9 \times 10^{-6} \times t_{SS}(\mu F)$$

t_{SS}: s

11. Overvoltage and Undervoltage Protection

The controller includes a dedicated OVP pin which can be used for output overvoltage protection. For Boost and SEPIC topologies, as shown in Figure 19 and Figure 20, the overvoltage threshold is programmed using a resistor divider, R_{OV1} and R_{OV2}, from the output voltage(V_O) to GND. In the Buck-Boost or Buck configuration, as shown in Figure 21 and Figure 22, if the LEDs are referenced to a potential other than ground, the output voltage is sensed and translated to ground by using a PNP transistor and level-shift resistors.

The overvoltage turn-off threshold, $V_{O(OV)}$, is:

Boost:

$$V_{O(OV)} = V_{OVP(THR)} \times \left(\frac{R_{OV1} + R_{OV2}}{R_{OV1}}\right)$$

Buck and Buck-Boost:

$$V_{O(OV)} = V_{OVP(THR)} \times \frac{R_{OV2}}{R_{OV1}} + 0.7$$

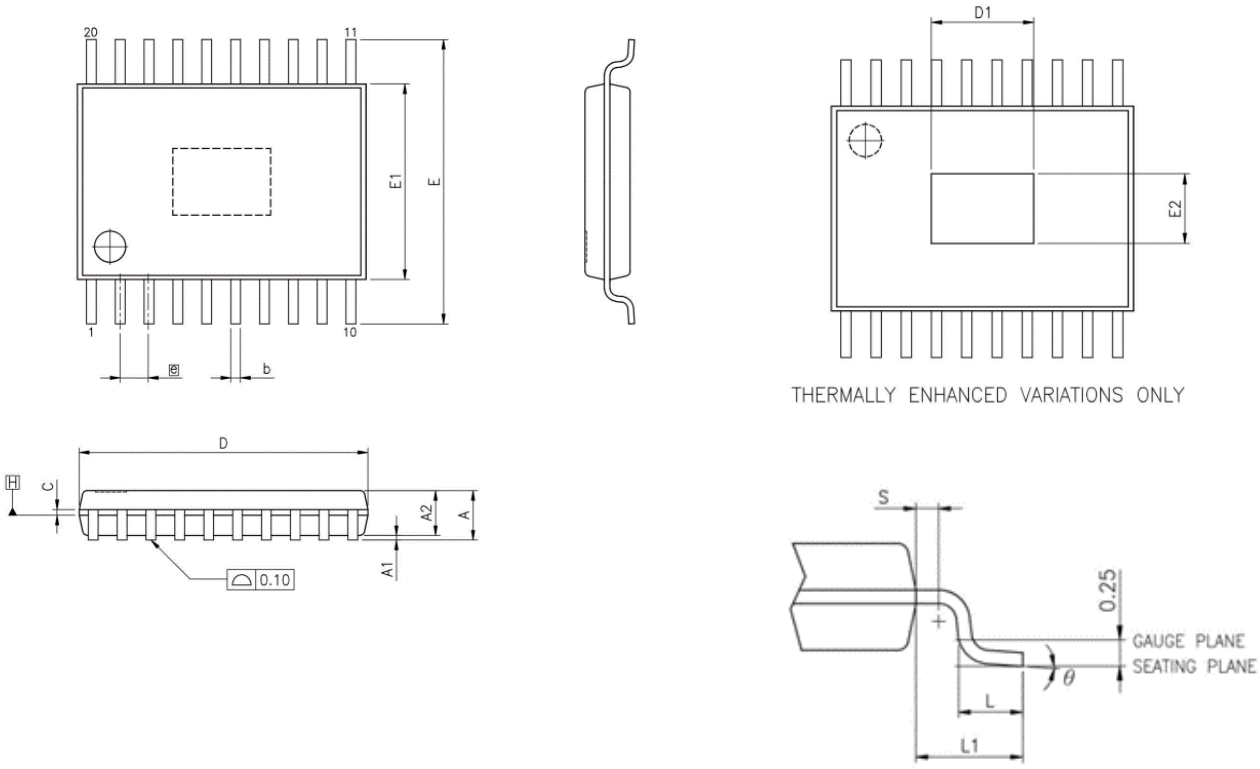
The overvoltage hysteresis, $V_{OV(HYS)}$ is:

$$V_{OV(HYS)} = I_{OVP(HYS)} \times R_{OV2}$$

The corresponding undervoltage fault threshold, $V_{O(UV)}$ is:

$$V_{O(UV)} = 0.1 \times \left(\frac{R_{OV1} + R_{OV2}}{R_{OV1}}\right)$$

12. PACKAGE INFORMATION



Refer to JEDEC MO-153 ACT

Symbol	Dimensions		
	Min.	Nom.	Max.
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
b	0.19	—	0.30
c	0.09	—	0.20
e	0.65 BSC		
D	6.40	6.50	6.60
D1	—	3.99	—
E	6.40 BSC		
E1	4.30	4.4	4.50
E2	—	2.8	—
S	0.2	—	—
L	0.5	0.60	0.75
L1	1.00 REF		
θ	0 °	—	8 °

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