# DESCRIPTION

The PT3344 is a stereo audio digital to analog converter (DAC), the chip includes interpolation filter, fourth-order multi-bit delta-sigma modulator, and analog output signal is filtering by on-chip switched-capacitor low-pass filter. The digital input interface compliant to industrial standard $I^2S$ format exclusively.

PT3344 support the audio sampling rates from 8KHz up to 200KHz, and internal timing circuit will automatic detects the clock ratio between the sample rate clock (LRCI) and system master clock (MCK) and auto-select the proper clock for system processing.

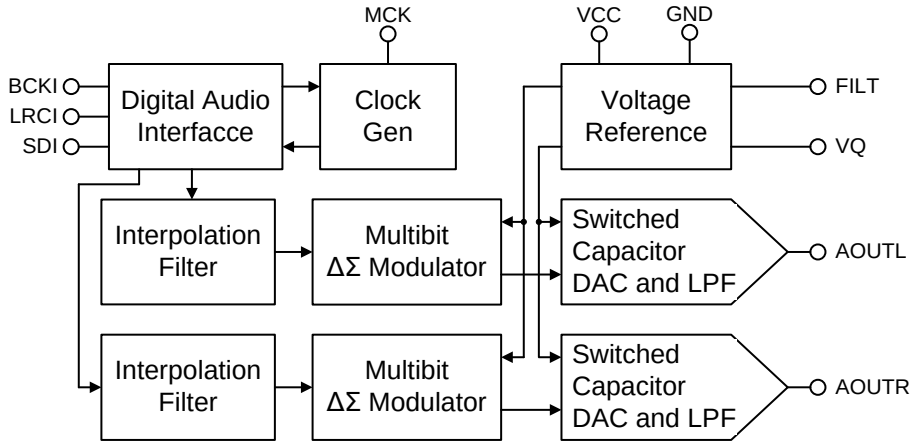
# FEATURES

- Single +3.3V or +5V Power Supply
- Support Sample Rates : 8 ~ 192KHz
- Support 24-bit Audio Data Conversion
- Support $I^2S$ format exclusively
- 102 dB Dynamic Range
- -85 dB THD+N
- Multi-bit Delta-Sigma Modulator
- Auto-Detect MCK/LRCI clock Ratio
- Low Clock-Jitter Sensitivity
- On-chip Low-pass Filter for Line-Level Outputs
- 10-pin MSOP Package

# APPLICATIONS

- Set top box
- Home theater
- TV or PC display audio decoding
- Projector

# BLOCK DIAGRAM



# APPLICATION CIRCUIT

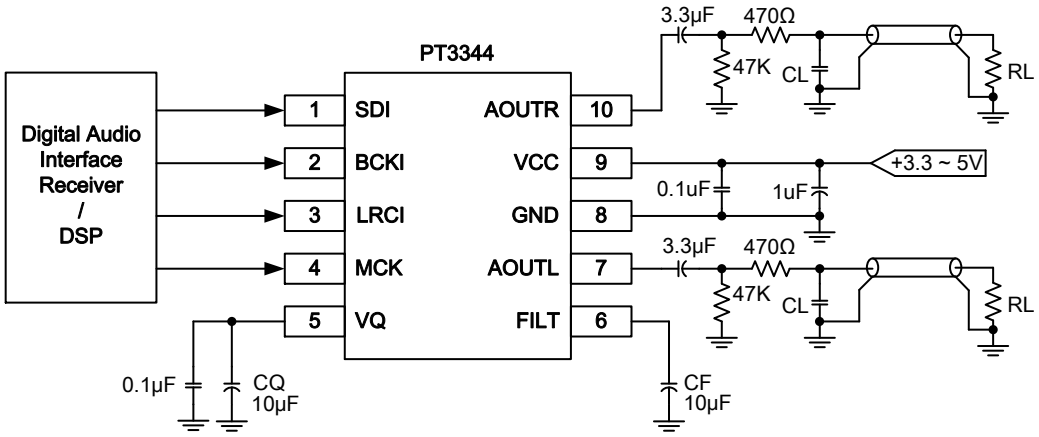



**Figure 1, Application Circuit**

| Part No. | Recommended Value | Description |
|---|---|---|
| CF | 10μF | Bypass capacitor for internal voltage reference |
| CQ | 10μF // 0.1μF | Output soft ramps-up time control, applies a 10μF cap for 450ms delay, and 3.3μF for 280ms delay. |
| CL | 3300pF | External low-pass filter in-cooperates with a 470Ω resistor. |
| RL | >10KΩ | Output AC-loaded resistance, should not lower than recommend value to achieve specified full-scale output level. |

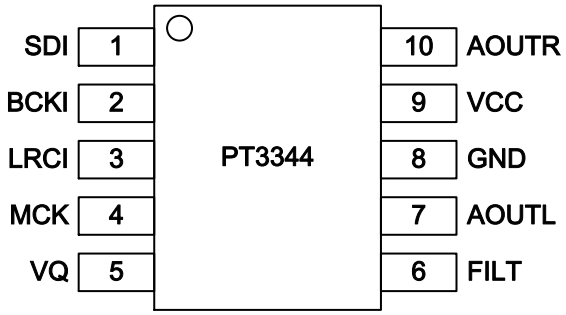
**Table 1, Application circuit parts recommendation**

# ORDER INFORMATION

| Valid Part Number | Package Type | Top Code |
|---|---|---|
| PT3344 | 10 Pin, MSOP | PT3344 |

# PIN CONFIGURATION

**Top View**



# PIN DESCRIPTION

| Pin Name | I/O | Description | Pin No. |
|---|---|---|---|
| SDI | I | Input pin for two's complement serial audio data. | 1 |
| BCKI | I | Input pin for serial clock input. | 2 |
| LRCI | I | Input pin for sample rate clock input. | 3 |
| MCK | I | Input pin for chip mater clock input | 4 |
| VQ | Power | Internal output bias voltage reference bypassing | 5 |
| FILT | O | Internal reference voltage bypassing for delta-sigma modulator circuits | 6 |
| AOUTL | O | The left channel analog line level output | 7 |
| GND | Power | Chip ground | 8 |
| VCC | Power | Positive power input for the analog and digital sections | 9 |
| AOUTR | O | The right channel analog line level output. | 10 |

# FUNCTION DESCRIPTION

## *MASTER CLOCK AND I²S DATABUS*

The MCK and LRCI clock must be an integer ratio, as shown in Table 1. The LRCI frequency is equal to audio sample rate (Fs), the MCK-to-LRCI frequency ratio detected automatically during the initialization procedure by counting the number of MCK transitions during a single LRCI period, next the internal dividers determinate the relatives speed mode of modulator and digital interpolation filter. The Table 2 shows several standard audio sample rates and correspond MCK and LRCI frequencies. Please note the MCK, LRCI and BCKI clocks must be synchronous and edge alignment.

| LRCI (KHz) | MCK(MHz) | | | Recommendation |
|---|---|---|---|---|
| | **128x** | **256x** | **512x** | |
| 32 | - | 8.192 | - | ▪ If **Fs≤96 KHz**, choose **256x Fs** clock as MCK.<br>▪ If **Fs>96 KHz**, choose **128x Fs** clock as MCK.<br>▪ The maximum MCK frequency should not exceeds 30MHz.<br>▪ QSM (Quarter Speed Mode), HSM (Half Speed Mode) and FSM (Full Speed Mode) is uses to determinate interpolation filter clock and coefficients. |
| 44.1 | - | 11.2896 | 22.5792 | |
| 48 | - | 12.288 | 24.576 | |
| 88.2 | 11.2896 | 22.5792 | - | |
| 96 | 12.288 | 24.576 | - | |
| 176.4 | 22.5792 | - | - | |
| 192 | 24.576 | - | - | |
| **Mode** | **QSM** | **HSM** | **FSM** | |

**Table 2, Master clock selection table**

The serial bit clock (BCKI) is the shift clock of the SDI input data. The rising edge of BCKI must align to the center portion of SDI data hold times. The BCKI/LRCI clock ratio is fixed in 64x Fs for proper 24bit audio data decoding. In the Figures 2 shows I²S data formats and clock relationship.

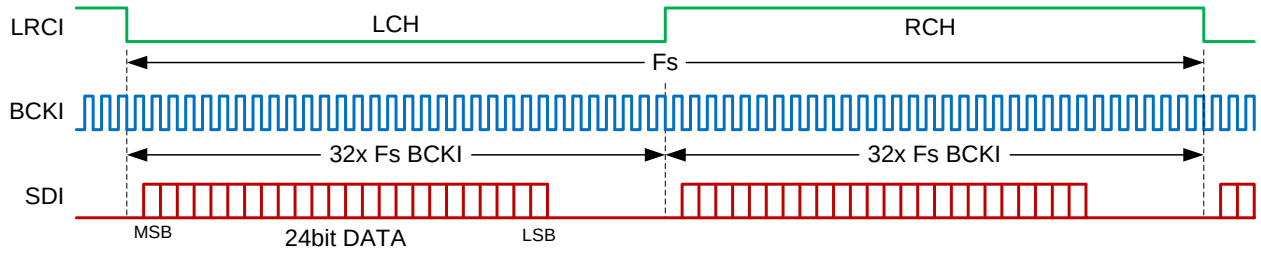



**Figure 2. PT3344 Digital Interface Data Format (I²S)**

IMPORTANT NOTICE

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