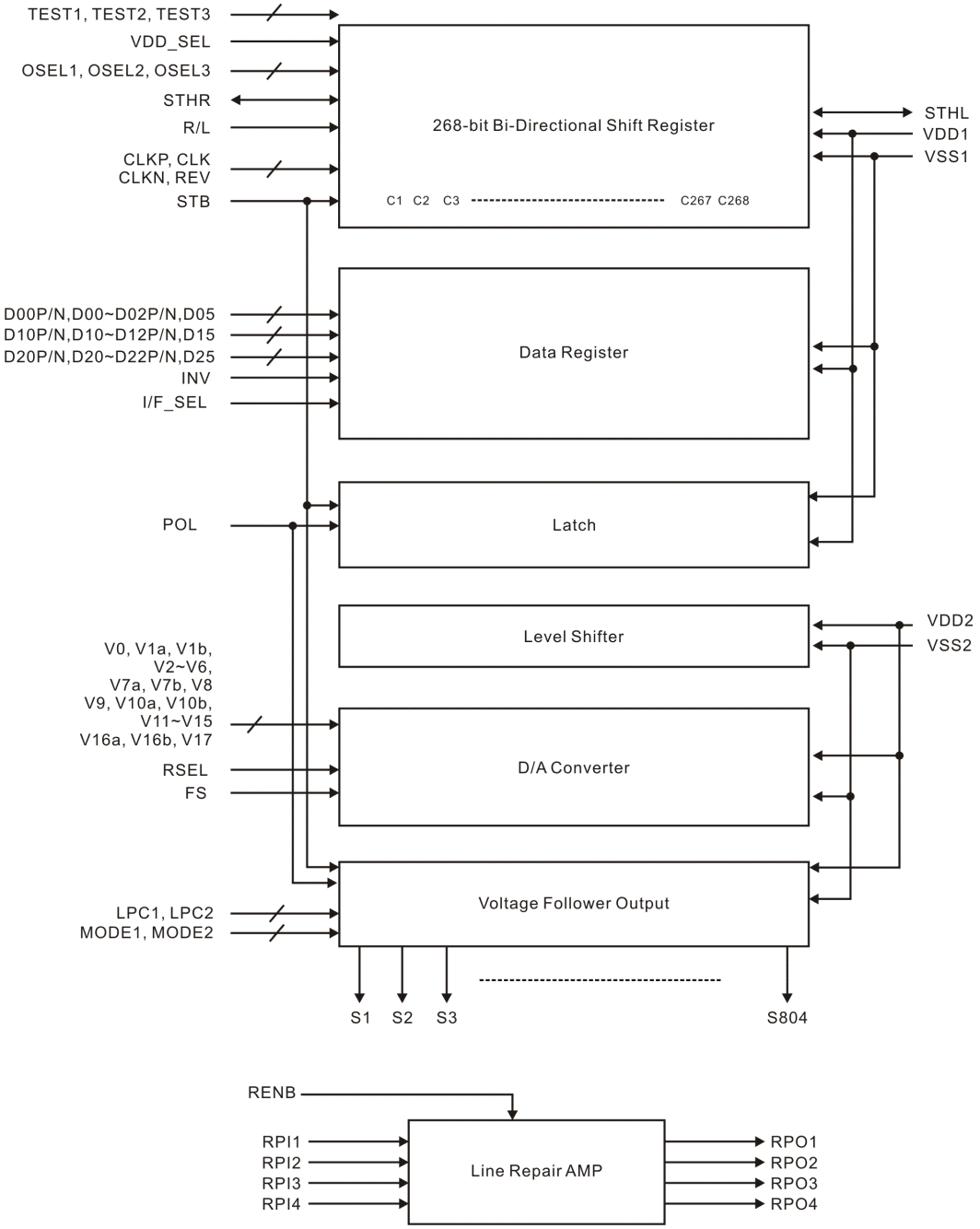
DESCRIPTION

The PT16102 is a CMOS silicon source driver IC for active matrix TFT LCD panels. After a CMOS/RSDS 6-bit RGB data is applied, this device will generate 64-gray scale for driving the TFT LCD panel source lines. It supports 804/792/768/720/684 channel selectable function, shift right/left selectable function, and cascade function for dot expansion.

FEATURES

- 64-gray scale source driver for active matrix TFT LCD panels
- Selectable 804/792/768/720/684 output channels
- Logic voltage power supply: 2.3V to 3.6V
- High voltage power supply: 7.5V to 13.5V
- Maximum RSDS operating frequency at 85 MHz
- Bi-directional shift right/left function
- COG package

BLOCK DIAGRAM

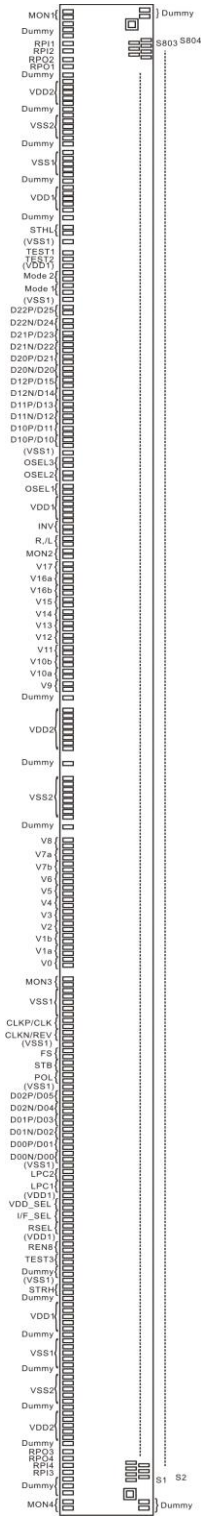


CONTENTS

1. ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT16102	COG	-

2. PIN CONFIGURATION



3. PIN DESCRIPTION

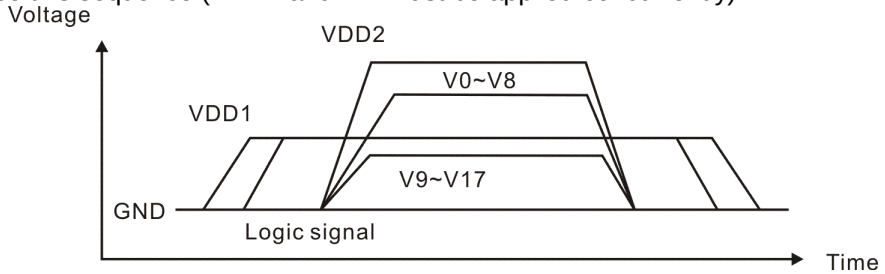
Symbol	Pin Name	I/O	Description
S1 to S804	Driver output	O	The D/A converted 64-qray-scale analog voltage is output.
I/F_SEL	Interface select	I	By setting this pin, the I/F input mode of this IC can be switched. When I/F_SEL pin = L or open, the mode is RSDS I/F. When I/F_SEL pin = H, the mode is CMOS I/F. This pin is pulled down to VSS1 within IC. Caution should be exercised because the pin function and electrical specifications of this IC change by setting this pin.
D00P/N,D00 to D02P/N, D05	Display data	I(Note)	The function of these pins changes according to the setting of I/F_SEL pin.
D10P/N,D10 to D12P/N, D15			When I/F _SEL pin = L or open, these pins become display data input pins in RSDS I/F mode (D00P/N to D02P/N, D10P/N to D12P/N, D20P/N to D22P/N). Display data are input by double-edged 9-bit width, or gray-scale data (6-bit) x 3-dot (1-pixel)
D20P/N,D20 to D22P/N, D25			When I/F_SEL pin = H, these pins become display data input pins in CMOS I/F mode (D00 to D15, D10 to D15, D20 to D25). Display data are input by single-edged 18-bit width, or gray-scale data (6-bit) x 3-dot (1- pixel). D x 0 = LSB, D x 5 = MSB
CLKP, CLK, CLKN, REV	Shift clock, CMOS data inversion (REV)	I(Note)	The function of this pin chances according to the setting of I/F_SEL pin.
			When I/F_SEL pin = L or open, these pins become shift clock input pins by the pair of CLKP and CLKN in RSDS I/F mode. This is shift clock input of the shift register. Display data are retrieved to the data register both on rising edges and falling edges.
			When I/F_SEL pin = H, it becomes a CLK (shift clock input) input pin and .REV (a signal to select inversion/non-inversion of display input data) in CMOS I/F mode. Display data is retrieved to the data register on a rising edge of CLK. REV: inverts/not inverts display data of D00 to D05, D10 to D15, and D20 to D25. REV = H: Inverts display data within IC. REV = L: Does not invert any input data.
R,/L	Shift direction control	I	This is a control pin of switching shift direction of start pulse I/O when ICs are connected in cascade. The shift directions are as follows. R,/L = H (VDD1 level): STHR input, S1~ S804, STHL output R,/L = L (VSS1 level): STHL input, S804~ S1, STHR output
STHR	Right shift start pulse	I/O	R,/L= H (VDD1 level): Start pulse input pin. R,IL = L (VSS1 level): Start pulse output pin
STHL	Left shift start pulse	I/O	R,/L = H (VDD1 level): Start pulse output pin. R,/L= L (VSS1 level): Start pulse input pin.
STB	Latch	I	The contents of data register are transferred to the latch circuit at rising edges. After an output short-circuit period, the gray scale voltage is supplied to the driver. This should be input by 1 pulse per horizontal period during a CMOS I/F mode (No double start pulse input is supported during a CMOS I/F mode).
INV	RSDS data inversion	I	This pin is valid only when I/F_SEL pin = L or open. It selects inversion/non-inversion of display input data in RSDS I/F mode. INV = H: Inverts data within this IC. INV = L: Does not invert any input data. DC signal should be input into this pin. For more details, reference to DATA INVERSION. This pin is pulled down to VSS1 within IC. Moreover, it becomes invalid when I/F_SEL pin = H (CMOS I/F mode). (Pull-down of this pin also exists even when it is Invalid.)
POL	Polarity select	I	POL = H (VDD1 level): S2n-1 output uses V0 to V8, and S2n output uses V9 to V17 as a reference power supply. POL = L (VSS1 level): S2n-1 output uses V9 to V17, and S2n output uses V0 to V8 as a reference power supply. S2n-1 indicates odd output and S2n shows even output. POL signal is input securing a setup time (tPOL-STB) to the rising edge of STB.

<table>
<tr><th>Symbol</th><th>Pin Name</th><th>I/O</th><th>Description</th></tr>
<tr><td>MODE1,MODE2</td><td>Charge sharing control</td><td>I</td><td>These pins control charge sharing function.
<table>
<tr><th>Mode1</th><th>Mode2</th><th>Charge Sharing</th></tr>
<tr><td>L or open</td><td>L or open</td><td>When the polarity changes because of switching POL. charge sharing function operates only during a STB = H period.</td></tr>
<tr><td>L or open</td><td>H</td><td>Whether a change of POL occurs or not. All outputs short-circuit (charge sharing) during the period of STB = H.</td></tr>
<tr><td>H</td><td>L or open</td><td rowspan="2">Charge sharing does not operate</td></tr>
<tr><td>H</td><td>H</td></tr>
</table>
These pins are pulled down to VSS1 within IC.
For details, refer to RELATIONSHIP BETWEEN MODE, STB, POL AND OUTPUT WAVEFORM.</td></tr>
<tr><td>OSEL1, OSEL2, OSEL3.</td><td>Output channel number selection</td><td>I</td><td>These pins determine the number of output
<table>
<tr><th>OSEL3</th><th>OSEL2</th><th>OSEL1</th><th>Number of Valid Output Pin</th><th>Number of Invalid Output Pin</th><th>Invalid Output Pin</th></tr>
<tr><td>L or open</td><td>L or open</td><td>L or open</td><td>804</td><td>0</td><td>-</td></tr>
<tr><td>L or open</td><td>L or open</td><td>H</td><td>768</td><td>36</td><td>S385 to S420 are Hi-Z.</td></tr>
<tr><td>L or open</td><td>H</td><td>L or open</td><td>720</td><td>84</td><td>S361 to S444 are Hi-Z.</td></tr>
<tr><td>L or open</td><td>H</td><td>H</td><td>684</td><td>120</td><td>S343 to S462 are Hi-Z.</td></tr>
<tr><td>H</td><td>L or open</td><td>L or open</td><td>792</td><td>12</td><td>S397 to S408 are Hi-Z.</td></tr>
</table>
Any setting other than shown above is not allowed to be set.
These pins are pulled down to VSS1 within IC.</td></tr>
<tr><td>LPC1, LPC2</td><td>Low power control</td><td>I</td><td>By setting these pins, it is possible to change the driving ability of output AMP. Caution is demanded because as the driving ability is increased more, the driver current consumption also becomes larger.
<table>
<tr><th>LPC1</th><th>LPC2</th><th>Driving Ability Mode</th><th>Reference Ratio</th></tr>
<tr><td>L or open</td><td>L or open</td><td>Low power mode</td><td>(80%)</td></tr>
<tr><td>L or open</td><td>H</td><td>Ultra low power mode</td><td>(70%)</td></tr>
<tr><td>H</td><td>L or open</td><td>Normal power mode</td><td>100%</td></tr>
<tr><td>H</td><td>H</td><td>High power mode</td><td>(130%)</td></tr>
</table>
These pins are pulled down to VSS1 within IC.</td></tr>
<tr><td>VDD_SEL</td><td>VDD1 selection control</td><td>I</td><td>VDD_SEL = L (VSS1 level) or open: VDD1 = 2.7 to 3.6 V mode
VDD_SEL = H (VDD1 level): VDD1 = 2.3 to 2.7 V mode
The "VDD1 = 2.3 to 2.7 V" mode is allowed to select for only RSDS I/F mode.
During a CMOS I/F mode, this pin shall be set to L (VSS1 level) or open, and used on a VDD1 = 2.7 to 3.6 V mode.
This pin is pulled down to VSS1 within IC.</td></tr>
<tr><td>RENB</td><td>Line repair AMP selection</td><td>-</td><td>By setting this pin, whether line repair AMP is used or not is determined.
When RENB = L or open:used
When RENB = H: Not used
This pin is pulled down to VSS1 within IC.</td></tr>
<tr><td>RPI1, RPI2, RPI3, RPI4</td><td rowspan="2">Line repair AMP</td><td>I</td><td rowspan="2">The driving ability of line repair AMP is three times as high as that of normal analog output.
Its relationship with RENB is shown below
<table>
<tr><th>RENB</th><th>RPIn (n = 1 to 4)</th><th>RPOn (n = 1 to 4)</th></tr>
<tr><td>H</td><td>Leave open.</td><td>Hi-z</td></tr>
<tr><td>L or open</td><td colspan="2">RPIn → Impedance conversion→RPOn</td></tr>
</table></td></tr>
<tr><td>RP01, RP02, RP03, RP04</td><td>O</td></tr>
<tr><td>RSEL</td><td>r –corrected power supply input switching</td><td>I</td><td>This pin selects voltage follower circuits (hereinafter, it maybe called r AMP) provide within IC.
RSEL = L or open: Selects Vnb (n = 1, 7, 10, 16) (γ AMP is not used).
RSEL = H : Selects Vna (n = 1, 7, 10,16) (γAMP is used).
This pin is pulled down to VSS1 within IC.</td></tr>
</table>

Symbol	Pin Name	I/O	Description
FS	Frame signal input	I	This pin inputs an offset cancel start signal to the y-corrected circuit which is provided on a γ –corrected power supply (Vna (n = 1, 7, 10, 16)). It is required to input one pulse per frame. Moreover, the number of times for STB to be input should be same in each frame. As for its timing, refer to **Switching Characteristic Waveform** (4/4).
V0, V1a, V1b, V2 to V6, V7a, V7b, V8, V9, V10a, V10b, V11 to V15, V16a, V16b, V17	*r*-corrected power supply	-	These pins input γ-corrected power supply externally. Selection of inputting Vna or Vnb (n = 1, 7, 10, 16) is executed by RSEL. Vna input pins have a γ AMP within IC. Vnb input pins are directly connected to a ladder resistor When Vna (n = 1, 7, 10, 16) is selected while RSEL = H, the input pins of Vnb (n = 1, 7, 10, 16) shall be open. When Vnb (n = 1, 7, 10, 16) is selected while RSEL = L or open, a Vna input pins shall be connected to a stable potential, for example, by aligning its potential to that of Vnb. During a grayscale output, keep the gray scale level power supply constant. As for power supply voltage and γ-corrected voltage, the following relationship shall be followed: VDD2 - 0.2 V≥V0> V1a or V1b > V2> V3 > V4 > V5 > V6 >V7a orV7b > V8≥0.5VDD2 0.5 VDD 2 ≥V9 > V10a or V10b > V11 > V12 > V13 > V14 > V15 > V16a or V16b >V17≥VSS2 + 0.2V (When there is an explanation irrespective of V*a or V*b In this specification table, one of them to be used is intended.)
TEST1, TEST2, TEST3	Test pin	I	When used, these pins must be open or L. These pins are pulled down to VSS1 within IC.
MON1, MON2, MON3, MON4	Monitor pin	-	The pins having same number n among MONn (n = 1 to 4) are connected in the wiring within an IC. (e.g.: pin 1 and pin 2 of MON1 are connected in an internal wiring.)
VDD1	Logic power supply	-	2.3 to 3.6 V
VDD2	Driver power supply	-	7.5 to 13.5V
VSS1	Logic ground	-	Grounding
VSS2	Driver ground		Grounding

Cautions:

1. The power shall be turned on in the following order: VDD1 → logic input → VDD2, γ –corrected power supply (V**), and for turning it off, reverse this sequence (VDD2 and V** must be applied concurrently).



2. To stabilize the supply voltage, it is recommended to insert a 0.1*μ*F bypass capacitor between VDD1 to VSS1 and VDD2 to VSS2 respectively. In addition, to increase the precision of a *D/A* converter, it is also recommended to insert a bypass capacitor of about 0.01 μF between γ-corrected power supply pins (V**) and VSS2.

IMPORTANT NOTICE

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