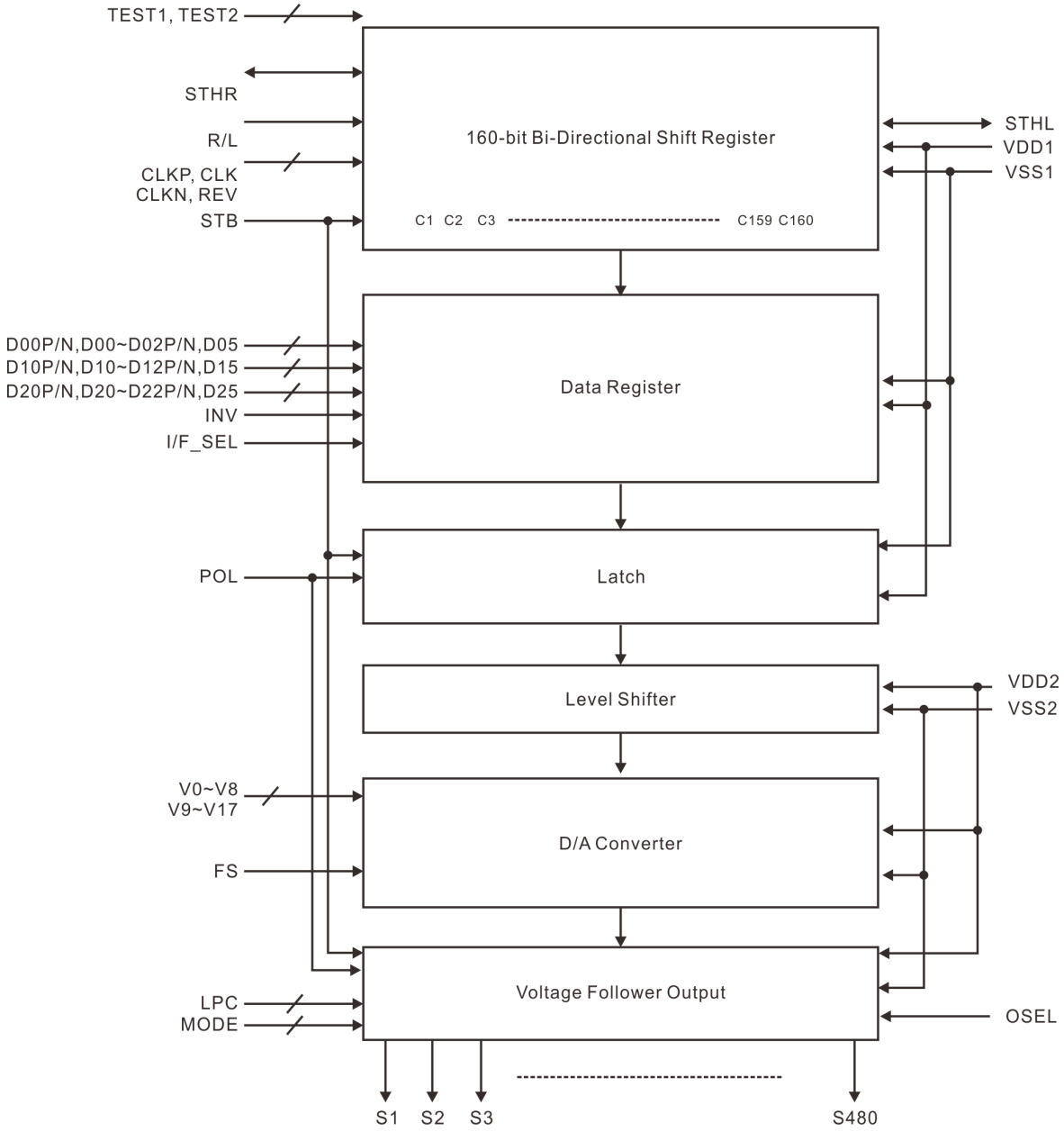
DESCRIPTION

The PT16103 is a CMOS silicon source driver IC for active matrix TFT LCD panels. After a CMOS/RSDS 6-bit RGB data is applied, this device will generate 64-gray scale for driving the TFT LCD panel source lines. It supports 480/402 channel selectable function, shift right/left selectable function, and cascade function for dot expansion.

FEATURES

- 64-gray scale source driver for active matrix TFT LCD panels
- Selectable 480/402 output channels
- Logic voltage power supply: 2.7V to 3.6V
- High voltage power supply: 7.0V to 13.5V
- Maximum RSDS operating frequency at 85 MHz
- Bi-directional shift right/left function
- COG package

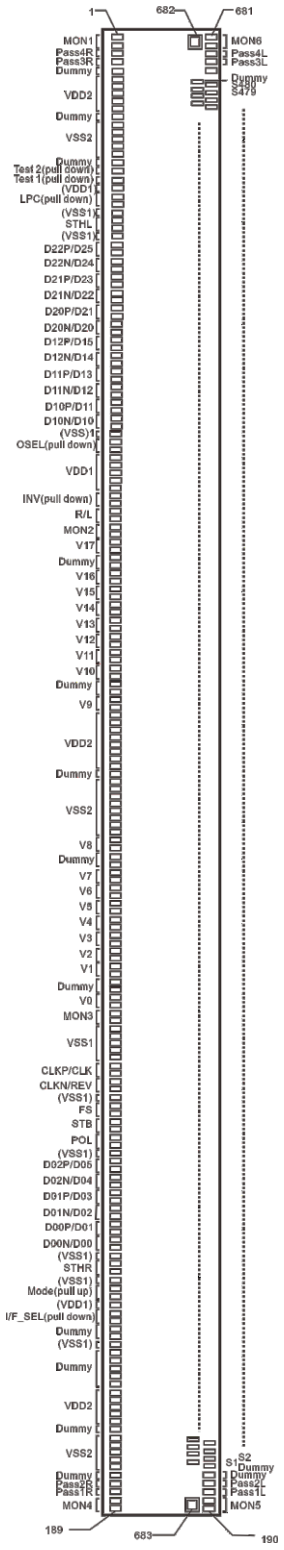
BLOCK DIAGRAM



1. ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT16103	COG	-

2. PIN CONFIGURATION



3. PIN DESCRIPTION

Symbol	Pin Name	I/O	Description
S1 to S480	Driver output	O	The D/A converted 64-qray-scale analog voltage is output.
I/F_SEL	Interface select	I	A setup of this pin performs IIF input mode change of this IC. When I/F_SEL pin = L or open, it becomes RSDS I/F mode. When I/F_SEL pin = H, it becomes CMOS I/F mode. This pin is pull downed to VSS1 inside IC. Cautions are required for the pin function and the electrical property of this IC to change with setup of this pin.
D00P/N, D00 to D02P/N, D05 D10P/N, D10 to D12P/N, D15 D20P/N, D20 to D22P/N, D25	Display data	I(Note)	The function of this pin changes with setup of I/F_SEL pin. When I/F_SEL pin = L or open, it becomes a display data input pin in RSDS I/F mode (D00 PIN. to D02P/N, D10P/N to D12P/N, D20P/N to D22P/N). Display data is inputted by the 9-bit width of the edge of double, i.e., gray-scale data (6 bits) x 3dots (1 pixel). When I/F_SEL pin = H, It becomes a display data input pin in CMOS I/F mode (D00 to D15, D10 to D15, D20 to D25). Display data is inputted by the 18-bit width of single edge, i.e.., gray-scale data (6 bits) x 3 dots (1pixel). D x 0: LSB, D x 5: MSB
CLKP, CLK, CLKN, REV	Shift clock, CMOS data inversion (REV)	I(Note)	The function of this pin changes with setup of I/F_SEL pin. When I/F_SEL pin = L or open, it becomes a shift clock input pin by the pair of CLKP and CLKN in the RSDS I/F mode. It is the shift clock input of a shift register. Display data is taken in to a data register by both the rising edge and the falling edge. When I/F_SEL pin = H, it is set to the CLK (shift clock input) input pin in CMOS I/F mode, and REV (inverted/not inverted selection signal of display input data). CLK takes in display data to a data register by the rising edge. REV: Performs being inverted/not inverted of D00-D05, D10-D15 and D20-D25 display data. REV = H: Display data is inverted inside IC. REV = L: Inversion of input data is not performed.
INV	RSDS data inversion	I(Note)	This is valid pin only at the time of I/F_SEL pin = L or Open. Inverted/not inverted selection of the display input data in RSDS I/F mode are selected. INV = H: Inverts data inside this IC INV = L: Inversion of input data is not perform Input DC signal into this pin. For more details, **Refer to DATA INVERSION** This pin is pull downed to VSS1 inside IC. Moreover, it becomes invalid when I/F_SEL pin = H(CMOS I/F mode). (As for the pull down of this pin, it exists also at the time of invalid).
R,/L	Shift direction control	I	These refer to the start pulse input/output pins when driver ICs is connected in cascade. The shift directions of the shift registers are as follows. R,/L = H: STHR input, S1→ S480, STHL output R,/L = L: STHL input, S480→S1, STHR output
STHR(CMOS)	Right shift start pulse	I/O	R,/L= H: Becomes the start pulse input pin R,IL = L: Becomes the start pules output pin
STHL(CMOS)	Left shift start pulse	I/O	R,/L = H: Becomes the start pules output pin R,/L= L: Becomes the start pulse input pin
STB(CMOS)	Latch	I	The contents of the data register are transferred to the latch circuit at rising edges. At the falling edge of STB, the gray scale voltage is supplied to the driver. It is necessary to input before start pulse input When there is no STB signal input and a start pulse is inputted continuously, loading the data based on a start pulse not performed.
POL(CMOS)	Polarity select	I	This is the output polarity selection input pin of a driver output. POL = H: S2n-1 output uses V0 to V8 as a reference power supply. The S2n output used V9 to V17 as the reference supply POL = L: S2n-1 output uses V9 to V17 as a reference power supply. The S2n output used V0 to V8 as the reference supply S2n-1 indicates odd output and S2n indicates the even output.

Symbol	Pin Name	I/O	Description
MODE(CMOS)	Output reset	I	The pin controls output reset function. MODE: H or OPEN: With output reset(during the STB=H period) MODE: L: No output reset This pin is pulled up to power supply VDD1 inside IC.
LPC(CMOS)	Low power control	I	<table><tr><td>LPC1</td><td>Driver Ability(reference ratio)</td></tr><tr><td>L or open</td><td>Large(100%)</td></tr><tr><td>H</td><td>Small(67%)</td></tr></table> This pin is pulled down to power supply VSS1 inside IC
OSEL(CMOS)	Output selection	I	Output channel numbers select pin. OSEL= L or Open: 480ch output OSEL = H: 402ch output (S205 to S282: Hi-Z) This pin is pulled down to power supply VSS1 inside IC
V0 to V8, V9 to V17	γ-corrected power supply	I	Input the γ-corrected power supply from outside by using operational amplifier. V_0, V_8, V_9, and V_{17} input pin are not connected to ladder resistance. V_1, V_7, V_{10}, and V_{16} input pin, the voltage follow circuit is attached to the inside of IC. V_2 to V_6, V_{10}, and V_{11} to V_{15} input pin are connected to ladder resistance directly. Make sure to maintain the following relationships. During the gray scale voltage output, be sure to keep the gray scale level power supply at a constant level. VDD2 - 0.1V ≥ V0> V1 > V2> V3 > V4 > V5 > V6 >V7 > V8≥0.5VDD2 0.5 VDD 2 ≥V9 > V10 > V11 > V12 > V13 > V14 > V15 > V16 >V17≥VSS2 + 0.1V
FS	Frame signal input	I	The offset cancellation start signal of the voltage follower circuit with which the inside of IC of gamma corrected power supply parts V1, V7 and V10 and V16 input pin is equipped is inputted. The input if one pulse is required for easy frame. Moreover, it is necessary to make in agreement the number of times of STB inputted in each frame. Refer to **SWITCHING CHARACTERISTIC** about timing etc.
VDD1	Logic power supply	-	2.7 to 3.6 V(Connect all pins)
(VDD1)	Pull for pull up	-	This pin is used when carrying out the pull-up of the adjoining functional setting pin. Leave it open at the time of intact.
VDD2	Driver power supply	-	7.0 to 13.5V(Connect all pins)
VSS1	Logic ground	-	Grounding(Connect all pins)
(VSS1)	Pull for pull up	-	This pin is used when carrying out the pull-down of the adjoining functional setting pin. Leave it open at the time of intact.
VSS2	Driver ground	-	Grounding(Connect all pins)
TEST1, TETS 2 (CMOS)	Test pin	I	TEST 1/2 = L or Open: Normal operation(Be sure to use it in the normal mode when this IC use) TEST 1/2 = H: Test mode This pin is pulled down to VSS1 inside IC
MON1 to MON6	Monitor pin	-	MONn(n=1 to 6) is connected between common in numbers.
PASSnR, PASSnL (n=1 to 4)	Pass pin	-	Wiring connection if between PASSnR and PASSnL (n=1 to 4) is made inside IC between each n number in agreement (Example: PASSnR and PASSnL are connected). And this pin is used for simple evaluations, such as contact resistance measurement of ACF. Therefore, the power supply relation and control signal which are used in LCD panel operation are not connectable. When this pin is unnecessary, leave this pin open.

Note: A pin function changes by setup of I/F_SEL pin.

IMPORTANT NOTICE

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