

## DESCRIPTION

PT2258 is a 6-Channel Electronic Volume Controller IC utilizing CMOS Technology specially designed for the new generation of AV Multi-Channel Audio System. PT2258 provides an I2C Control Interface, an attenuation range of 0 to -79dB at 1dB/step, low noise, and high channel separation. Housed in 20 pins, DIP or SOP, PT2258's pin assignments and application circuit are optimized for easy PCB Layout and cost saving advantages.

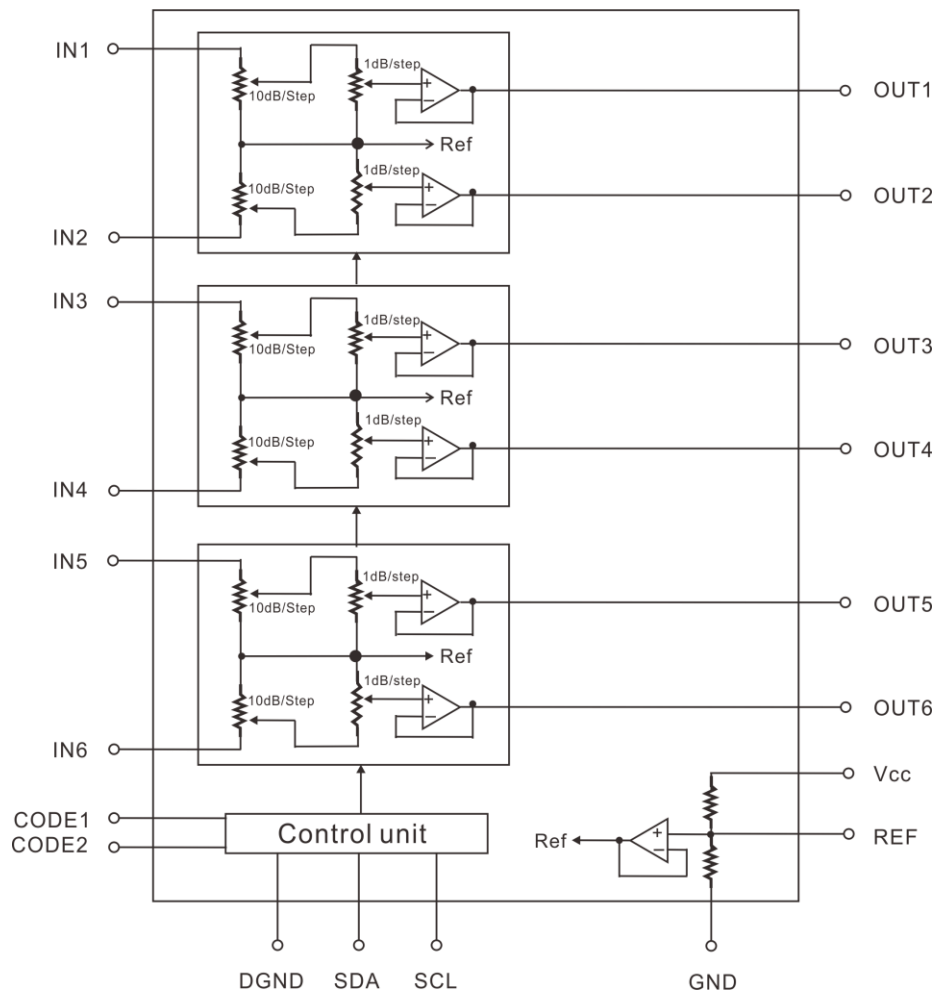
## APPLICATIONS

- AV Surround Audio Equipment
- Car Audio
- Mini Compo
- Computer Multi-Media Speaker
- Other Audio Equipments

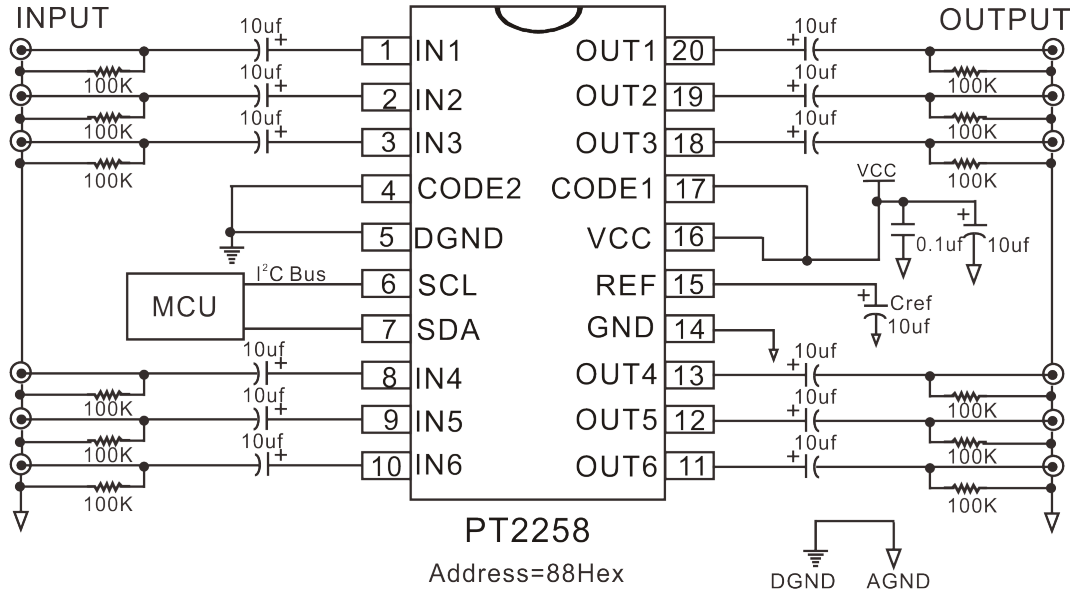
## FEATURES

- CMOS Technology
- Low Power Consumption
- Least External Components
- Attenuation Range: 0 to -79dB at 1dB/step
- Operating Voltage: 5 to 9 V
- Low Noise, S/N Ratio>100dB (A-weighting)
- High Channel Separation
- I2C Bus Control Interface
- Selectable Address
- 6-Channel Outputs
- Available in 20 pins, DIP or SOP

## BLOCK DIAGRAM



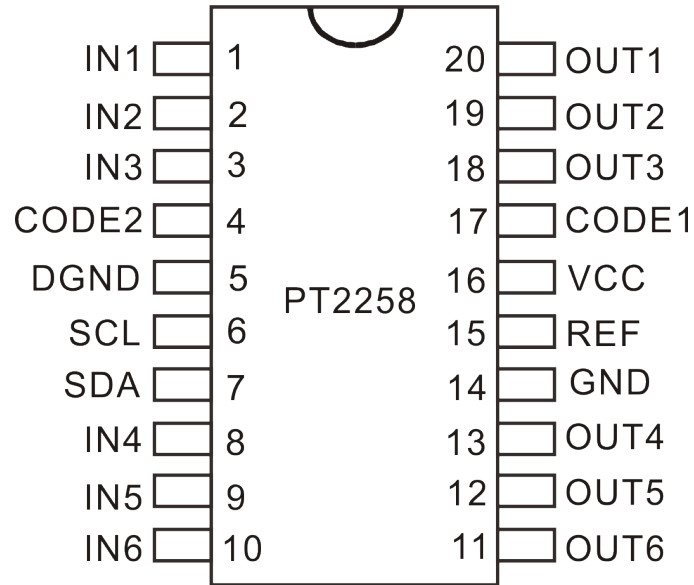
# APPLICATION CIRCUIT



## ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT2258	20 Pins, DIP, 300mil	PT2258
PT2258-S	20 Pins, SOP, 300mil	PT2258-S

## PIN CONFIGURATION



## PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
IN1	I	Channel Input No. 1. Connect a Capacitor to Audio Source	1
IN2	I	Channel Input No. 2 Connect a Capacitor to Audio Source	2
IN3	I	Channel Input No. 3 Connect a Capacitor to Audio Source	3
CODE2	-	Refer to Address Code Section	4
DGND	-	Digital Ground	5
SCL	I	I <sup>2</sup> C Clock Input	6
SDA	I	I <sup>2</sup> C Data Input	7
IN4	I	Channel Input No. 4 Connect a Capacitor to Audio Source	8
IN5	I	Channel Input No. 5 Connect a Capacitor to Audio Source	9
IN6	I	Channel Input No. 6 Connect a Capacitor to Audio Source	10
OUT6	O	Channel Output No. 6 Connect a Capacitor to the Next Stage	11
OUT5	O	Channel Output No. 5 Connect a Capacitor to the Next Stage	12
OUT4	O	Channel Output No. 4 Connect a Capacitor to the Next Stage	13
GND	-	Ground 14	14
REF	-	Reference Voltage= 1/2 Vcc Connect a Capacitor to the Ground	15
VCC	-	Power Supply Input 16	16
CODE1	-	Refer to the Address Code Section	17
OUT3	O	Channel Output No. 3 Connect a Capacitor to the Next Stage	18
OUT2	O	Channel Output No. 2 Connect a Capacitor to the Next Stage	19
OUT1	O	Channel Output No. 1 Connect a Capacitor to the Next Stage	20

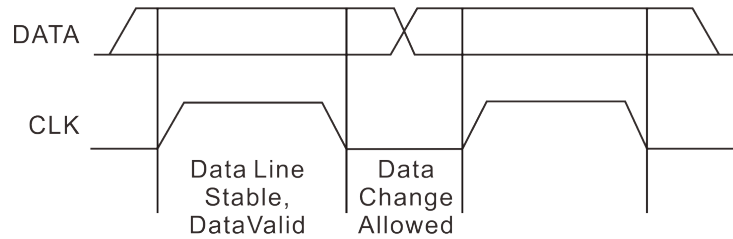
# FUNCTIONAL DESCRIPTION

## BUS INTERFACE

Data are transmitted to and from the microprocessor to the PT2258 via the SDA and SCL. The SDA and SCL make up the BUS Interface. It should be noted that the pull-up resistors must be connected to the positive supply voltage.

## DATA VALIDITY

A data on the SDA Line is considered valid and stable only when the SCL Signal is in HIGH State. The HIGH and LOW States of the SDA Line can only change when the SCL signal is LOW. Please refer to the figure below.



## START AND STOP CONDITIONS

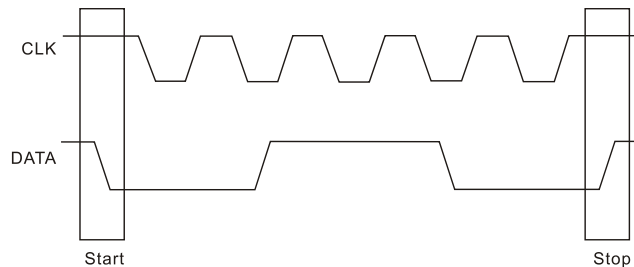
A Start Condition is activated when

- 1) the SCL is set to HIGH and
- 2) SDA shifts from HIGH to LOW State.

The Stop Condition is activated when

- 1) SCL is set to HIGH and
- 2) SDA shifts from LOW to HIGH State.

Please refer to the timing diagram below.



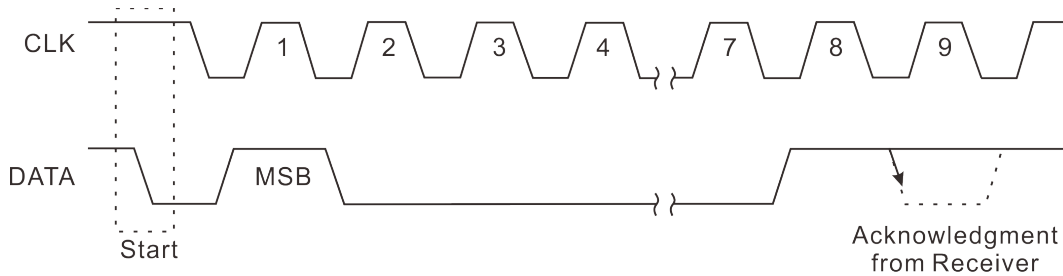
## BYTE FORMAT

Every byte transmitted to the SDA Line consists of 8 bits. Each byte must be followed by an Acknowledge Bit. The MSB is transmitted first.

## ACKNOWLEDGE

During the Acknowledge Clock Pulse, the master ( $\mu$ P) puts a resistive HIGH level on the SDA Line. The peripheral (audio processor) that acknowledges has to pull-down (LOW) the SDA line during the Acknowledge Clock Pulse so that the SDA Line is in a Stable Low State during this Clock Pulse. Please refer to the diagram below.

The audio processor that has been addressed has to generate an Acknowledge after receiving each byte, otherwise, the SDA Line will remain at the High Level during the ninth (9th) Clock Pulse. In this case, the master transmitter can generate the STOP Information in order to abort the transfer.



## TRANSMISSION WITHOUT ACKNOWLEDGE

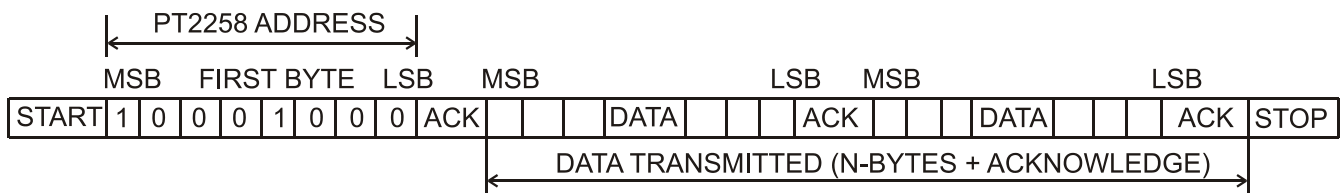
If you want to avoid the acknowledge detection of the audio processor, a simpler  $\mu$ P transmission may be used. Wait one clock and do not check the slave acknowledge of this same clock then send the new data. If you use this approach, there are greater chances of faulty operation as well as decrease in noise immunity.

## INTERFACE PROTOCOL

The interface protocol consists of the following:

- A Start bit
- A Chip Address Byte
- ACK=Acknowledge bit
- A Data byte
- A Stop bit

Please refer to the diagram below:



Notes:

1. ACK = ACKNOWLEDGE
2. MAX. CLOCK SPEED = 100K BITS/S

## PT2258 ADDRESS CODE

PT2258 Address Code depends on the state of CODE1 (Pin No.17) and CODE2 (Pin No.4).

If CODE1 or CODE2 is connected to Vcc, then CODE1 or CODE2 is set to "1". If CODE1 or CODE2 is connected to the Ground, it is set to "0". Please refer to the information below:

Condition 1:

CODE1	CODE2
1	1

Then, PT2258 Address Code is 8 CH:

1 MSB	0	0	0	1	1	0	0 LSB
----------	---	---	---	---	---	---	----------

Condition 2:

CODE1	CODE2
1	0

Then, PT2258 Address Code is 88 H:

1 MSB	0	0	0	1	0	0	0 LSB
----------	---	---	---	---	---	---	----------

Condition 3:

CODE1	CODE2
0	1

Then, PT2258 Address Code is 84 H:

1 MSB	0	0	0	0	1	0	0 LSB
----------	---	---	---	---	---	---	----------

Condition 4:

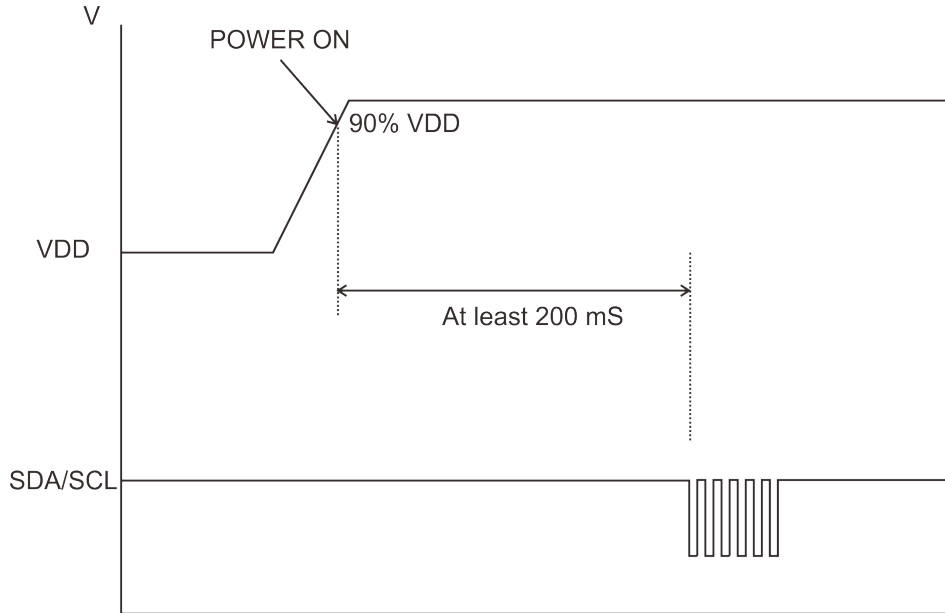
CODE1	CODE2
0	0

Then, PT2258 Address Code is 80H:

1 MSB	0	0	0	0	0	0	0 LSB
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## I<sup>2</sup>C BUS INTERFACE START TIME

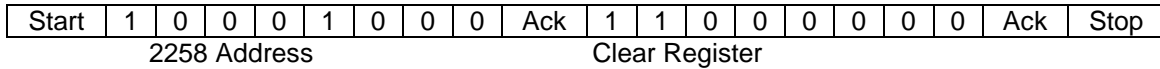
After Power is turned ON, PT2258 needs to wait for a short time in order to insure stability. The waiting time period for PT2258 to send I<sup>2</sup>C Bus Signal is at least 200ms. If the waiting time period is less than 200ms, I<sup>2</sup>C Control may fail. Please refer to the diagram below.





## PT2258 CONTROL SOFTWARE PROCEDURE

1. In order to ensure exact operation under any operating voltage, it is recommended an instruction to clear the register "C0H" must be transmitted first. Please refer to the following diagram:



2. The PT2258 function register does not have any default settings. After clearing the register, an initial value must send in order to each register. If a register does has not been set, it is possible that no sound will be output.

3. When adjusting the volume of PT2258, it is necessary to send a multiple of 10dB followed by a 1dB code to the attenuator in sequence. If this sequence is not followed, or if only a 10dB or 1dB value is sent, the IC may not operate normally. Please refer to the diagram below:

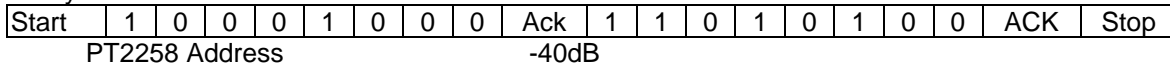
Volume setting -42dB :



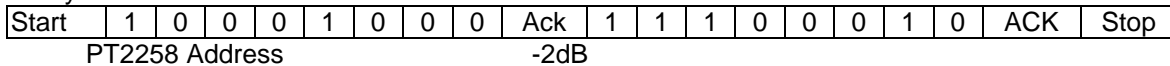
The two methods above are both acceptable.

**Warning!! The following transmission method is not permitted.**

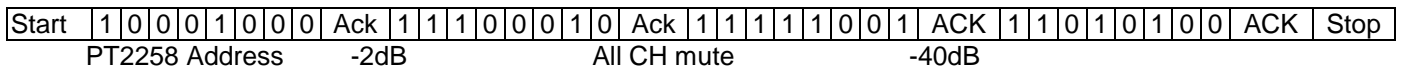
Send only a 10dB attenuation value:



Send only a 10dB attenuation value:



Do not send a 10dB code without simultaneously with a 1dB code or in combination with other instruction codes.



## DATA BYTES DESCRIPTION

### FUNCTION BITS

MSB							LSB	FUNCTION
1	1	1	0	A3	A2	A1	A0	6-Channel, -1dB/step
1	1	0	1	0	B2	B1	B0	6-Channel, -10dB/step
0	0	0	1	A3	A2	A1	A0	Channel No. 3, -1dB/step
0	0	0	0	0	B2	B1	B0	Channel No. 3, -10dB/step
0	0	1	1	A3	A2	A1	A0	Channel No. 4, -1dB/step
0	0	1	0	0	B2	B1	B0	Channel No. 4, -10dB/step
0	1	0	1	A3	A2	A1	A0	Channel No. 2, -1dB/step
0	1	0	0	0	B2	B1	B0	Channel No. 2, -10dB/step
0	1	1	1	A3	A2	A1	A0	Channel No. 5, -1dB/step
0	1	1	0	0	B2	B1	B0	Channel No. 5, -10dB/step
1	0	0	1	A3	A2	A1	A0	Channel No. 1, -1dB/step
1	0	0	0	0	B2	B1	B0	Channel No. 1, -10dB/step
1	0	1	1	A3	A2	A1	A0	Channel No. 6, -1dB/step
1	0	1	0	0	B2	B1	B0	Channel No. 6, -10dB/step
1	1	1	1	1	0	0	M	6-Channel, Mute When M= 1, MUTE ON When M=0, MUTE OFF

### ATTENUATION UNIT BIT

A3/---	A2/B2	A1/B1	A0/B0	Attenuation Value(dB)
0	0	0	0	0/0
0	0	0	1	-1/-10
0	0	1	0	-2/-20
0	0	1	1	-3/-30
0	1	0	0	-4/-40
0	1	0	1	-5/-50
0	1	1	0	-6/-60
0	1	1	1	-7/-70
1	0	0	0	-8/----
1	0	0	1	-9/----

Note: Ax=-1dB/step, Bx=-10dB/step

## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings	Unit
Vs	Supply Voltage	12	V
Topr	Operation Temperature	-40~+85	°C
Tstg	Storage Temperature	-65~+150	°C

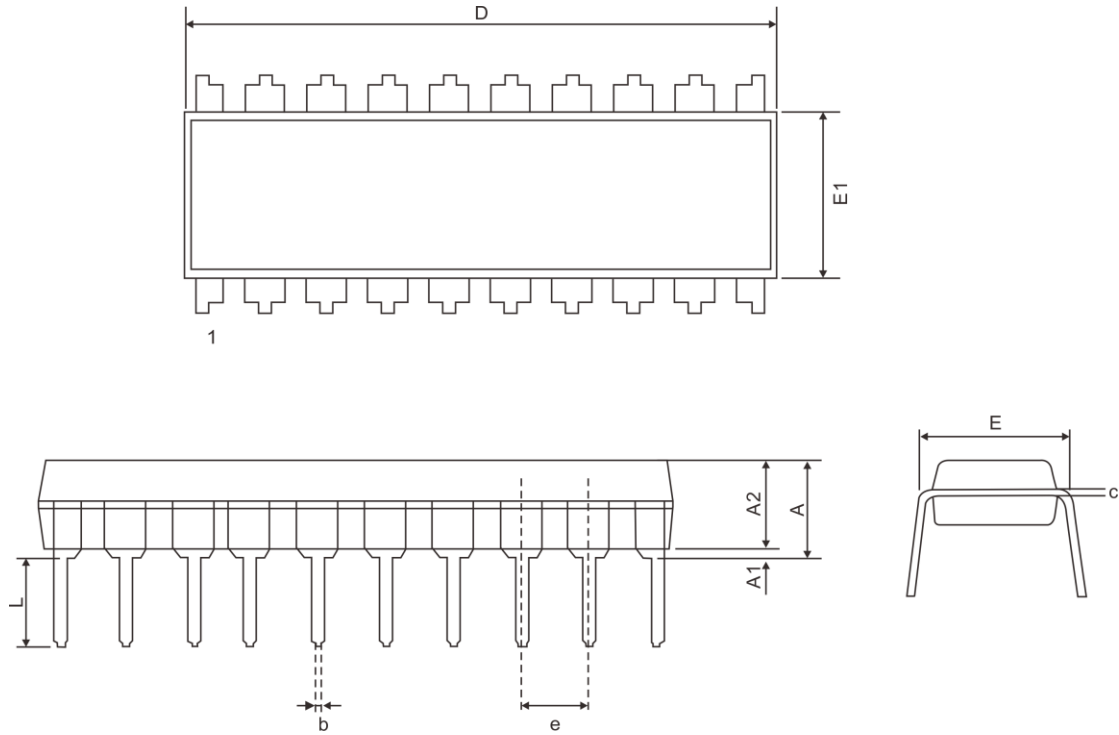
## ELECTRICAL CHARACTERISTICS

(VDD=9V, VI=1Vrms, f=1 KHz, Temp=27°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VDD	Supply Voltage		5	9	10	V
Is	Supply Current		7	10	12	mA
RIN	Input Impedance	FL, FR, CTR, SUB, SL, SR	22	33	42	KΩ
VCL	Max. Input Voltage	Volume=0dB, THD=1%		2.8	3.0	Vrms
Sc	Channel Separation		90	100	110	dB
Crange	Volume Control Range			79		dB
Avmax	Max. Attenuation			-79		dB
Astep	Attenuation Step			1		dB
EA	Attenuation Error	Volume=0~-50dB	-1.0	0	+1.0	dB
AMUTE	Mute Attenuation	A-weighting	90	95	98	dB
THD	Total Harmonic Distortion	Volume=0dB, input 200mVrms	0.003	0.005	0.01	%
Noise	Output Noise	A-weighting		3	5	μV
S/N	Signal-Noise Ratio	0dB=1Vrms, A-weighting	100	105	110	dB
Ro	Output Impedance			600	900	Ω
Go	Output Gain		-0.5	0	+0.5	dB
Vomax	Max. Output Voltage	FL, FR, CENTER, SUB, SL, SR THD=1%	2.3	2.5	2.8	Vrms
<b>I<sup>2</sup>C Section</b>						
VIL	Bus Low Input Level			2.4	2.5	V
VIH	Bus High Input Level		2.8	3.0		V
TINIT	Bus Initialization	Cref=10 μF		250	300	mS

# PACKAGE INFORMATION

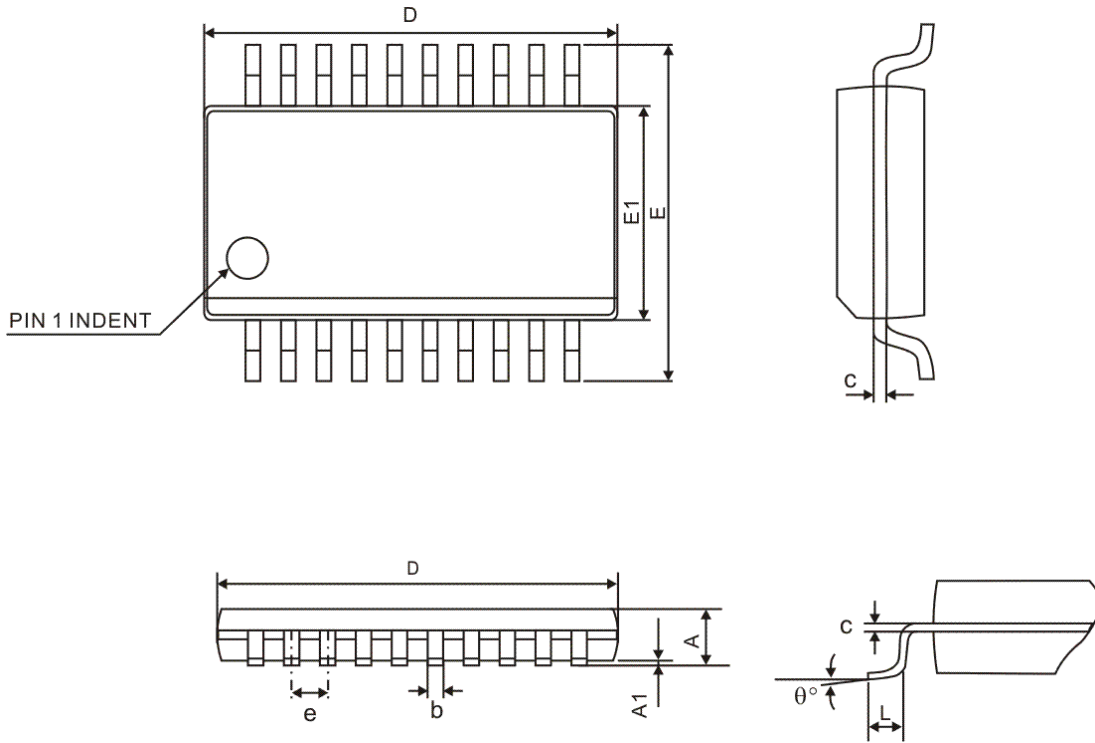
20 PINS, DIP, 300MIL



Symbol	Dimensions (mm)		
	Min.	Nom.	Max.
A	-	-	5.33
A1	0.38	-	-
A2	2.92	3.30	4.95
b	0.36	-	0.56
c	0.20	-	0.36
D	24.89	26.16	26.92
E	7.62BSC		
E1	6.10	6.35	7.11
e	2.54BSC		
L	2.92	-	3.81

- Notes:
1. Refer to JEDEC MS-001, Variation BA
  2. All dimensions are in millimeter

**20 PINS, SOP, 300MIL**



Symbol	Dimensions(mm)		
	Min.	Nom.	Max.
A	-	-	2.65
A1	0.10	-	0.30
b	0.31	-	0.51
c	0.20	-	0.33
e	1.27 BSC		
D	12.80 BSC		
E	10.30 BSC		
E1	7.50 BSC		
L	0.40	-	1.27
$\theta$	0°	-	8°

Notes:

1. Refer to JEDEC MS-013AC
2. All dimensions are in millimeter

## **IMPORTANT NOTICE**

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