

DESCRIPTION

The PT4301 is a very low power and highly sensitive single chip OOK/ASK super-heterodyne receiver for the 315MHz and 434MHz frequency bands that offers a high level of integration and requires only a few external components. The PT4301 consists of a low-noise amplifier (LNA), an image-rejection mixer, an on-chip phase-locked loop (PLL) with integrated voltage-controlled oscillator (VCO) and loop filter, a 10.7MHz intermediate frequency (IF) limiting amplifier stage with received-signal-strength indicator (RSSI), and analog baseband data recovery circuitry (data filter, peak detector, and data slicer). The PT4301 also implements a discrete one-step automatic gain control (AGC) that reduces the LNA gain by 20dB when the RF input signal is greater than -47dBm. The PT4301 is available in a 24-pin SSOP package.

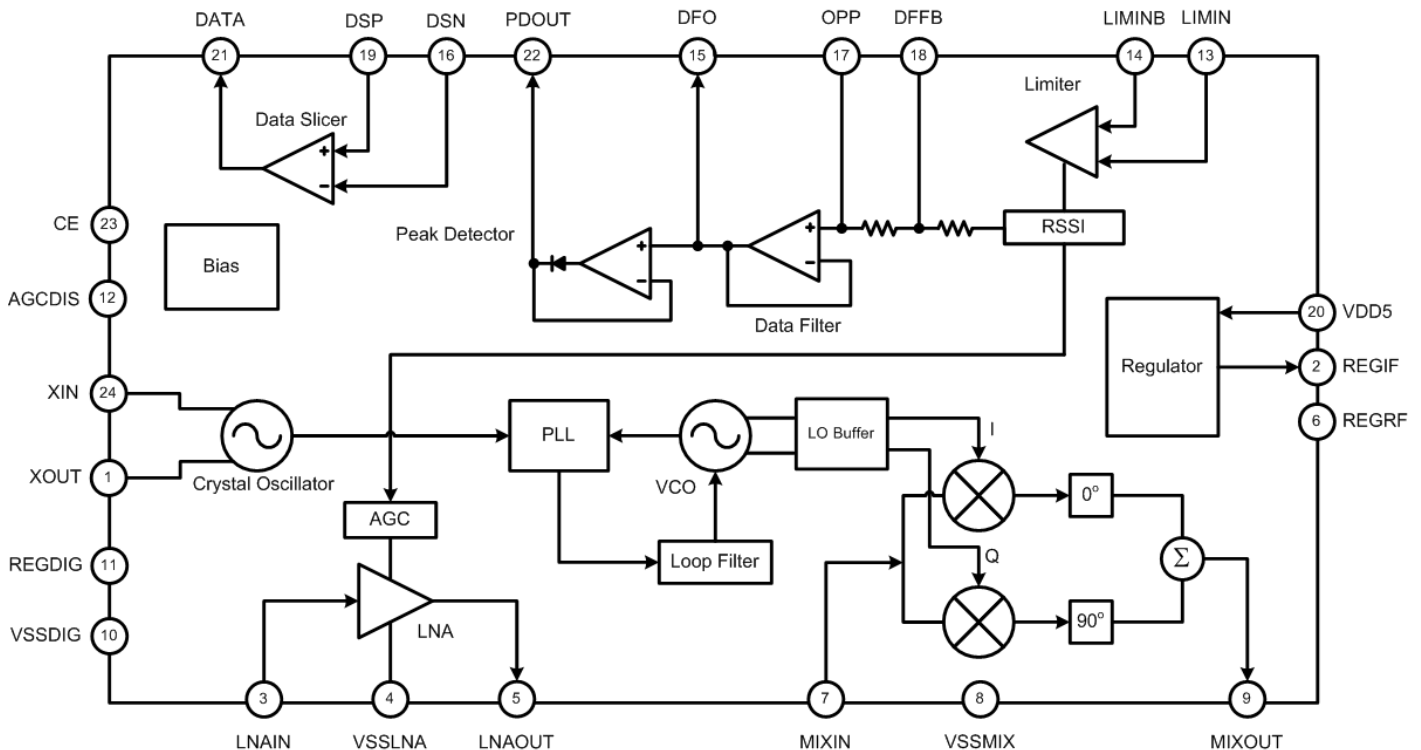
FEATURES

- Low current consumption (5mA fully active mode at 315MHz)
- 2.4V to 5.5V supply voltage operation range
- Optimized for 315MHz or 434MHz ISM Band
- On-chip image-rejection function
- High dynamic range with on-chip AGC
- Low power down mode current (<1μA)
- High sensitivity of -114dBm (315MHz, 2Kb/s AM 99% square-wave modulation)
- 24-pin SSOP package

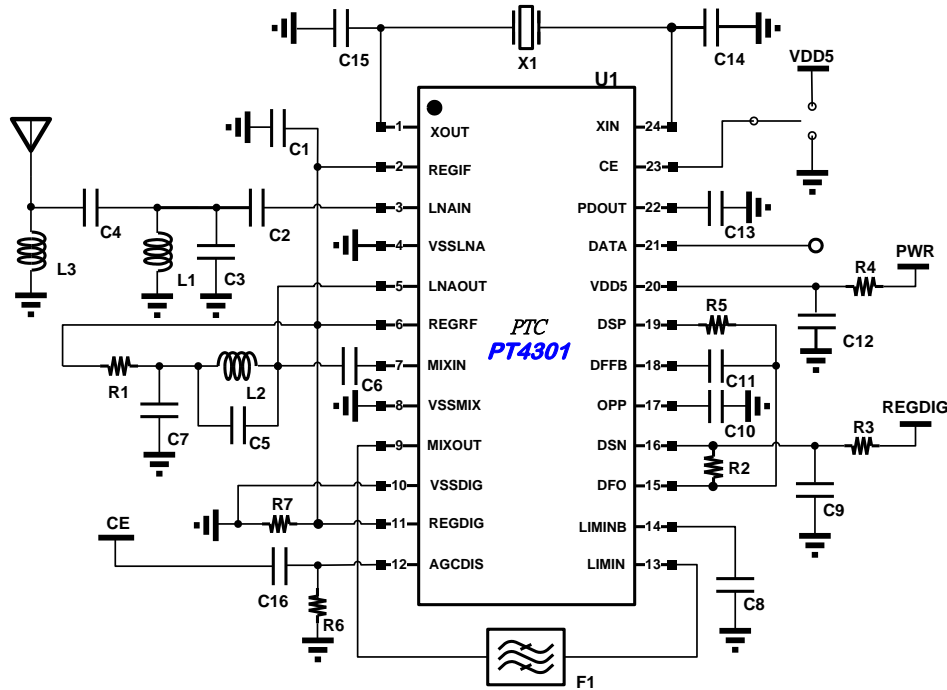
APPLICATIONS

- Remote keyless entry (RKE) systems
- Remote control systems including garage door and gate openers
- Alarm and security systems
- Wireless sensors

BLOCK DIAGRAM



APPLICATION CIRCUIT



BILL OF MATERIALS

Component	Value		Unit	Description
	315MHz	434MHz		
R1, R4	10	10	Ω	Power supply de-coupling resistors (option)
R2	27K	27K	Ω	Data filter to data slicer interface resistor
R3	8.2M	8.2M	Ω	Data slicer threshold adjustment (option)
R5	220K	220K	Ω	Data filter to data slicer interface resistor
R6	100K	100K	Ω	AGC disable
R7	5.6K	5.6K	Ω	REGDIS discharge resistor (option)
L1	68n	39n	H	LNA input matching, coil inductor
L2	47n	27n	H	LNA output matching
L3	39n	27n	H	Antenna ESD protection, coil inductor (option)
C1 ^{Note1} , C7, C12	100n	100n	F	Power supply de-coupling resistors
C2	10p	10p	F	LNA input matching
C3	-	-	F	LNA input matching (option)
C4	1.8p	1.2p	F	LNA input matching
C5	-	-	F	LNA output matching (option)
C6	100p	100p	F	LNA to mixer interface capacitor
C8	1.5n	1.5n	F	IF amplifier de-coupling capacitor
C9	470n	470n	F	Data slicer threshold charge capacitor
C10	390p	390p	F	Data filter capacitor
C11	1.2n	1.2n	F	Data filter capacitor
C13	-	-	F	Peak mode charge capacitor (option)
C14, C15	27p	27p	F	Crystal oscillator frequency fine tune capacitors
C16	100n	100n	F	AGC high gain mode quick start capacitor
F1 ^{Note2}	10.7	10.7	MHz	IF filter
X1	9.509	13.226	MHz	Reference crystal oscillator
U1	PT4301 IC	PT4301 IC	-	Receiver chip

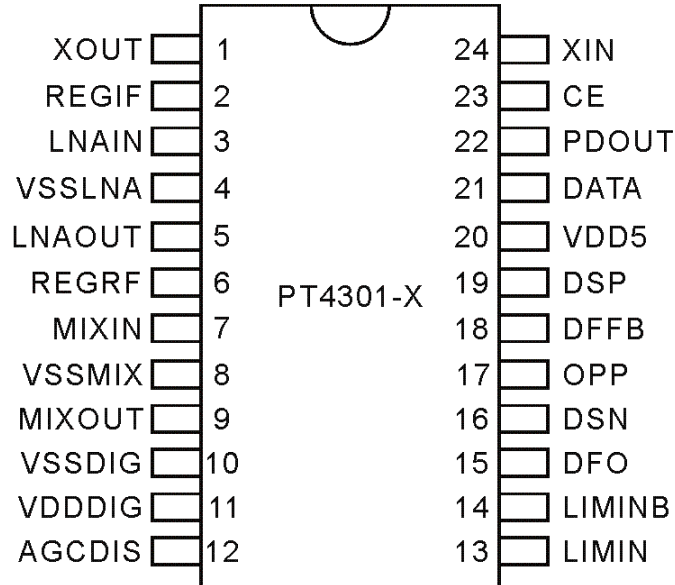
Notes:

1. C1 could be separated into three de-coupling capacitors and connect them against the three VDD pins as close as possible.
2. F1 is the 10.7MHz ceramic filter. The recommended part number is Murata SFELA10M7HA00-B0.

ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT4301-X	24 Pins, SSOP, 150mil	PT4301-X

PIN CONFIGURATION



PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
XOUT	O	Crystal oscillator output	1
REGIF	P	Supply voltage for IF portion	2
LNAIN	I	LNA input	3
VSSLNA	G	Ground for LNA	4
LNAOUT	O	LNA output	5
REGRF	P	Supply voltage for RF portion	6
MIXIN	I	Mixer input	7
VSSMIX	G	Ground for image-rejection mixer	8
MIXOUT	O	Mixer output	9
VSSDIG	G	Ground for LO and digital portions	10
REGDIG	P	Supply voltage for LO and digital portions	11
AGCDIS	I	AGC control pin. Pull high (connect to VDD5) to disable AGC	12
LIMIN	I	Limiting amplifier input	13
LIMINB	I	Limiter amplifier de-coupling input	14
DFO	O	Data filter output	15
DSN	I	Negative data slicer input	16
OPP	I	Non-inverting op-amp input for Sallen-Key data filter	17
DFFB	I/O	Data filter feedback node	18
DSP	I	Positive data slicer input	19
VDD5	P	5V supply voltage	20
DATA	O	Data output	21
PDOUT	O	Peak detector output	22
CE	I	Chip enable pin. Pull high (connect to VDD5) to power on the chip	23
XIN	I	Crystal oscillator input	24

Note: Pin 13 and Pin 14 are identical pins. Users can choose either pin as the limiting amplifier input and treat the other pin as the de-coupling input.

IMPORTANT NOTICE

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