

DESCRIPTION

The PT4330 is a low power 315/433/868/915MHz FM/FSK receiver IC which is suitable for use in the North American 315/915MHz and the European 433/868MHz ISM bands. The PT4330 chip consists of a low-noise amplifier (LNA), a down-conversion mixer, a 10.7MHz intermediate frequency limiting amplifier stage with received-signal-strength indicator (RSSI), a quadrature demodulator, and a selectable audio amplifier/slicing comparator. It also integrates a VCO with fixed $\div 64$ prescaler, phase/frequency detector, and reference oscillator forming complete phase-locked loop.

The PT4330 is available in 32-pin TQFP package, and is specified over the extended temperature range from -10°C to $+70^{\circ}\text{C}$.

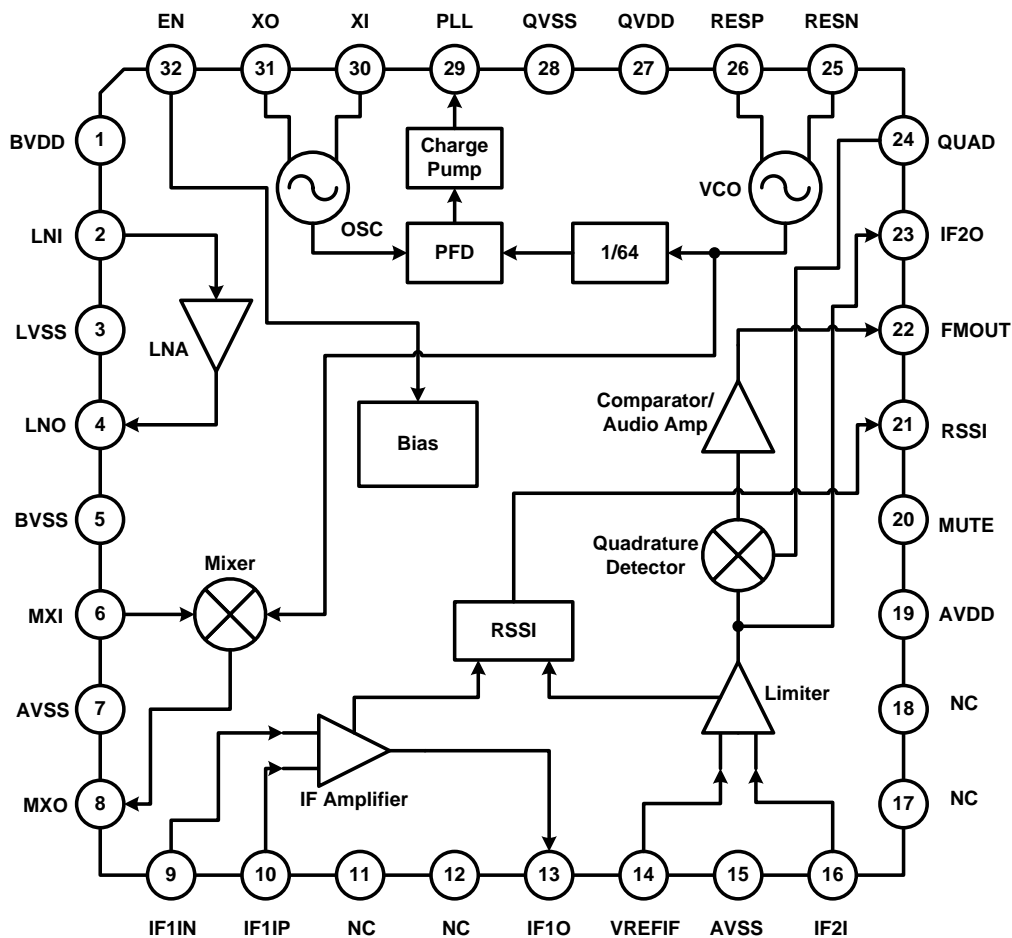
FEATURES

- Supply voltage range from 2.4V to 3.6V
- Low power consumption of 7.5mA for fully operation at 915MHz
- Excellent FSK sensitivity of the order of -100dBm (180KHz channel bandwidth and 0.1% BER)
- Reduced peripheral components
- Fixed RSSI response with 64dB dynamic range in both FM and FSK modes
- Receiver enable pin for power saving ($1\mu\text{A}$ current consumption in stand-by mode)
- TQFP 32L package (5mm x 5mm)

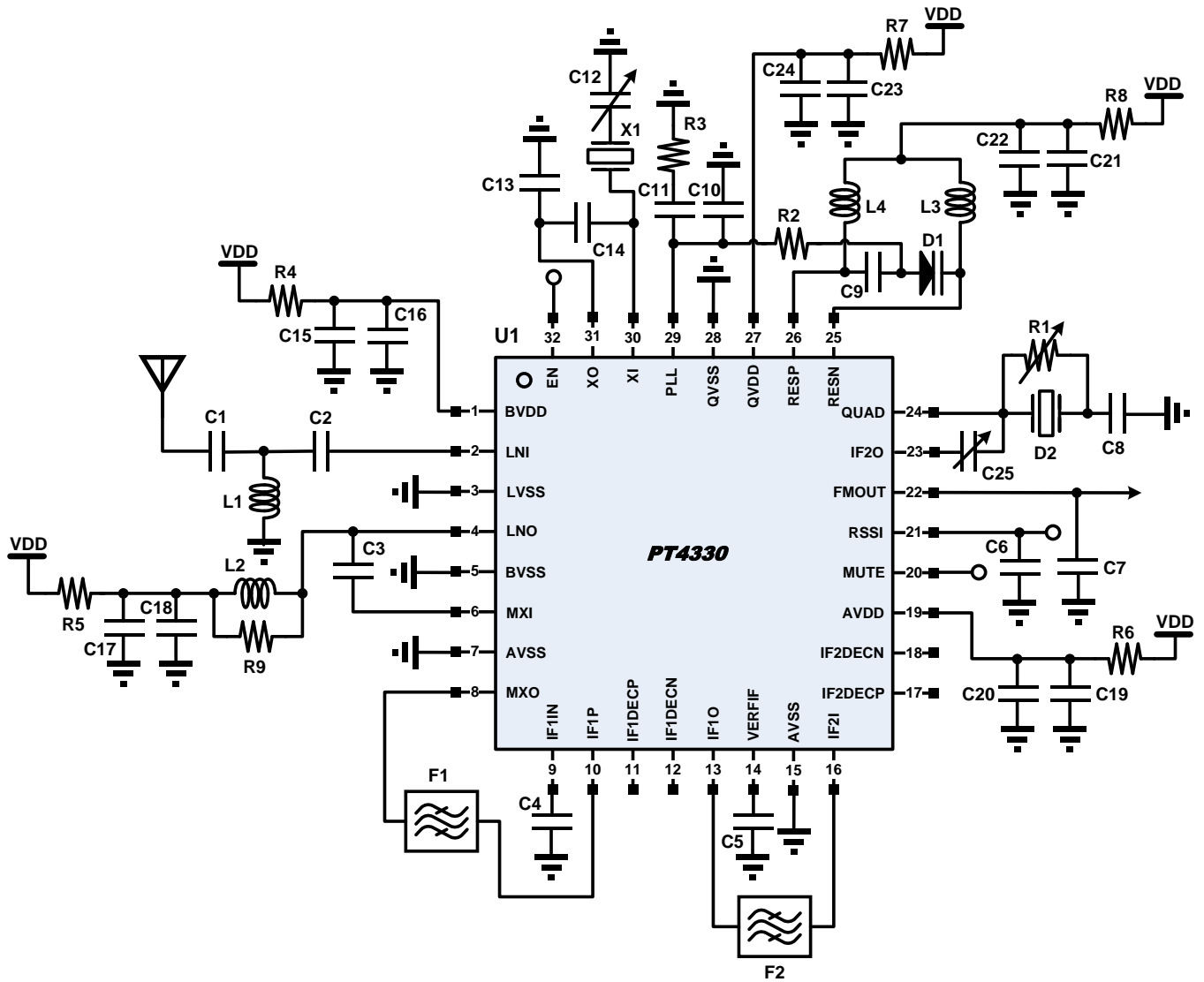
APPLICATIONS

- Wireless mouse / joystick
- Wireless voice transmission
- Wireless car alarm system

BLOCK DIAGRAM



APPLICATION CIRCUIT



BILL OF MATERIALS

Part	Value				Unit
	315MHz	434MHz	868MHz	915MHz	
C1	3.9p	1.5p	1.5p	1.0p	F
C2	33p	22p	18p	15p	F
C3	4.7p	3.9p	1.8p	1.5p	F
C4		—	—	—	F
C4/C5/C8	10n	10n	10n	10n	F
C6 ^{Note1}	10n	10n	10n	10n	F
C7	180p	180p	180p	180p	F
C9	8.2p	4.7p	3.3p	3.9p	F
C10	3.3n	3.3n	3.3n	3.3n	F
C11	47n	47n	47n	47n	F
C12/C25 ^{Note1}	—	—	—	—	F
C13/C14	39p	39p	39p	39p	F
C15/C17/C19/C21/C23	10n	10n	10n	10n	F
C16/C18/C20/C22/C24	47p	47p	27p	22p	F
L1	47n	33n	10n	10n	H
L2	68n	39n	12n	8.2n	H
L3/L4	27n	18n	4.7n	3.3n	H
R1	5.6K	5.6K	5.6K	5.6K	Ω
R2	10K	10K	10K	10K	Ω
R3	2.7K	2.7K	2.7K	2.7K	Ω
R4/R5/R6/ R7	10	10	10	10	Ω
R8	27	27	27	27	Ω
R9	560	—	—	—	Ω
F1/F2 ^{Note2}	10.7MHz Ceramic Filter				—
X1 (crystal)	4.755	6.613	13.41	14.15	MHz
D1 ^{Note3}	BB833	BB833	SMV1233	SMV1233	—
D2 ^{Note4}	10.7MHz FM Discriminator				—
U1	PT4330 IC				—

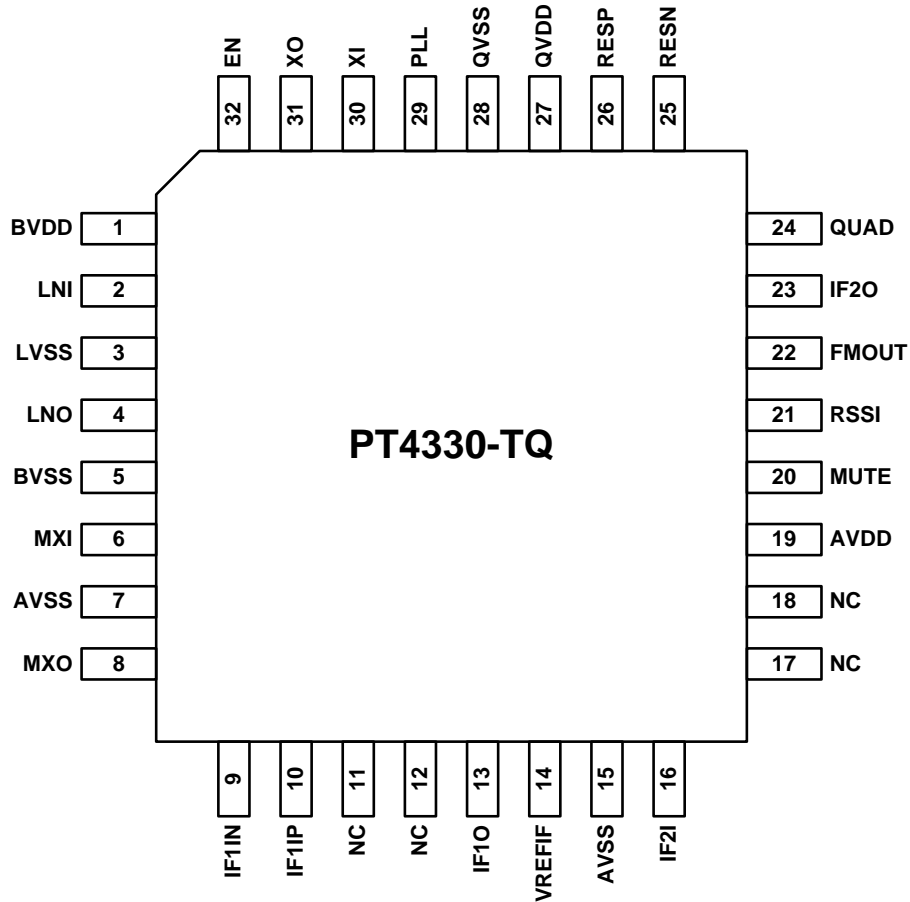
Notes:

1. C6 (RSSI bypassing capacitor), C12 (crystal trimming capacitor) and C25 (quadrature detector trimming capacitor) are not the necessary components for practical applications. Customers can consider to use or to tune these components by their applications.
2. F1 is the 10.7MHz ceramic filter. The recommended part number is Murata SFELA10M7HA00-B0.
3. D1 is varactor. The recommended part number is Alpha SMV1133-011
4. D2 is 10.7MHz FM Discriminator. The recommended part number is Murata CDALA10M7GA001-B0.

ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT4330-TQ	32 Pins, TQFP	PT4330-TQ

PIN CONFIGURATION



PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
BVDD	P	Nominal 3.6V supply for receiver front-end	1
LNI	I	Low noise amplifier input	2
LVSS	G	Ground for low noise amplifier	3
LNO	O	Low noise amplifier output	4
BVSS	G	Ground for receiver front-end	5
MXI	I	Mixer input	6
AVSS	G	Ground for baseband strip	7
MXO	O	Mixer output	8
IF1IN	I	Complementary IF amplifier input (330Ω input impedance; requires bypassing)	9
IF1IP	I	IF amplifier input (330Ω input impedance; requires ac-coupling)	10
NC	—	Non-connection pin	11
NC	—	Non-connection pin	12
IF1O	O	IF amplifier output	13
VREFIF	I	Complementary limiting amplifier input (330Ω input impedance; requires bypassing)	14
AVSS	G	Ground for baseband strip	15
IF2I	I	Limiting amplifier input (330Ω input impedance; requires ac-coupling)	16
NC	—	Non-connection pin	17
NC	—	Non-connection pin	18
AVDD	P	Nominal 3.6V supply for baseband strip	19
MUTE	I	Tri-state logic input to control FMOUT output (MUTE = high = output off; MUTE = low = FSK output; MUTE = floating = FM output)	20
RSSI	O	Received signal strength indicator voltage	21
FMOUT	O	FM amplifier/FSK comparator output	22
IF2O	O	Limiting amplifier output	23
QUAD	I/O	Quadrature demodulator input	24
RESN	I	Complementary open collector VCO output	25
RESP	I	Open collector VCO output	26
QVDD	P	Nominal 3.6V supply for phase-locked loop	27
QVSS	G	Ground for phase-locked loop	28
PLL	I/O	PLL charge pump output	29
XI	I	Oscillator input (base)	30
XO	O	Oscillator output (emitter)	31
EN	I	Chip enable control (RXEN = high = normal operation; RXEN = low = stand-by mode)	32

IMPORTANT NOTICE

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