Tel: 886-2-66296288
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DESCRIPTION

PT8300 is an I/O expander utilizing CMOS technology providing 16 bits serial input-parallel output and 8 bits parallel input-serial output shift register function. 8 input pins or 16 output pins can be configured to a cascading or parallel structure. Reading of serial data during the parallel to serial data conversion is enabled by the built-in independent registers for serial input to parallel output and parallel input to serial output. Housed in 28 pins, SOP Package, PT8300 provides 8 input or 16 output pins which can be configured into a cascading structure. Pin assignments and application circuits are optimized for easy PCB layout and cost saving benefits.

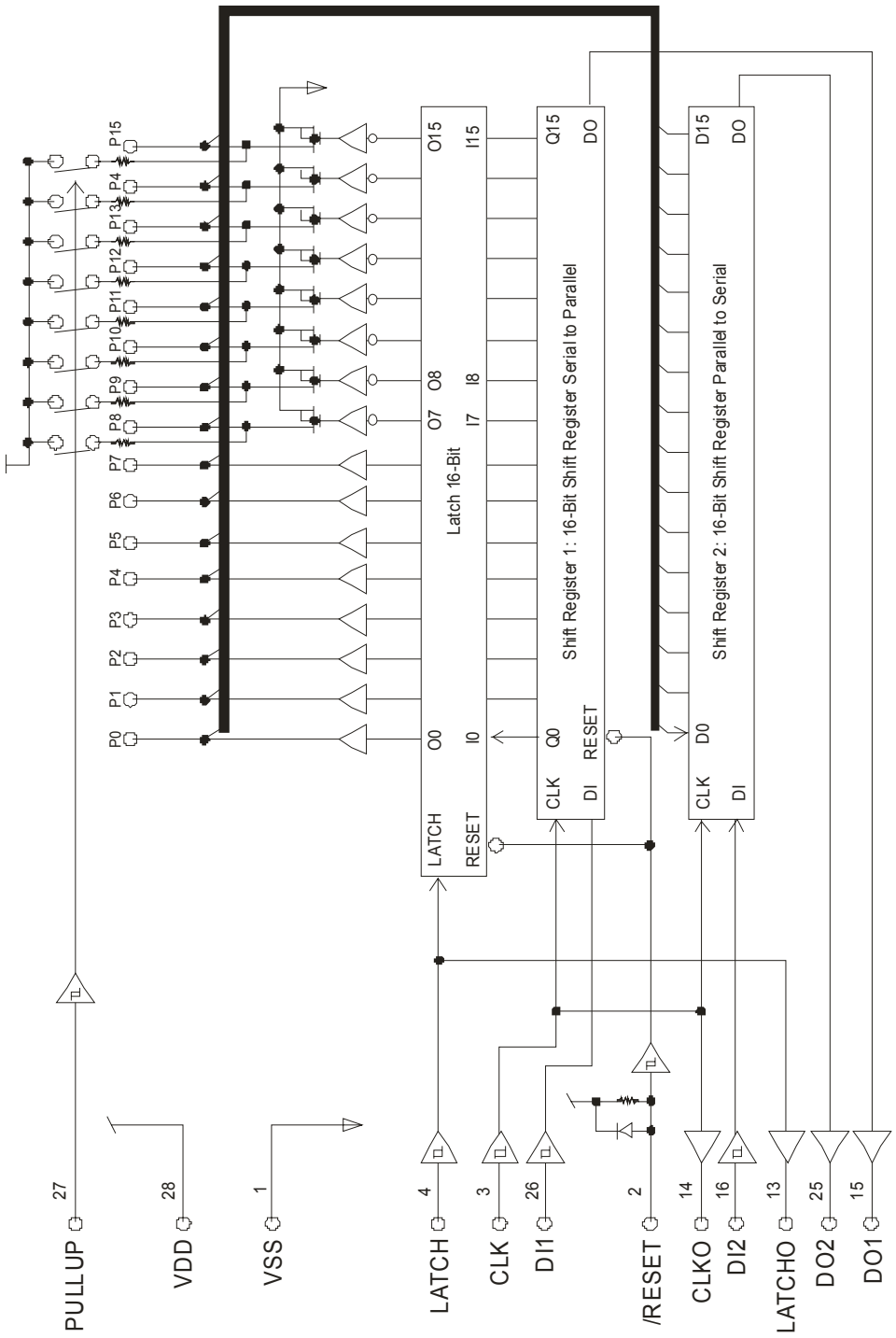
FEATURES

- CMOS technology
- Low power consumption:
  - Wide operating supply voltage range: V_{DD}=3 to 5.5V
  - Wide operating temperature range: Ta=-20 to +75℃
- Reading of the serial data during parallel to serial data conversion
- 8 output pins or 8 input/output pins provided
- Schmitt triggered inputs (DI1,DI2,CLK,LATCH, /RESET,PULLUP)
- Parallel data inputs provided (P8 to P15)
- Open drain with selectable pull up resistance ports provided (P8 to P15)
- Normal output ports provided (P0 to P7)
- Port extension is supported

APPLICATIONS

- MCU peripheral device
- Serial bus system data communication

BLOCK DIAGRAM



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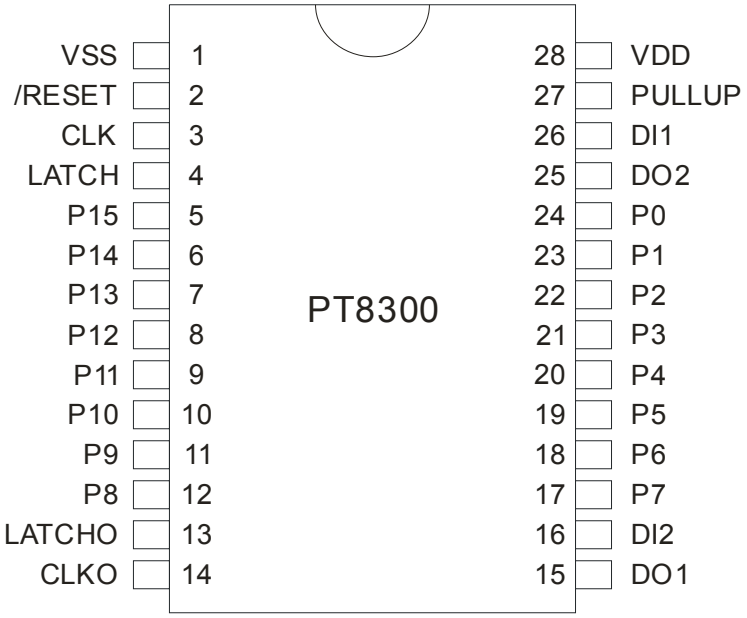
PIN CONFIGURATION



PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
VSS	-	Ground	1
/RESET	I	Reset pin (Active: Low)	2
CLK	I	Clock input pin	3
LATCH	I	Latch input pin	4
P15 ~ P8	I/O	Parallel data input/output pins	5 ~ 12
LATCHO	O	Latch output pin	13
CLKO	O	Clock output pin	14
DO1, DO2	O	Serial data output pins	15, 25
DI1, DI2	I	Serial data input pins	26, 16
P7 ~ P0	O	Parallel data output pins	17 ~ 24
PULLUP	I	P8 to P15 control pin for internal resistor When P8 to P15 are in the output state, the PULLUP pin must be connected to VDD. When P8 to P15 are in the input state, the PULLUP pin must be connected to VSS.	27
VDD	-		28