

DESCRIPTION

PT16528 is a LCD segment driver with 4 backplane and 18 segment-driver outputs, with either an I²C interface. It comprises an internal oscillator, bias generation, instruction decoding, and display controller.

FEATURES

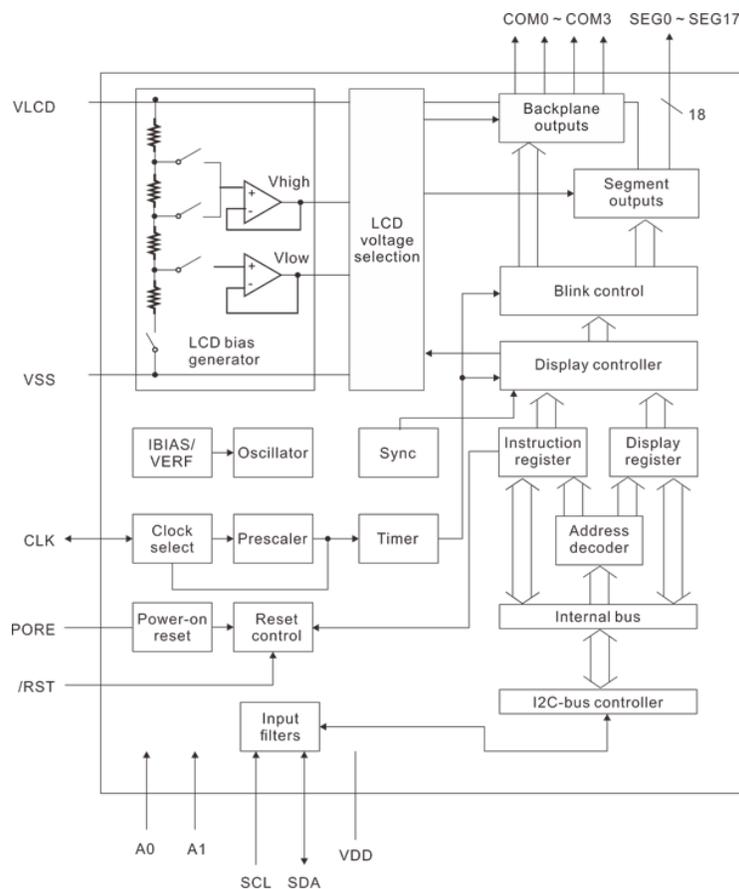
- AEC-Q100 grade 2 compliant for automotive applications
- Single chip LCD controller and driver
- Selectable backplane drive configuration: static, 2, 3, or 4 backplane multiplexing
- Selectable display bias configuration: static, 1/2, or 1/3
- Internal LCD bias generation with buffers
- 18 Segment drives:
 - Up to 9 "7-segment" numeric characters
 - Up to 4 "14-segment" alphanumeric characters
 - Any graphics of up to 72 segments/elements

- Auto-incrementing display data and instruction loading
- Versatile blinking modes
- Independent supplies of VLCD and VDD
- Power supply ranges:
 - 3.3 V to 6.0 V for VLCD
 - 2.7 V to 6.0 V for VDD
- 1MHz I²C-bus interface
- Internally generated or externally supplied clock signal

APPLICATIONS

- Small displays integrated
 - in a car instrument cluster
 - in a control knob

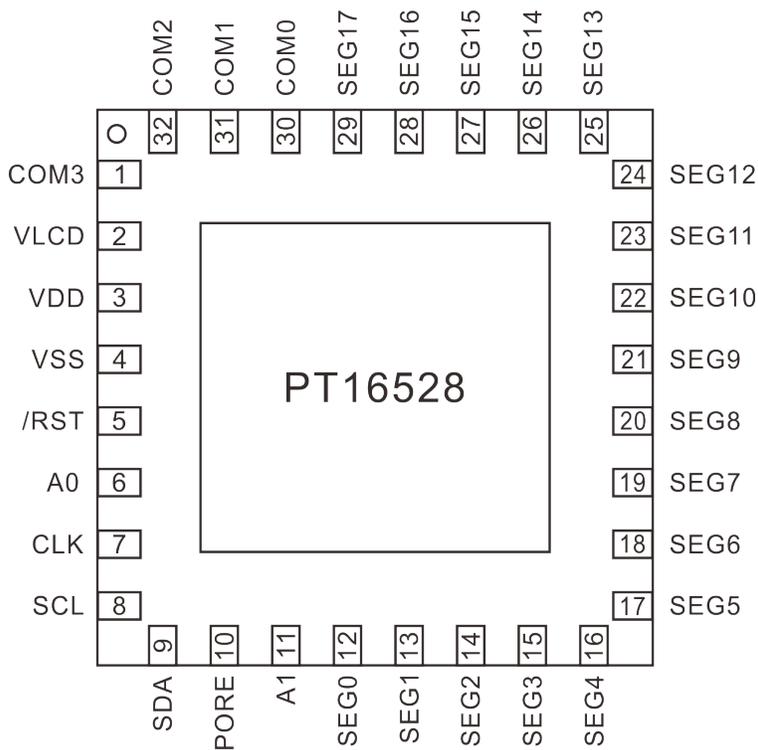
BLOCK DIAGRAM



ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT16528	32-Pin, QFN	PT16528

PIN CONFIGURATION



PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
COM3	O	LCD backplane output	1
VLCD	-	LCD supply voltage	2
VDD	-	Supply voltage	3
VSS	-	Ground supply	4
/RST	I	Reset input, active LOW	5
A0	I	Hardware device address selection - Connect to VSS = logic 0 - Connect to VDD = logic 1	6
CLK	I/O	Internal oscillator output external oscillator input - Must be left open if unused	7
SCL	I	Serial clock input	8
SDA	I/O	Serial data I/O	9
PORE	I	Power-on reset (POR) enable - Correct to VDD for enabling POR - Correct to VSS for disabling POR	10
A1	I	Hardware device address selection: - Connect to VSS = logic 0 - Connect to VDD = logic 1	11
SEG0 ~ SEG17	O	LCD segment outputs	12 ~ 29
COM0 ~ COM2	O	LCD backplane outputs	30 ~ 32
Heatsink	-	Connected to VSS is recommended.	back-side

IMPORTANT NOTICE

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