

## DESCRIPTION

The PT12477 is a monolith integrated motor driver designed for printers, scanners, and home or office automated equipment. The dual H-bridge drivers are consisting by all of N-channel MOSFETs, and designed to drive a 4-wires bipolar stepper motor. The output driving current of the PT12477 allows up to 1.6 Amps (mounted on dual layer PCB with proper heatsinking,  $V_M=24V$ ,  $T_A=25^\circ C$ ).

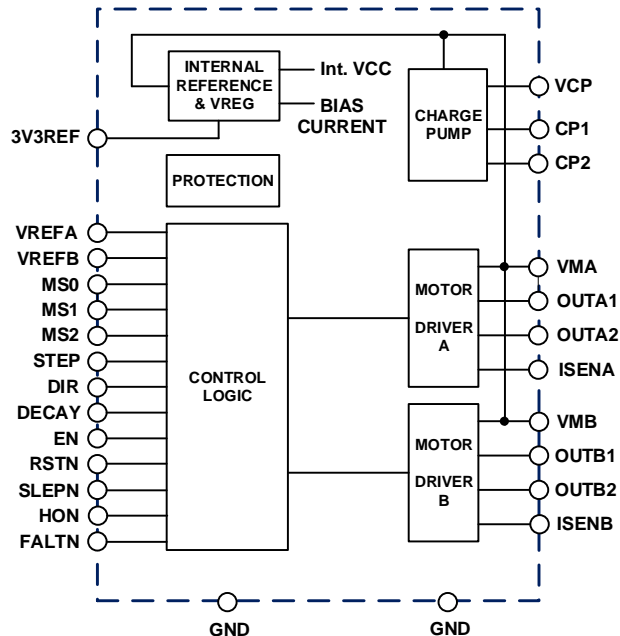
To simplified control interface, the STEP and DIR pins allows easy communicates with micro controller, Three Mode Select pins allow for configuration the micro steps from full-step divides to 1/32 micro-step. 3 kind of winding current decay modes are configurable to keeps motor not missing step and low current ripple. A low-power sleep mode is provided which shuts down internal circuitry to achieve very-low quiescent current draw. This sleep mode can be sets by SLEPN pin.

The PT12477 is available in 28-pins HTSSOP or 28-pins QFN package, both packages with thermal pad.

## APPLICATIONS

- Automatic teller machines
- Video security cameras
- Printers
- Scanners
- Office automation machines
- Amusement machines
- Factory automation
- Robotics

## BLOCK DIAGRAM

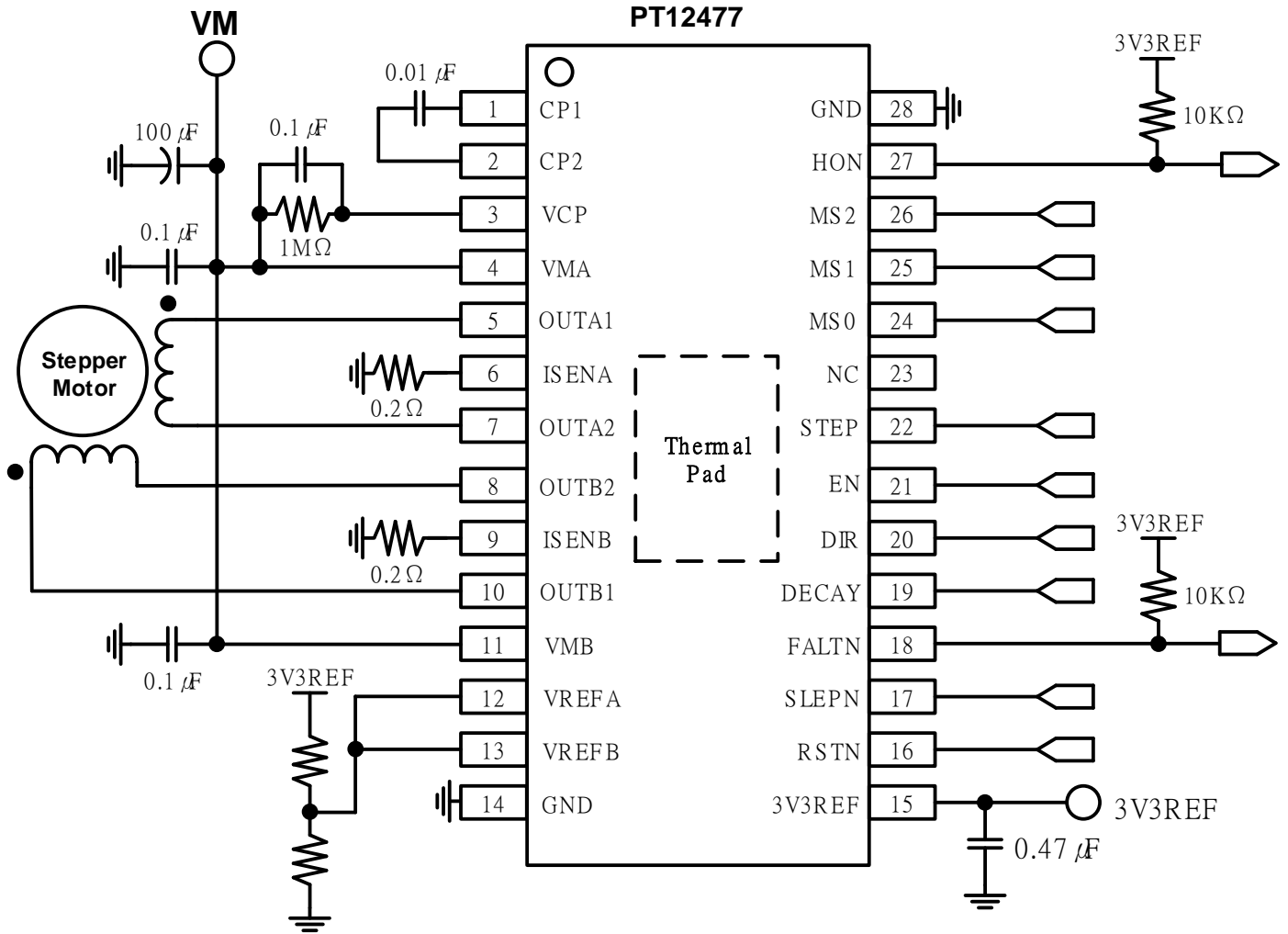


## FEATURES

- Automotive AEC-Q100 Grade 1 ( $-40^\circ C \sim +125^\circ C$ ) Qualified.
- 8V to 36V supply voltage range
- 1.6-A maximum driving current at  $V_M=24V$  (with additional heatsink)
- Dual H-bridge driver for bipolar stepper motor with such features:
  - PWM chopping constant current regulation
  - Built-In micro stepping sequencer
  - Multiple micro steps, Full, 1/2, 1/4, 1/8, 1/16 and up to 1/32 steps
- STEP and DIR logic inputs can control stepping motor revs and direction.
- Winding current decay modes
  - Mixed Decay
  - Slow Decay
  - Fast Decay
- Built In a 3.3V reference voltage output
- Low-power sleep mode
- Protection features
  - Over current protection (OCP)
  - Thermal shutdown (TSD)
  - VM under voltage lock out (UVLO)
  - Fault indication pin (FALTN)

**PT12477**

# APPLICATION CIRCUIT



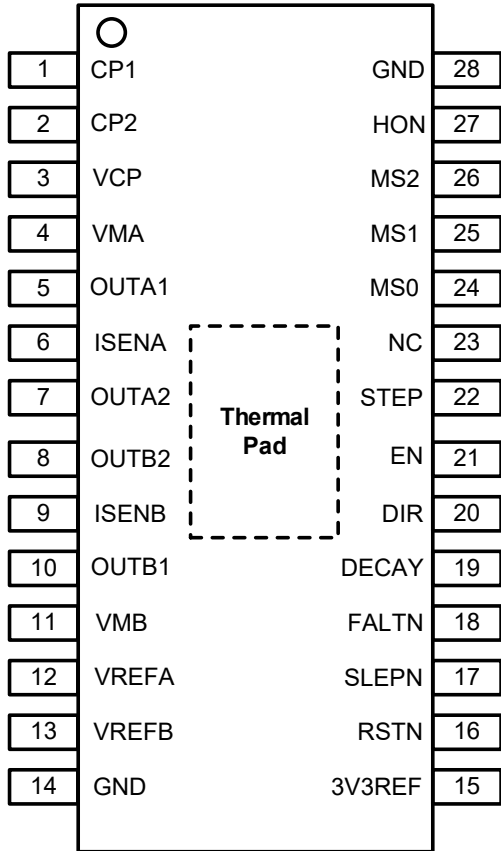
(HTSSOP-28 package for example)

## ORDER INFORMATION

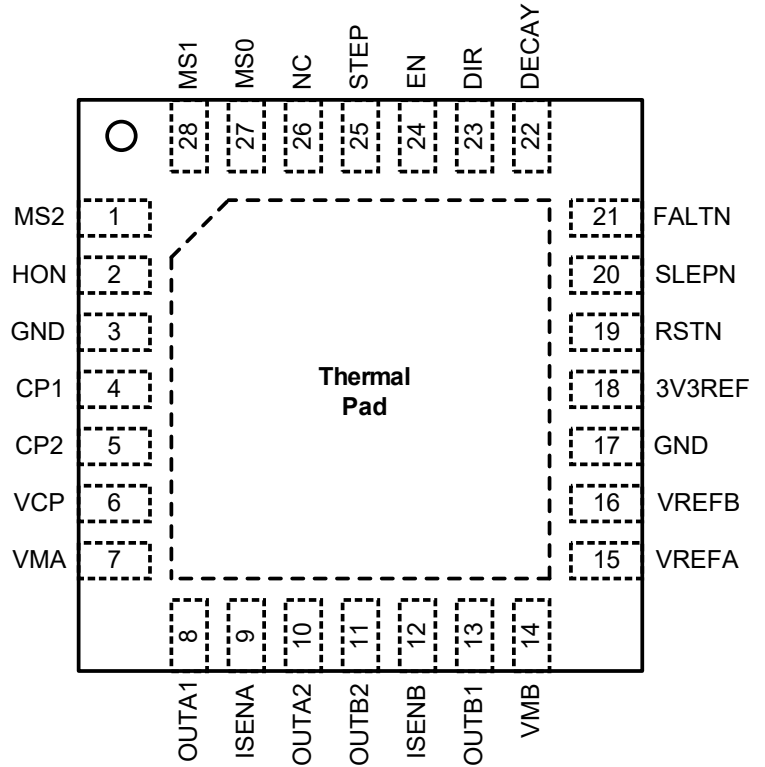
Valid Part Number	Package Type	Top Code
PT12477-HT	28 Pins, HTSSOP	PT12477-HT
PT12477	28 Pins, QFN	PT12477

# PIN CONFIGURATION

**PT12477**  
**28-Pin HTSSOP**  
**Top View**



**PT12477**  
**28-PIN QFN**  
**TOP VIEW**



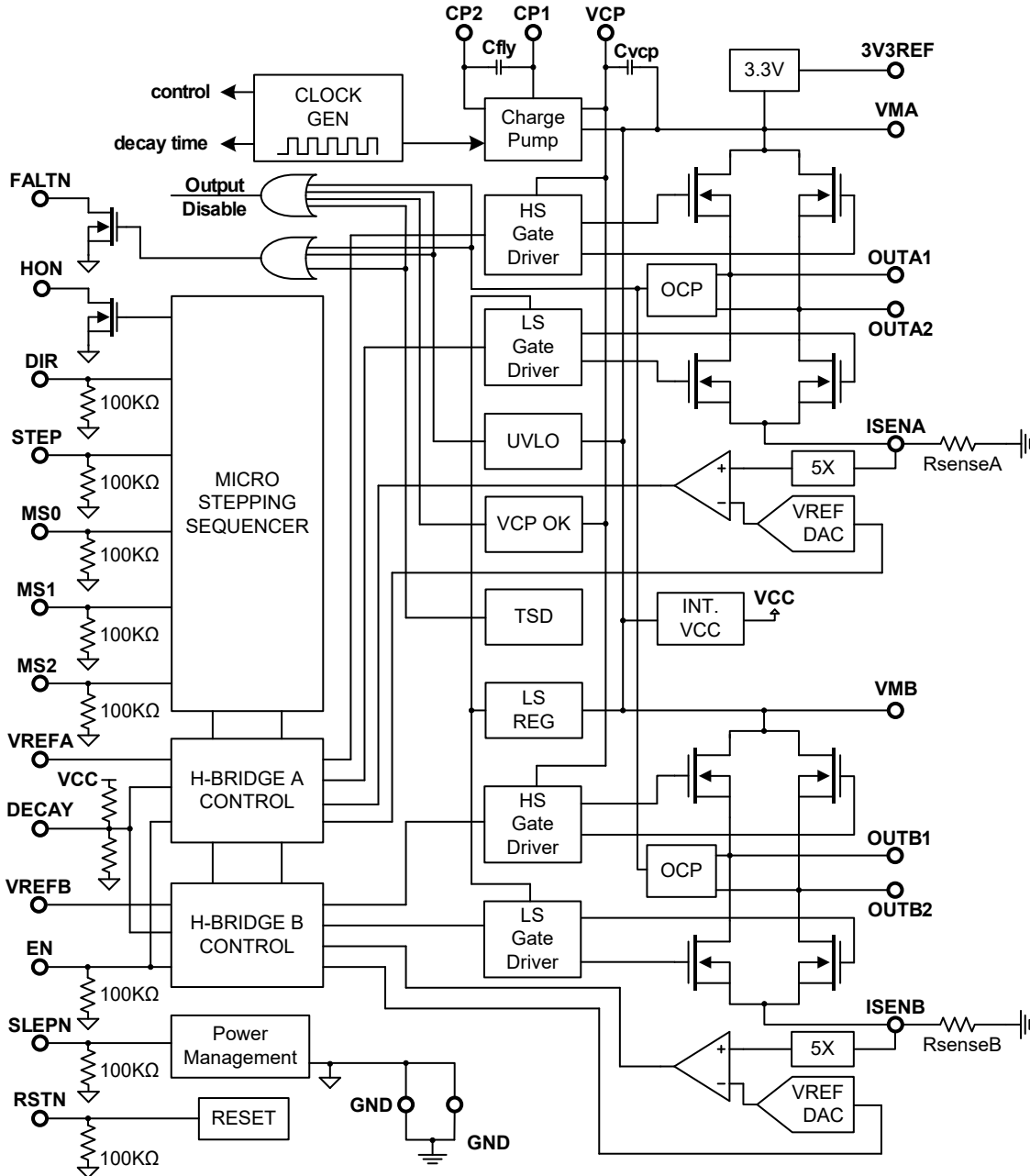
## PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.	
			HTTSSOP	QFN
CP1	I	External flying capacitor for charge pump, Connect a 0.01 $\mu$ F/50V low-ESR ceramic capacitor between CP1 and CP2.	1	4
CP2	I		2	5
VCP	O	High-side gate drive supply voltage, connect a 0.1 $\mu$ F/50V ceramic capacitor and a 1M $\Omega$ resistor to VM.	3	6
VMA	-	H-Bridge A power supply	4	7
OUTA1	O	H-Bridge A output 1	5	8
ISENA	I	H-Bridge A current sense	6	9
OUTA2	O	H-Bridge A output 2	7	10
OUTB2	O	H-Bridge B output 2	8	11
ISENB	I	H-Bridge B current sense	9	12
OUTB1	O	H-Bridge B output 1	10	13
VMB	-	H-Bridge B power supply	11	14
VREFA	I	H-Bridge A current set reference input	12	15
VREFB	I	H-Bridge B current set reference input	13	16
GND	-	Device ground	14	17
3V3REF	O	3.3V reference voltage output	15	18
RSTN	I	Reset input. Logic L=Initialize all of internal logic registers and disables H-bridge outputs, Logic H= normal operation.	16	19
SLEPN	I	Sleep mode input Logic H=device enable, Logic L=low-power sleep mode.	17	20
FALTN	O	Fault, Logic low when fault condition appear (OCP, TSD)	18	21
DECAY	I	Decay mode input Logic L=slow decay, Open=mixed decay, Logic H=fast decay	19	22
DIR	I	Motor rotation Direction logic input (with Internal pulldown). Logic H= winding current A leading winding current B Logic L= winding current B leading winding current A	20	23
EN	I	Enable input (with Internal pulldown ) Logic H = disable device outputs and sequencer operation Logic L = enable	21	24
STEP	I	Step input (with Internal pulldown). The step sequencer moves to next step during rising edge of STEP clock input.	22	25
NC	--	No connect	23	26
MS0	I	Micro-stepping sequencer configurations (with internal pull-down), Full, 1/2, 1/4, 1/8, 1/16, or 1/32 step depends combination of MS pins.	24	27
MS1	I		25	28
MS2	I		26	1
HON	OD	Home alignment output, active pull low at both winding current sets to +71% locations.	27	2
GND	-	Device ground	28	3

# FUNCTION DESCRIPTION

## MOTOR DRIVER SYSTEM BLOCK

The PT12477 includes two H-bridge drivers with PWM current regulation circuitry. A block diagram of the system control circuitry shown on Figure 1; it is ideal for driving a 4-wire bipolar stepper motor.



**Figure 1. Motor Driver Control Block Circuitry**

The multiple motor power supply pins (VMA and VMB) must be tight together to single supply voltage node on PCB.

## H-BRIDGE OUTPUT CONFIGURATION

The STEP is clock input of the micro stepping sequencer, and DIR pin determinates output winding current phase and polarity. After the RSTN pin released from reset state, the register of sequencer will be re-indexing to the HOME state and HON output will active pull low. The step resolution of the micro stepping sequencer is configures by Mode Select pins (MS0, MS1 and MS2). The EN pin is controls the H-bridge driver enable or not.

## PWM CHOPPING CURRENT REGULATION

The motor windings current regulated by the fixed-frequency PWM chopping, when the H-bridge enable, the winding current flows through the switches FET of H-bridge and direction determinate by micro stepping sequencer. The slew rate of winding current is depends on the VM voltage and inductance of the winding. Once the current reaches the current chopping threshold, the H-bridge FET will be disabled and decay mode will handles winding current decay behavior.

For a stepping motor, PWM current regulation will holding the winging current on certain level and keeps motor torque steady, and chopping current level can be further slice for micro-stepping drives. A comparator is used to sets the chopping current level, the Itrip. The voltage across an external current sense resistor connected to the ISENx pins will multiples by 5 and compare with VREFx DAC output. The VREFx input voltage scaled by a 6-bit VREFx DAC and output voltage restrict by micro-stepping sequencer and Mode Select (MSx) pins configuration.

The full-scale (100%) PWM chopping current level is calculate in Equation 1.

$$I_{CHOP} = \frac{V_{REFx} \times VREF \text{ DAC ratio}}{5 \times R_{SENSE}} \quad \text{Eq.(1)}$$

### For Example:

If a 0.5Ω sense resistor is used and the VREFx pin is 2.5 V, the full-scale chopping current Itrip will be:

$$(2.5 \text{ V} \times 100\%) / (5 \times 0.5 \Omega) = 1.0A.$$

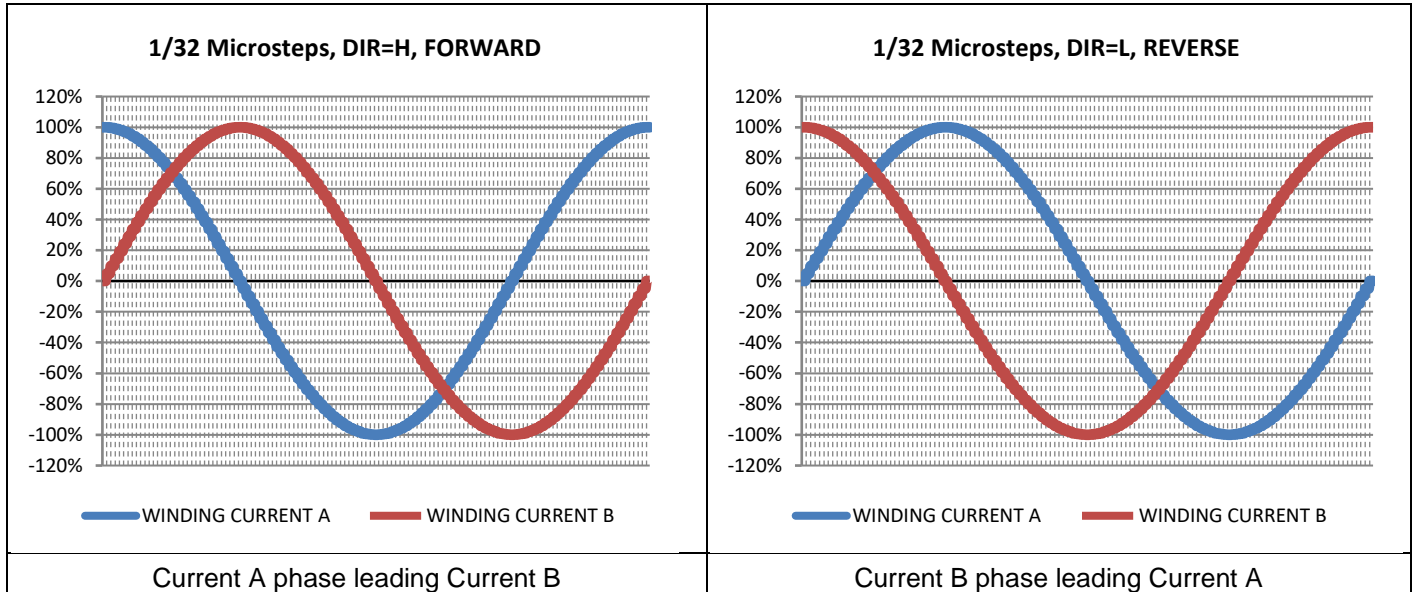
## MICROSTEPPING SEQUENCER

Built-in micro-stepping sequencer allows many different kind of stepping configurations. The MS0 through MS2 pins are uses to configure the stepping format, as shown in Table 1.

MS2	MS1	MS0	STEP MODE
0	0	0	Full step (2-phase excitation) with 71% of full-scale current
0	0	1	1/2 step (1-2 phase excitation)
0	1	0	1/4 step (W1-2 phase excitation)
0	1	1	1/8 microstep (2W1-2 phase excitation)
1	0	0	1/16 microstep (4W1-2 phase excitation)
1	0	1	1/32 microstep
1	1	0	1/32 microstep
1	1	1	1/32 microstep

Table 1. Stepping Format

At each rising edge of the STEP clock input, the microstepping sequencer transit to the next step according to step table definition, the motor rotation direction is determinate by logic state of DIR pin, it will determinates the winding current phase between two H bridge output, please refers to Figure 2.



**Figure 2. Winding Current Phase and Direction**

Table 2 and Figure3 shows the winding current relative level and both H-bridge phase relationship by different settings of Mode Select Pin (MSx). Note that if the microstepping mode is changing while stepping, the sequencer advances to the next valid state for the new MSx setting at the STEP rising edge.

Refer to Figure 4, the home alignment state (HON) means the shaft angle in 45°. After power-up or RSTN pin released, the HON will active pull low and both winding current will sets to +71% position. The logic inputs DIR, STEP, RSTN, and MSx have internal pulldown resistors of 100 KΩ

1/32 STEP	1/16 STEP	1/8 STEP	1/4 STEP	1/2 STEP	FULL STEP	HON STATE	WINDING A CURRENT	MIXED DECAY A	WINDING B CURRENT	MIXED DECAY B	ELEC. ANGLE
1	1	1	1	1			100%	S	0%	-	0
2							100%	S	5%	S	3
3	2						100%	S	10%	S	6
4							99%	M	15%	S	8
5	3	2					98%	M	20%	S	11
6							97%	M	24%	S	14
7	4						96%	M	29%	S	17
8							94%	M	34%	S	20
9	5	3	2				92%	M	38%	S	23
10							90%	M	43%	S	25
11	6						88%	M	47%	S	28
12							86%	M	51%	S	31
13	7	4					83%	M	56%	S	34
14							80%	M	60%	S	37
15	8						77%	M	63%	S	39
16							74%	M	67%	S	42
17	9	5	3	2	1	L	71%	M	71%	S	45
18							67%	M	74%	S	48
19	10						63%	M	77%	S	51
20							60%	M	80%	S	53



1/32 STEP	1/16 STEP	1/8 STEP	1/4 STEP	1/2 STEP	FULL STEP	HON STATE	WINDING A CURRENT	MIXED DECAY A	WINDING B CURRENT	MIXED DECAY B	ELEC. ANGLE
21	11	6					56%	M	83%	S	56
22							51%	M	86%	S	59
23	12						47%	M	88%	S	62
24							43%	M	90%	S	65
25	13	7	4				38%	M	92%	S	68
26							34%	M	94%	S	70
27	14						29%	M	96%	S	73
28							24%	M	97%	S	76
29	15	8					20%	M	98%	S	79
30							15%	M	99%	S	82
31	16						10%	M	100%	S	84
32							5%	M	100%	S	87
33	17	9	5	3			0%	-	100%	S	90
34							-5%	S	100%	S	93
35	18						-10%	S	100%	S	96
36							-15%	S	99%	M	98
37	19	10					-20%	S	98%	M	101
38							-24%	S	97%	M	104
39	20						-29%	S	96%	M	107
40							-34%	S	94%	M	110
41	21	11	6				-38%	S	92%	M	113
42							-43%	S	90%	M	115
43	22						-47%	S	88%	M	118
44							-51%	S	86%	M	121
45	23	12					-56%	S	83%	M	124
46							-60%	S	80%	M	127
47	24						-63%	S	77%	M	129
48							-67%	S	74%	M	132
49	25	13	7	4	2		-71%	S	71%	M	135
50							-74%	S	67%	M	138
51	26						-77%	S	63%	M	141
52							-80%	S	60%	M	143
53	27	14					-83%	S	56%	M	146
54							-86%	S	51%	M	149
55	28						-88%	S	47%	M	152
56							-90%	S	43%	M	155
57	29	15	8				-92%	S	38%	M	158
58							-94%	S	34%	M	160
59	30						-96%	S	29%	M	163
60							-97%	S	24%	M	166
61	31	16					-98%	S	20%	M	169
62							-99%	S	15%	M	172

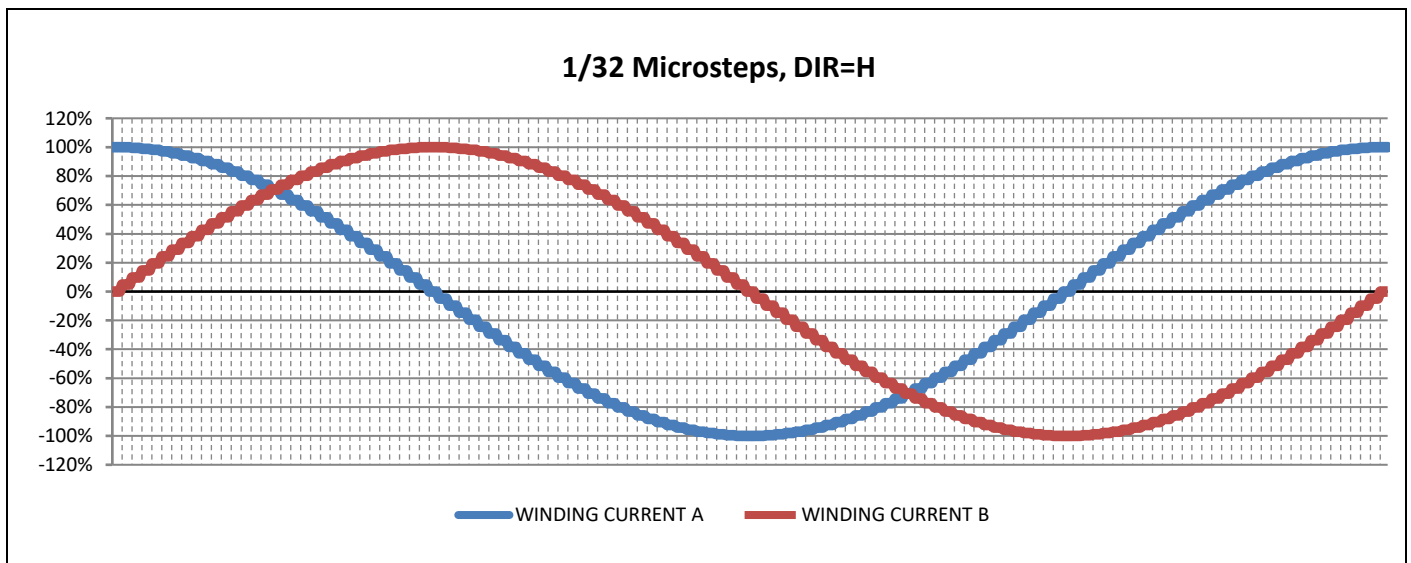


1/32 STEP	1/16 STEP	1/8 STEP	1/4 STEP	1/2 STEP	FULL STEP	HON STATE	WINDING A CURRENT	MIXED DECAY A	WINDING B CURRENT	MIXED DECAY B	ELEC. ANGLE
63	32						-100%	S	10%	M	174
64							-100%	S	5%	M	177
65	33	17	9	5			-100%	S	0%	-	180
66							-100%	S	-5%	S	183
67	34						-100%	S	-10%	S	186
68							-99%	M	-15%	S	188
69	35	18					-98%	M	-20%	S	191
70							-97%	M	-24%	S	194
71	36						-96%	M	-29%	S	197
72							-94%	M	-34%	S	200
73	37	19	10				-92%	M	-38%	S	203
74							-90%	M	-43%	S	205
75	38						-88%	M	-47%	S	208
76							-86%	M	-51%	S	211
77	39	20					-83%	M	-56%	S	214
78							-80%	M	-60%	S	217
79	40						-77%	M	-63%	S	219
80							-74%	M	-67%	S	222
81	41	21	11	6	3		-71%	M	-71%	S	225
82							-67%	M	-74%	S	228
83	42						-63%	M	-77%	S	231
84							-60%	M	-80%	S	233
85	43	22					-56%	M	-83%	S	236
86							-51%	M	-86%	S	239
87	44						-47%	M	-88%	S	242
88							-43%	M	-90%	S	245
89	45	23	12				-38%	M	-92%	S	248
90							-34%	M	-94%	S	250
91	46						-29%	M	-96%	S	253
92							-24%	M	-97%	S	256
93	47	24					-20%	M	-98%	S	259
94							-15%	M	-99%	S	262
95	48						-10%	M	-100%	S	264
96							-5%	M	-100%	S	267
97	49	25	13	7			0%	-	-100%	S	270
98							5%	S	-100%	S	273
99	50						10%	S	-100%	S	276
100							15%	S	-99%	M	278
101	51	26					20%	S	-98%	M	281
102							24%	S	-97%	M	284
103	52						29%	S	-96%	M	287
104							34%	S	-94%	M	290

1/32 STEP	1/16 STEP	1/8 STEP	1/4 STEP	1/2 STEP	FULL STEP	HON STATE	WINDING A CURRENT	MIXED DECAY A	WINDING B CURRENT	MIXED DECAY B	ELEC. ANGLE
105	53	27	14				38%	S	-92%	M	293
106							43%	S	-90%	M	295
107	54						47%	S	-88%	M	298
108							51%	S	-86%	M	301
109	55	28					56%	S	-83%	M	304
110							60%	S	-80%	M	307
111	56						63%	S	-77%	M	309
112							67%	S	-74%	M	312
113	57	29	15	8	4		71%	S	-71%	M	315
114							74%	S	-67%	M	318
115	58						77%	S	-63%	M	321
116							80%	S	-60%	M	323
117	59	30					83%	S	-56%	M	326
118							86%	S	-51%	M	329
119	60						88%	S	-47%	M	332
120							90%	S	-43%	M	335
121	61	31	16				92%	S	-38%	M	338
122							94%	S	-34%	M	340
123	62						96%	S	-29%	M	343
124							97%	S	-24%	M	346
125	63	32					98%	S	-20%	M	349
126							99%	S	-15%	M	352
127	64						100%	S	-10%	M	354
128							100%	S	-5%	M	357

(ELEC. ANGLE=ELECTRICAL ANGLE, S = Slow decay, M= Mixed decay)

**Table 2. Relative Current Ratio and Step Directions**



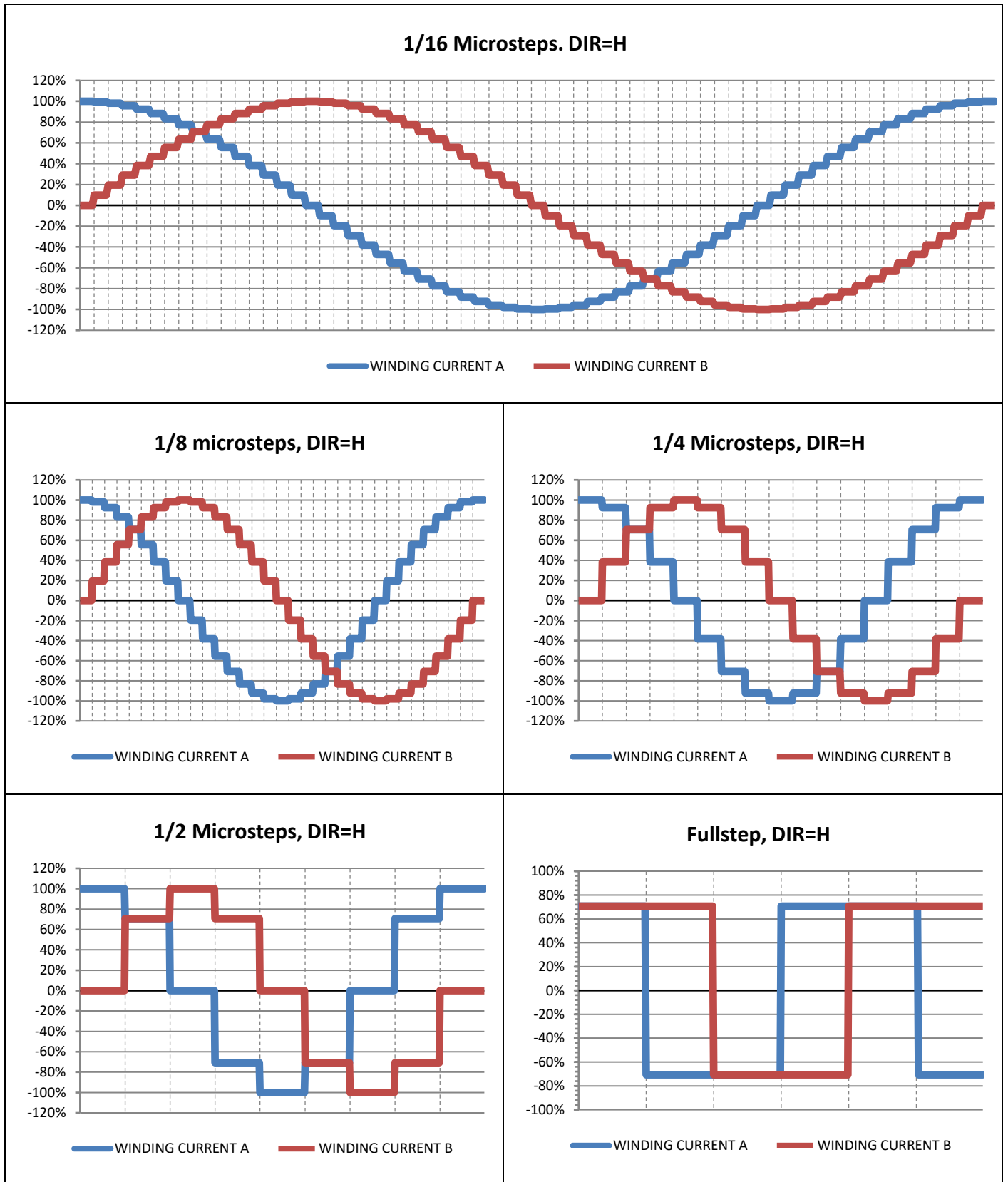
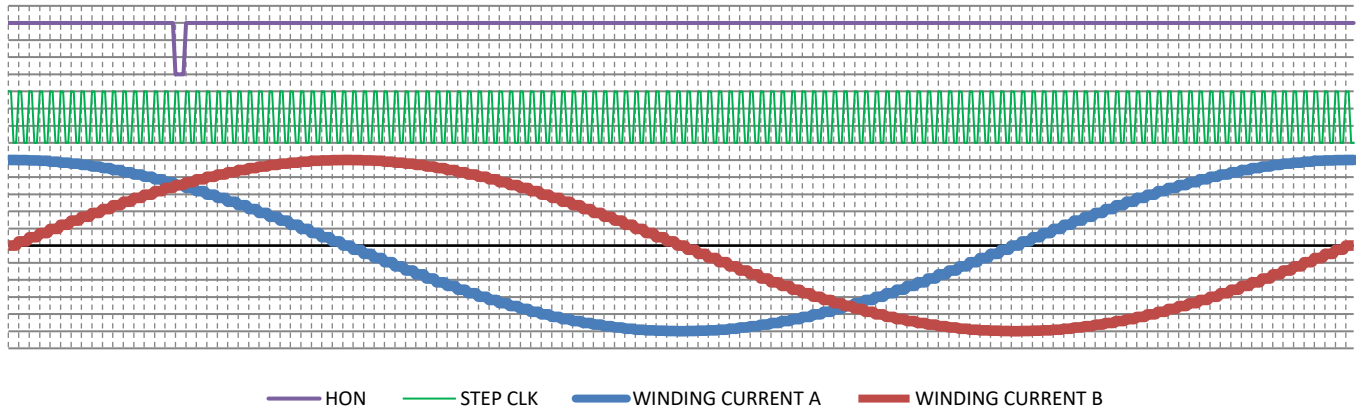
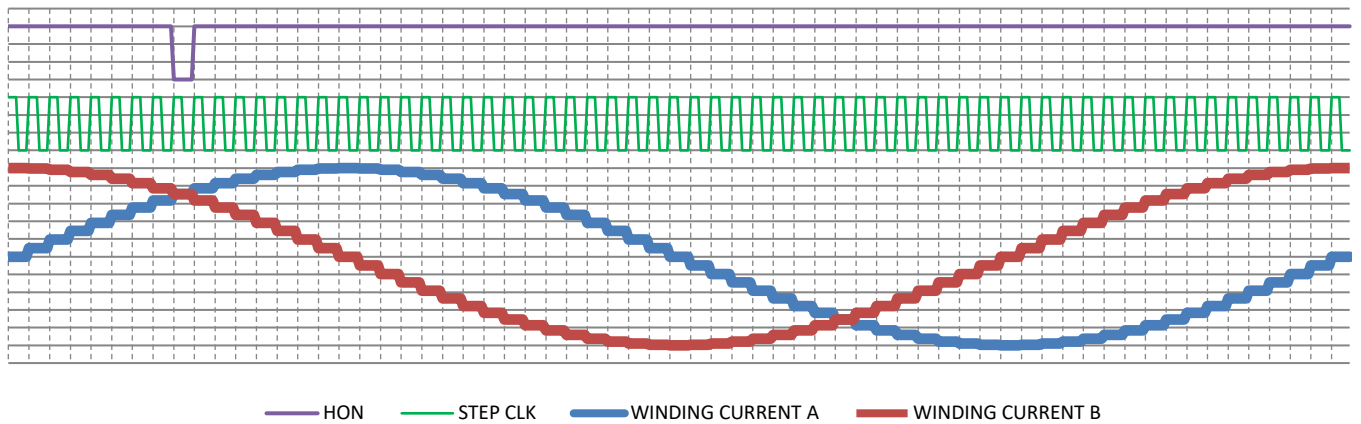


Figure 3. PWM Chopping Current Ratio in Each Microstepping Mode

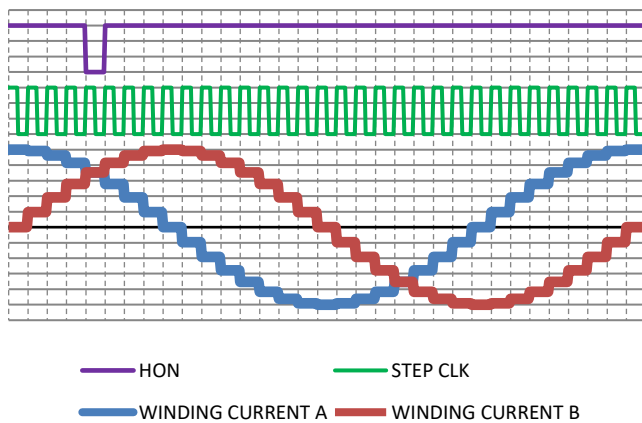
1/32 Microsteps, DIR=H



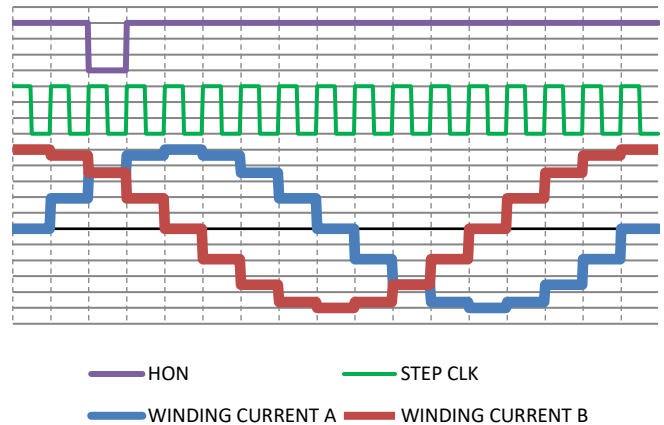
1/16 Microsteps. DIR=L



1/8 Microsteps, DIR=H



1/4 Microsteps, DIR=L



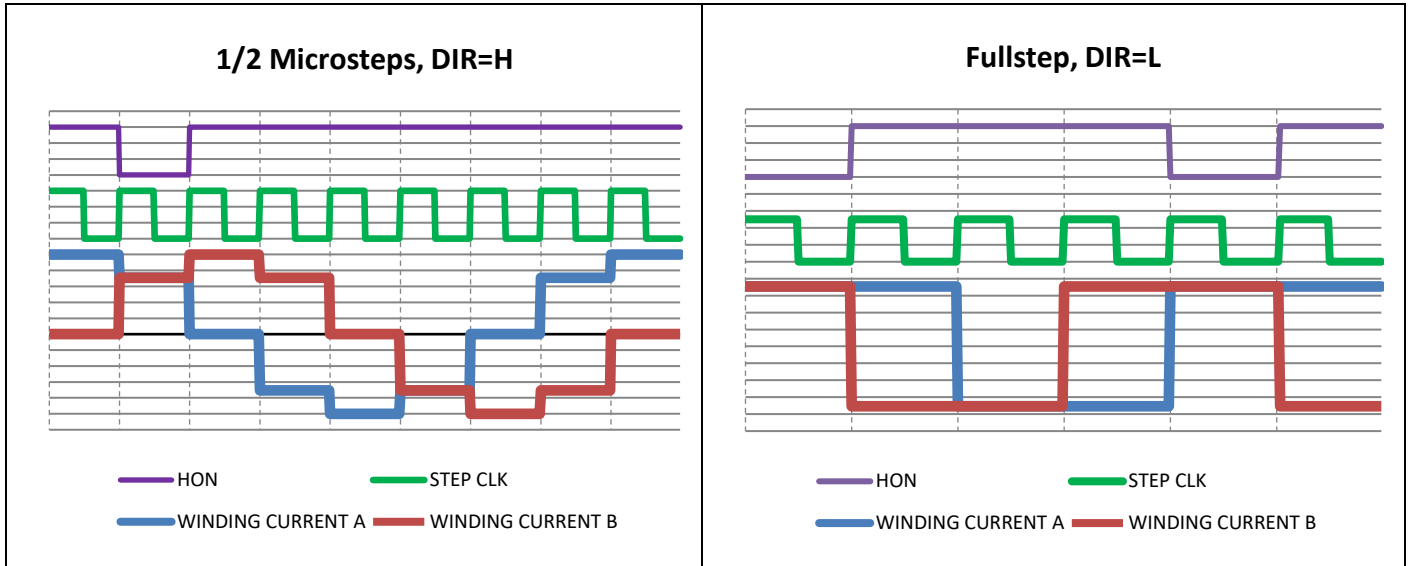


Figure 4. PWM Chopping Current and STEP / HON Relations

## DECAY MODE

The motor winding current in PWM chopping cycle is determined by the voltage on the DECAY pin. In charge phase, the winding is excited by H-bridge output current, the winding current through the current sense resistor on the ISENx pin presents a voltage drop and H-bridge will leave charge mode if reaches comparator threshold, and next step of H-bridge will go to one of three modes, fast, slow or mixed decay, depends on DECAY pin logic status. Please refer to the Table 3 for DECAY setting definition and H-bridge current flows in each decay mode is shown on Figure 5.

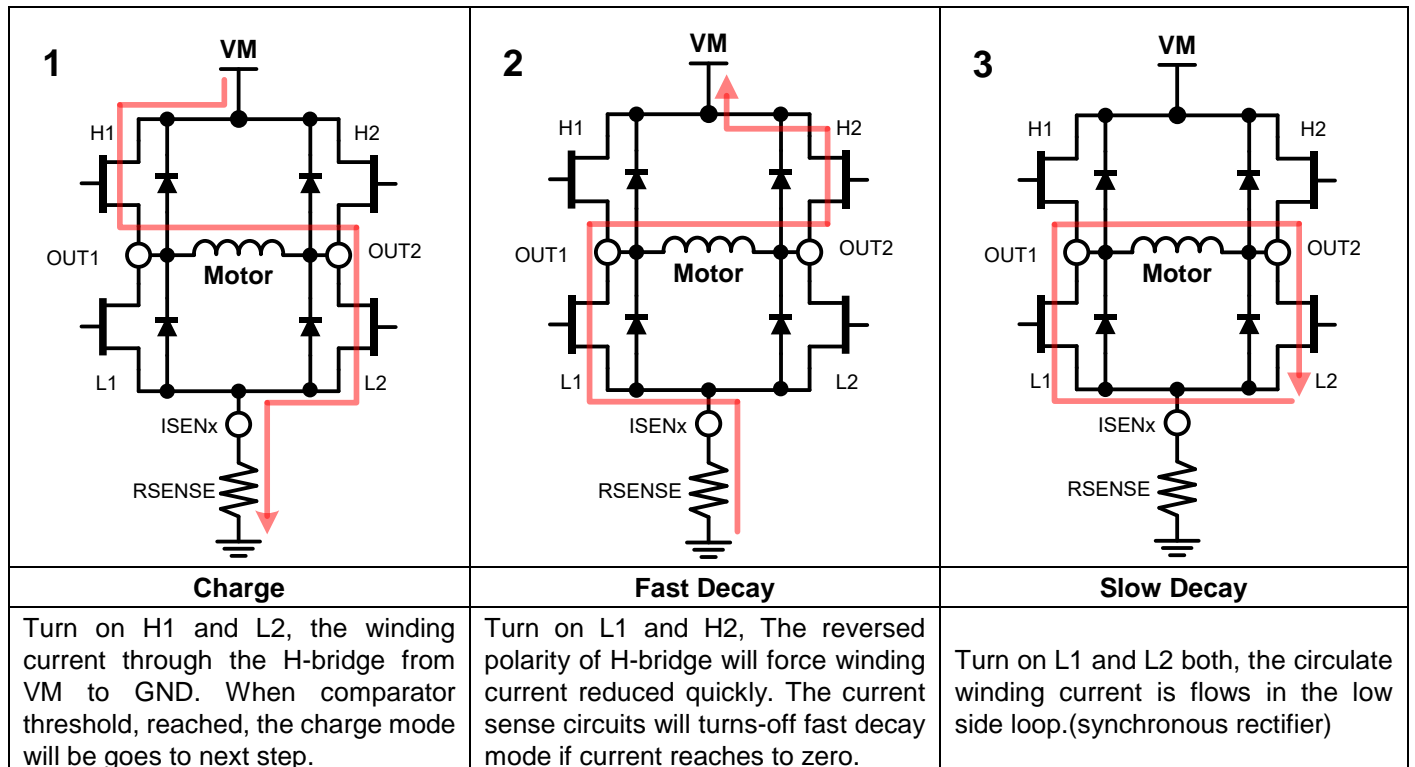
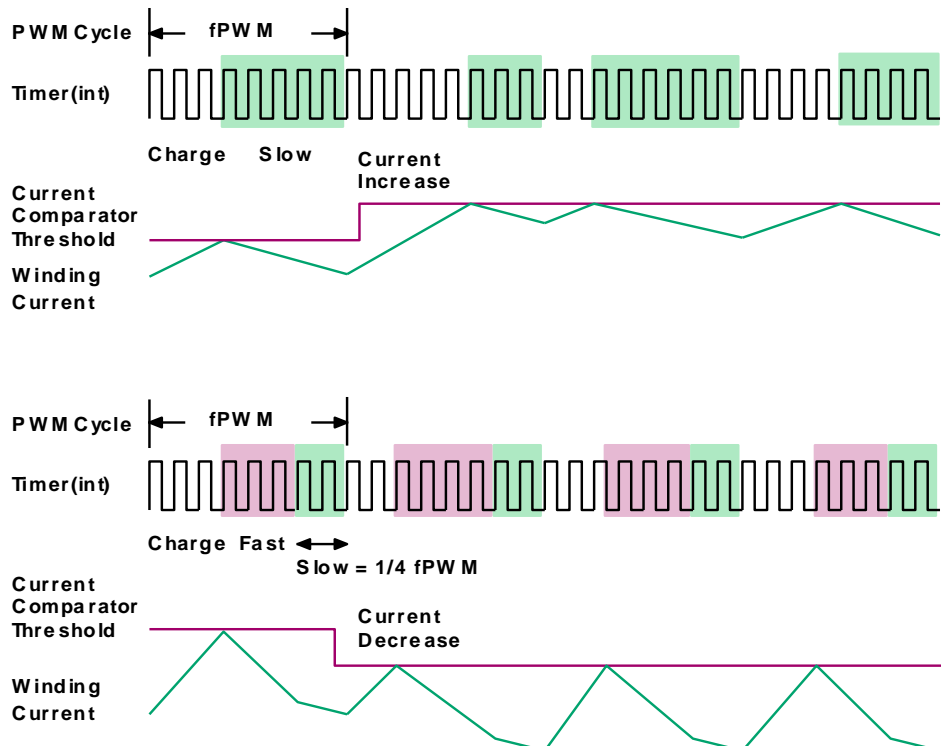


Figure 5. Mixed Decay Mode Switching Sequence (Forward mode only)

Decay Pin Level	DECAY Pin Logic	Decay Mode
<0.6V	L	Slow
OPEN	FLOAT	Mixed
>2V	H	Fast

Table 3. DECAY Mode Setting

The slow and fast decay will apply to both H-bridges simultaneously whatever which kind of MSx or DIR setting. The mixed decay have different behavior; if MSx configuration sets to FULL STEP (2 phase excitation) mode and mixed decay mode is active, the H-bridge will always operating in mixed decay whatever the winding current direction. In other microstepping modes the decay mode will following the Table 3 definition; during the winding current increasing period the slow decay is active, and mixed decay will applied in the winding current reducing period, in the Figure 6 shows the mixed decay current waveform.



(Timer(int) is an internal clock management block uses to drives charge pump and PWM switching cycles, timing clock is only for realize mixed decay operation, not an exactly clock )

Figure 6. Mixed Decay Sequence Waveform

## RESET and LOW POWER SLEEP MODE

Pull the RSTN pin to logic low state, the status of all control pins (except SLEPN) will be ignore and internal control circuit will be reset to initial state, the H-bridge output also disabled during RSTN in low state, in the meantime the 3.3V voltage reference and charge pump still works.

Pull the SLEPN pin to logic low will force the chip into a low power sleep mode. During sleep mode is active the H-bridges outputs are disabled, and analog circuit such like charge pump for HS gate driver, 3.3V voltage reference (3V3REF) and internal clocks blocks all stopped. In this mode, all inputs ignored until SLEPN returns to logic high state. When chip is wakes up from the low power sleep mode, a short waiting time (less than 1mS) before H-bridge becomes to normal operation is required because of charge pump starting time.

## **BLANKING TIME**

During PWM chopping current is flows after the H-bridge enable, the current signal can be picked-up in the sense resistor connected in ISENx pins, the signal will delivers to comparator after a fixed delay time to avoid noises or current spike causes fault-triggered. The blanking time is fixed at 3.75 $\mu$ S and it also sets a limit to the duty cycle of PWM in charge period, the minimum on-duty will not less than around 18.75% in a 50KHz PWM frequency.

## **PROTECTION CIRCUITS**

The PT12477 have fully protection function to against miss-operation events.

### **◆ OVERCURRENT PROTECTION (OCP)**

Overcurrent detection circuit will always monitor all of output pins current during H-bridge is enable, this operation is independent from PWM chopping. If any output pin connected to VM, GND or across load shorted, the inrush high current will be detect by OCP circuit and immediately turn off both H-bridge outputs after blanking time. The chip will remain disabled until either RSTN pin is toggle once or power down the VM supply and apply again.

If an output pin connects to the VM, the short circuit current will be passing through the low side MOSFET and current sense resistor to GND, to avoid sense resistance interference the OCP detection, it should not be higher than a certain range, for example, 0.5 $\Omega$  or less is recommend.

### **◆ THERMAL SHUTDOWN (TSD)**

If the chip temperature exceeds preset 160 $^{\circ}$ C, all of MOSFET of H-bridge will be turn off and the FALTN pin will be pull down, an external pull up resistor may needed to detects FALTN logic state by MCU I/O pin. Once the chip temperature is cooling down to below hysteresis window, H-bridge outputs will enable again.

### **◆ UNDERVOLTAGE LOCKOUT (UVLO)**

In Any time the VM pin voltage drops below the under voltage lockout threshold voltage, all circuitry in the chip will be disabled and internal logic will be reset. Operation will resume when VM rises above the UVLO threshold.

### **◆ FAULT INDICATION (FALTN)**

Whatever which condition is happens, the OCP, TSD or charge pump voltage failed, the open-drain FALTN pin will pull down immediately and remains until RSTN pin re-toggled or VM voltage re-applied. FALTN could connect to MCU I/O port for error reporting with a pull high resistor to the 3V3REF or 5V logic supply.

## **POWER SUPPLY CAPACITOR RECOMMENDATIONS**

Consider a real world application scenario; the motor driver is uses to drives high inductance load such like motor winding or solenoid coil. If a H-bridge turns-off all of outputs during inductor current still flowing, because the inductor current would not be reset immediately, the rest of free-wheel current would re-directs and passing through the body diode of the output FET and runs into VM supply and final decay to zero after de-magnetization time. This reverse current depends on load inductance, inductor current and re-generates current from the motor due to inertia of rotor.

In another case, the parasitic reactance (inductance + resistance) of power wire between the power supply and motor driver board with parasitic capacitance of PCB consists a LC resonates tank. During power supply sourcing current to the motor driver board, the VM voltage may be drops quickly and parasitic LC will causes oscillation spike if the local bypass capacitor is not sufficient.

To prevent unstable bounce or spike appears on VM bus, a high capacitance bounce absorber capacitor (>100 $\mu$ F) should be placed on VM bus line, it could absorb re-generates free-wheels current during DC motor brake and stabilize VM voltage during high forward/reverse motor current sources. A small MLCC 0.1 $\mu$ F bypass capacitor should be place near the motor driver IC power pin, VM and 3V3REF both, to reduce the spike causes by power line LC resonates.

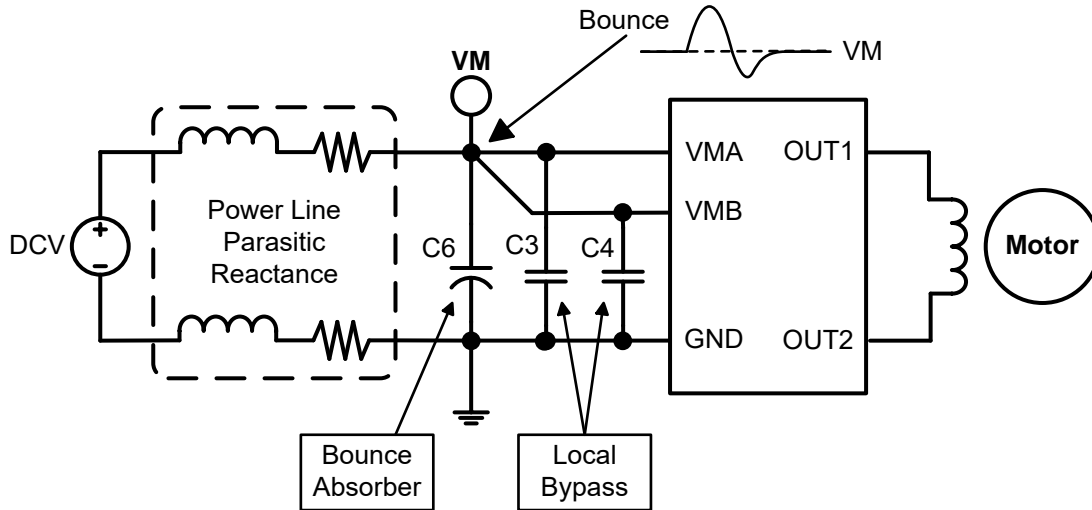


Figure 7. Motor Driver System with External Power Supply

## PCB LAYOUT RECOMMENATION

The local bypass capacitor C3 and C4 should be place near the IC power pins, and bounce absorber capacitor C6 should be place on VM bus line. The GND plane should be place on the component side under the chip as a low impedance power trace, and larger area of GND plane and wider cooper trace reduce the thermal resistance ( $\theta_{JA}$ ). The thermal pad under the HTSSOP and QFN package should be soldered to PCB component side and connecting to bottom side through via holes, this arrangement can further enhance the heat dissipation.

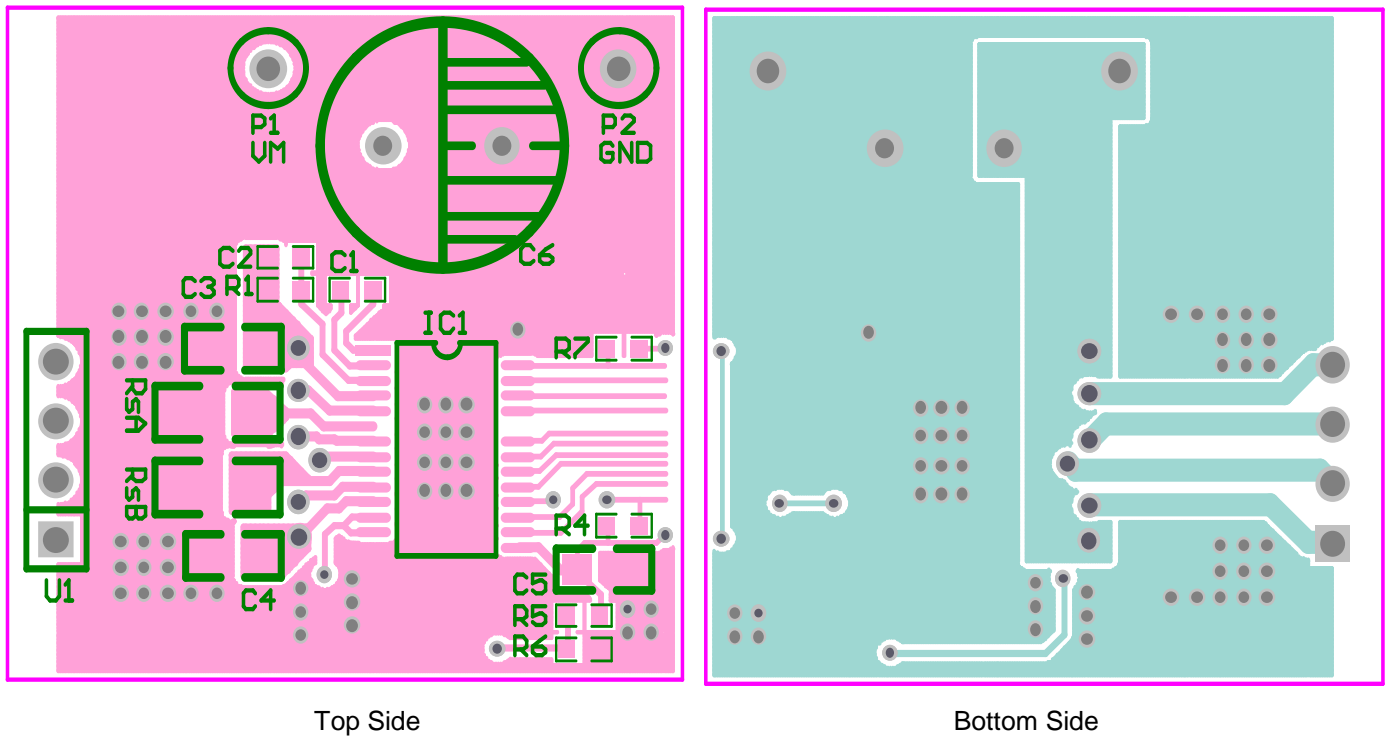


Figure 8. Simplified Layout Example (for HTSSOP package)

## ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage	VMA, VMB	-0.3	47	V
Digital I/O Pin Voltage	MS0,MS1,MS2,STEP, DIR,DECAY,EN,SLEPN, RSTN,FALTN	-0.3	7	V
VREF Input Voltage	VREFA,VREFB	-0.3	4	V
Output Current <sup>*note1</sup>	I <sub>OUT</sub>		1.6	A
Operating Temperature	T <sub>OPR</sub>	-40	125	°C
Storage Temperature	T <sub>STG</sub>	-40	150	°C
ESD, Human Body Model	HBM	-2000	+2000	V
ESD, Machine Model	MM	-200	+200	V

Operating a device beyond its Absolute Maximum Ratings may cause permanent damage. These limits do not guarantee proper function or performance. Even short-term operation within Absolute Maximum Ratings but outside the Recommended Operating Conditions may lead to malfunction, reduced reliability, or shortened lifespan.

## PACKAGE THERMAL CHARACTERISTIC

Parameter	Symbol	Condition	HTSSOP (28 PINS)	QFN (28 PINS)	Unit
From chip junction dissipation to external environment	R <sub>ja</sub>	T <sub>A</sub> =25 °C	38.9	35.8	°C/W
From chip junction dissipation to package surface	R <sub>jc</sub>		23.3	25.1	

## RECOMMENDED OPERATING CONDITION

Parameter	Symbol	Min	Typ	Max	Unit
Motor Power Supply Voltage Range	V <sub>M</sub>	8	24	36	V
VREFx Input Voltage	V <sub>REF1</sub> <sup>*note1</sup>	1		3.5	V
	V <sub>REF2</sub> <sup>*note2</sup>	0.2		3.5	V
3V3REF Load Current	I <sub>3V3</sub>			1	mA

Operation between Recommended Operating Conditions and Absolute Maximum Ratings for extended periods cannot guarantee long-term reliability or normal functionality

\*note1: For better current DAC linearity in micro-stepping mode, the VREF voltage keeps above 1V is recommended.

\*note2: For "FULL STEP" and "1/2 STEP" operation only, the VREF voltage down to 0.2V will not affect tolerance.

# ELECTRICAL CHARACTERISTIC

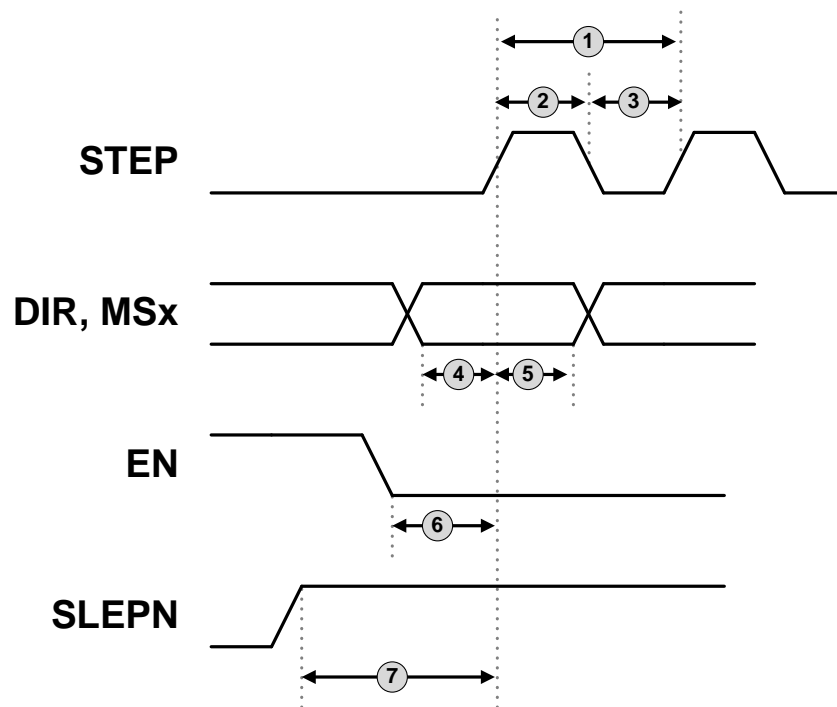
$T_A=25^{\circ}\text{C}$  ,  $V_M=24\text{V}$  ,over operating free-air temperature range (unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply current	$I_M$	$V_M=24\text{V}$ , SLEPN=5V	6	9	14	mA
		$V_M=24\text{V}$ , SLEPN=0V		10	20	$\mu\text{A}$
Under voltage lock out	UVLO	$V_M$ rises	7	7.2	7.4	V
		$V_M$ falls	6.4	6.6	6.8	V
<b>3V3REF REGULATOR</b>						
3V3REF voltage	$3V3_{REF}$	$I_{OUT} = 0$ to 1mA, $V_M=24\text{V}$	3.18	3.30	3.42	V
<b>LOGIC LEVEL INPUTS</b>						
Digital input high level	$V_{IH}$		2		5.25	V
Digital input low level	$V_{IL}$		0		0.6	V
Input high current	$I_{IH}$	$V_{IN} = 3.3\text{V}$		33	100	$\mu\text{A}$
Input low current	$I_{IL}$	$V_{IN} = 0\text{V}$	-20		20	$\mu\text{A}$
Logic inputs pull down Resistance	$R_{PD}$		70	100	130	K $\Omega$
Input Deglitch Time	$T_{INDG}$			400		ns
<b>HON, FALTN OUTPUT (OPEN DRAIN)</b>						
Output low voltage	$V_{OL}$	$I_O = 5\text{mA}$			0.5	V
Output high leakage current	$I_{OH}$	$V_O = 3.3\text{V}$			1	$\mu\text{A}$
<b>DECAY INPUT</b>						
Input high threshold voltage	$V_{IH}$	For fast decay mode	2		3.3	V
Input low threshold voltage	$V_{IL}$	For slow decay mode	0		0.6	V
Input current	$I_{IN}$	$V_{IN}=3.3\text{V}$		13	40	$\mu\text{A}$
Decay pull up resistance	$R_{DPU}$		175	250	325	K $\Omega$
Decay pull down resistance	$R_{DPD}$		175	250	325	K $\Omega$
<b>H-BRIDGE DRIVERS</b>						
HS MOSFET on resistance	$R_{DS(ON)}$	$V_M = 24\text{V}$ , $I_o = 1\text{A}$ , $T_J = 25^{\circ}\text{C}$		0.58		$\Omega$
		$V_M = 24\text{V}$ , $I_o = 1\text{A}$ , $T_J = 85^{\circ}\text{C}$		0.68		$\Omega$
LS MOSFET on resistance	$R_{DS(ON)}$	$V_M = 24\text{V}$ , $I_o = 1\text{A}$ , $T_J = 25^{\circ}\text{C}$		0.58		$\Omega$
		$V_M = 24\text{V}$ , $I_o = 1\text{A}$ , $T_J = 85^{\circ}\text{C}$		0.68		$\Omega$
Off-state leakage current	$I_{OFF}$		-20		20	$\mu\text{A}$
Internal PWM frequency	$f_{PWM}$			50		KHz
Current sense blanking time	$t_{BLANK}$			3.75		$\mu\text{s}$
Rise time	$t_R$	$V_M = 24\text{V}$	80		250	ns
Fall time	$t_F$	$V_M = 24\text{V}$	80		160	ns
Dead time	$t_{DEAD}$			400		ns
<b>PROTECTION CIRCUITS</b>						
Overcurrent protection trip level	$I_{OCP}$		1.8		5	A
Overcurrent protection deglitch time	$t_{OCDG}$			3		$\mu\text{s}$
Thermal shutdown temperature	$t_{TSD}$	Die temperature		160		$^{\circ}\text{C}$

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>CURRENT REGULATION CONTROL</b>						
VREFx Input Current	$I_{REF}$	$V_{REFx} = 3.3V$	-3		3	$\mu A$
ISENx Trip Voltage	$V_{TRIP}$	$V_{REFx}=3.3V$ , 100% current setting	635	660	685	mV
Trip current tolerance	$\Delta I_{TRIP}$	$V_{REFx}=3.3V$ , 5% current setting	-25		25	%
		$V_{REFx}=3.3V$ , 10% to 34% current setting	-15		15	
		$V_{REFx}=3.3V$ , 38% to 67% current setting	-10		10	
		$V_{REFx}=3.3V$ , 71% to 100% current setting	-5		5	
Current sense amplifier gain	$A_{ISENSE}$	Design Guaranteed		5		V/V

## TIMEING REQUIREMENT

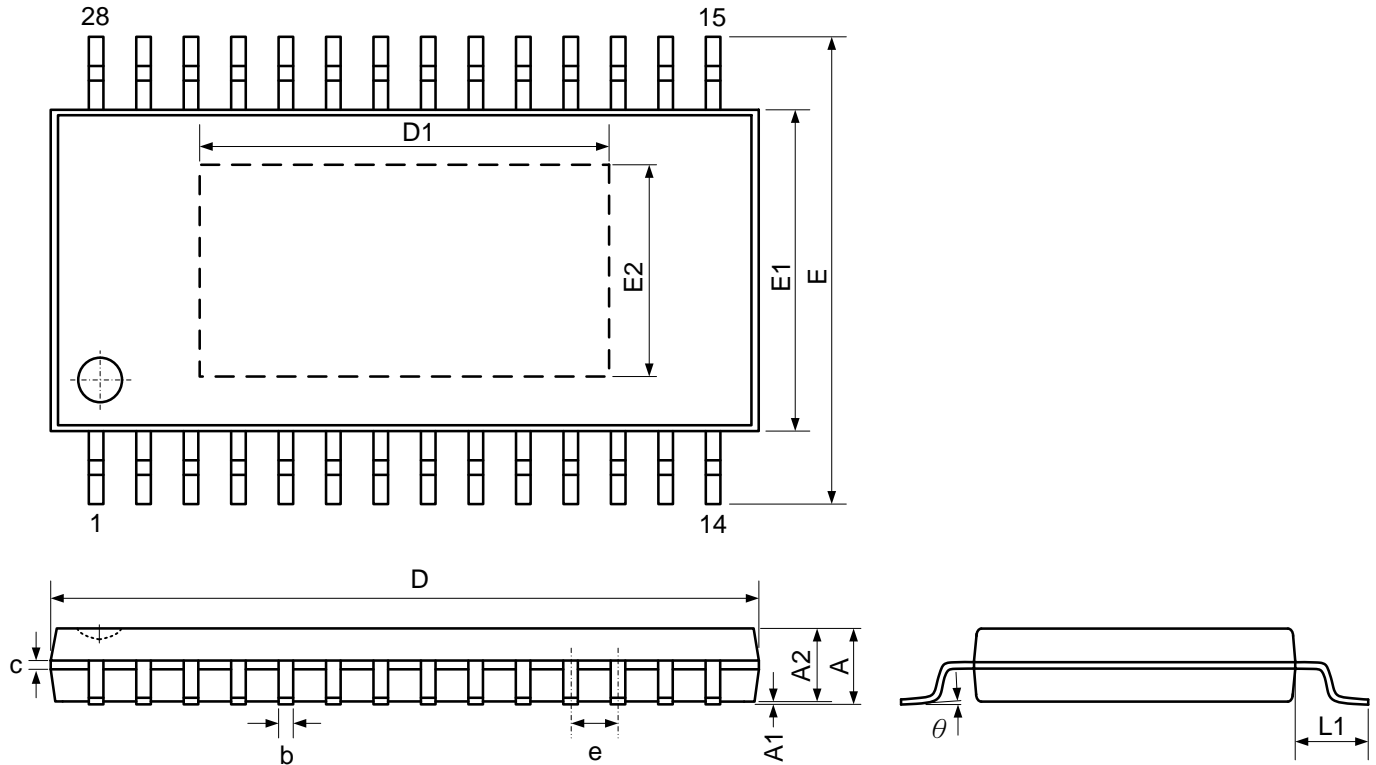
No.	Parameter	Symbol	MIN	MAX	UNIT
1	Step frequency	$f_{STEP}$		250	KHz
2	Pulse duration, STEP high	$t_{WH(STEP)}$	1.9		$\mu s$
3	Pulse duration, STEP low	$t_{WL(STEP)}$	1.9		$\mu s$
4	Setup time, commanded before STEP rising	$t_{SU(STEP)}$	450		ns
5	Hold time, commanded after STEP rising	$t_{H(STEP)}$	450		ns
6	Enable time, EN active to STEP	$t_{ENBL}$	450		ns
7	Wakeup time, SLEPN inactive high to STEP input accepted	$t_{WAKE}$		1	ms



Timing Diagram

# PACKAGE INFORMATION

## 28-PIN, HTSSOP, 173MIL

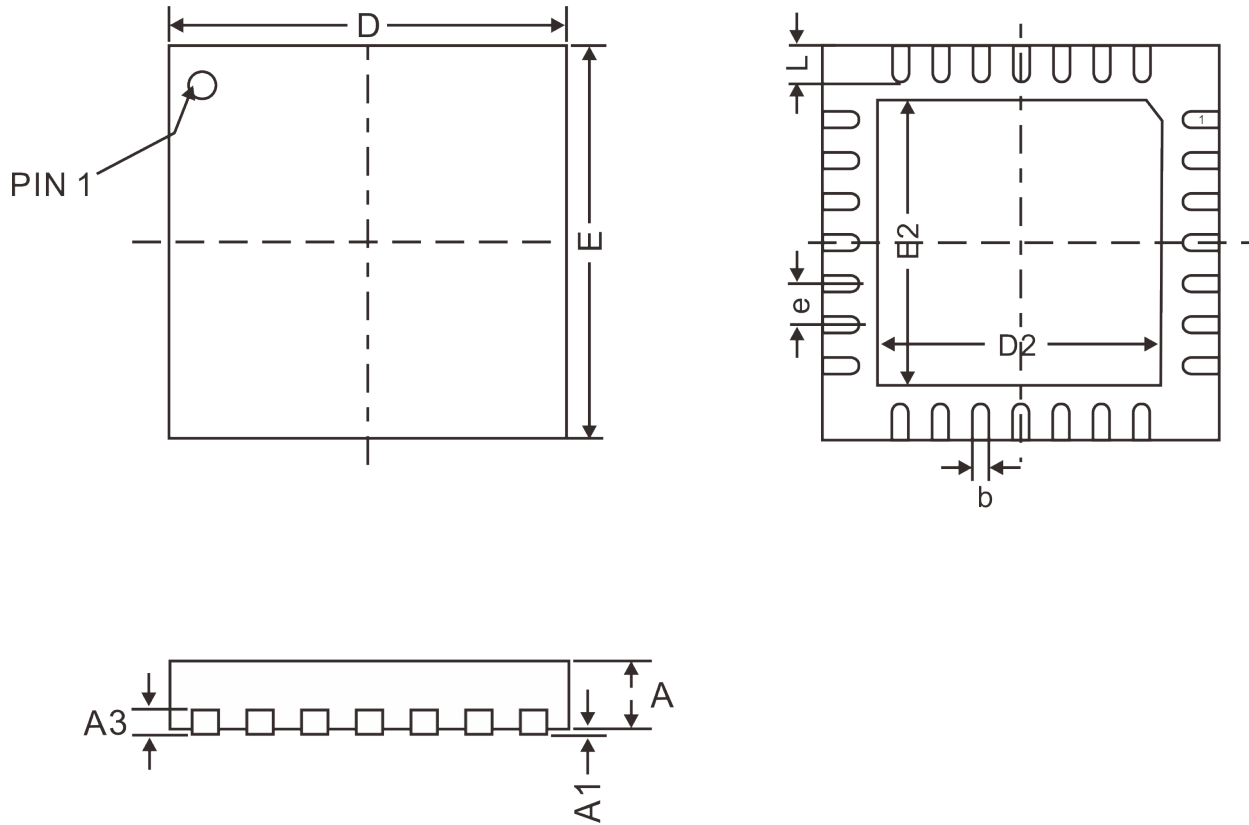


Symbol	Dimensions(mm)		
	Min.	Nom.	Max.
A			1.20
A1	0		0.15
A2	0.8		1.05
b	0.19		0.30
c	0.09		0.20
D	9.60	9.70	9.80
E1	4.30	4.40	4.50
E	6.4 BSC		
e	0.65 BSC		
D1	5.30	5.60	5.90
E2	2.50	2.80	3.10
L1	1.00 REF		
$\theta$	0°		8°

Notes:

1. All dimensions refer to JEDEC MO-153 AET

**28-PIN, QFN, 5X5**



Symbol	Dimensions(mm)		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1		0.02	0.05
A3	0.203 REF		
b	0.18	0.25	0.30
D	5.00 BSC		
D2	3.20	3.25	3.30
E	5.00 BSC		
E2	3.20	3.25	3.30
e	0.50 BSC		
L	0.50	0.55	0.60

Notes:  
 1. All dimensions refer to JEDEC MO-220 WHHD-1

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