

DESCRIPTION

The PT12493 is an integrated multi-channel half-bridge drivers with 8 half-bridges. The device features low on-state resistance ($R_{DS(ON)}$) for improved thermal performance during high-current operation. This device can drive brushed-DC (BDC) motors or stepper motors in independent, sequential, or parallel mode. The half-bridges are fully controllable to achieve a forward, reverse, coasting and braking operation of motor.

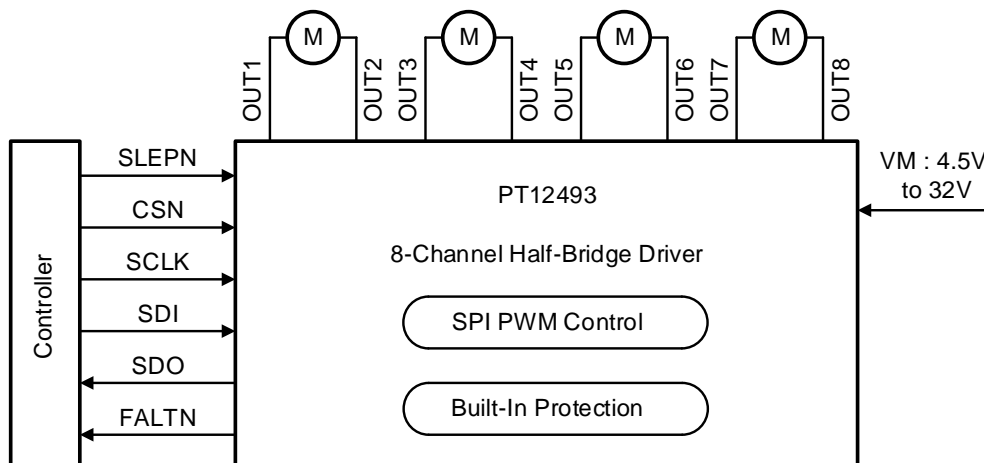
This device feature standard 16-bit, 5-MHz serial peripheral interface (SPI) with daisy chain capability for complete configuration and detailed diagnostics. The device has eight programmable PWM generators are integrated to allow for current limiting during motor operation or LED dimming control.

The device includes numerous protection and diagnostic features including an FALTN pin to alert the system when a fault occurs. The device features a low-current open load detection (OLD) mode to detect open-load conditions when the nominal load current is small and a passive OLD mode for offline OLD. The device is also fully-protected from short-circuit, under-voltage, and over-temperature conditions.

APPLICATIONS

- HVAC flap DC motors
- Side mirror adjustment and mirror fold
- LED applications
- Multiple brushed DC motors and solenoids

TYPICAL APPLICATION



FEATURES

- 8 half-bridge outputs
- 4.5-V to 32-V operating voltage
 - 40-V absolute maximum voltage
- 1-A RMS current for each output
 - 6-A maximum current for paralleled outputs
- Low-power sleep mode (1.5- μ A)
- Supports 3.3-V and 5-V logic inputs
- SPI for configuration and diagnostics
 - 5-MHz, 16-Bit SPI communication
 - Daisy chain functionality
- PWM generators programmable over SPI
 - Individual half-bridge PWM operation
 - Configurable for high-side, low-side, and H-bridge load driving
 - Supports 8-bit duty cycle resolution
- Integrated protection features with per channel detailed diagnostics over SPI
 - FALTN pin output
 - VM undervoltage lockout (UVLO)
 - VM overvoltage protection (OVP)
 - Logic supply power on reset (POR)
 - Overcurrent protection (OCP)
 - Enhanced open load detection (OLD)
 - Thermal warning and shutdown (OTW/OTSD)
- HTSSOP 24 pins package with exposed thermal pad

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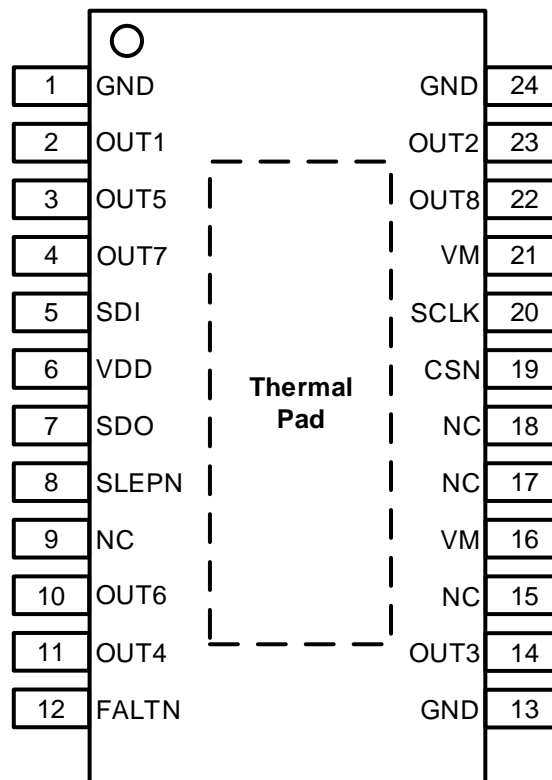
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ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT12493-HT	24 Pins, HTSSOP	PT12493-HT

PIN CONFIGURATION

PT12493, HTSSOP 24-Pin
Top View



PIN DESCRIPTION

PIN Name	I/O	Description	PIN NO.
GND	PWR	Device power ground. Connect the GND pin to the system ground.	1
OUT1	O	Half-bridge 1 output	2
OUT5	O	Half-bridge 5 output	3
OUT7	O	Half-bridge 7 output	4
SDI	I	Serial data input. Data is captured on the falling edge of the SCLK pin. Internal pull-down.	5
VDD	PWR	Logic power supply input. Connect a X5R or X7R, 0.1- μ F, VDD-rated ceramic capacitor and greater than or equal to 1- μ F bulk capacitance between the VDD and GND pins.	6
SDO	O	Serial data output. Data is shifted out on the rising edge of the SCLK pin.	7
SLEPN	I	Driver enable pin. When this pin is logic low the device goes to a low-power sleep mode. Internal pull-down.	8
NC	—	Not connected	9
OUT6	O	Half-bridge 6 output	10
OUT4	O	Half-bridge 4 output	11
FALTN	OD	Fault indicator output. This pin is pulled logic low during a fault condition and requires an external pull-up resistor.	12
GND	PWR	Device power ground. Connect the GND pin to the system ground.	13

OUT3	O	Half-bridge 3 output	14
NC	—	Not connected	15
VM	PWR	Main power supply input. Connect all VM pins together to the motor supply voltage. Connect a X5R or X7R, 0.1- μ F, VM-rated ceramic capacitor and greater than or equal to 10- μ F bulk capacitance between the VM and GND pins.	16
NC	—	Not connected	17
NC	—	Not connected	18
CSN	I	Serial chip selection. A logic low on this pin enables serial interface communication. Internal pull-up.	19
SCLK	I	Serial clock input. Serial data is shifted out and captured on the corresponding rising and falling edge on this pin. Internal pull-down.	20
VM	PWR	Main power supply input. Connect all VM pins together to the motor supply voltage. Connect a X5R or X7R, 0.1- μ F, VM-rated ceramic capacitor and greater than or equal to 10- μ F bulk capacitance between the VM and GND pins.	21
OUT8	O	Half-bridge 8 output	22
OUT2	O	Half-bridge 2 output	23
GND	PWR	Device power ground. Connect the GND pin to the system ground.	24
TH Pad	—	Expose thermal pad on the bottom side, connect to a board PCB copper plane with thermal vias for enhance heat dissipation.	-

BLOCK DIAGRAM

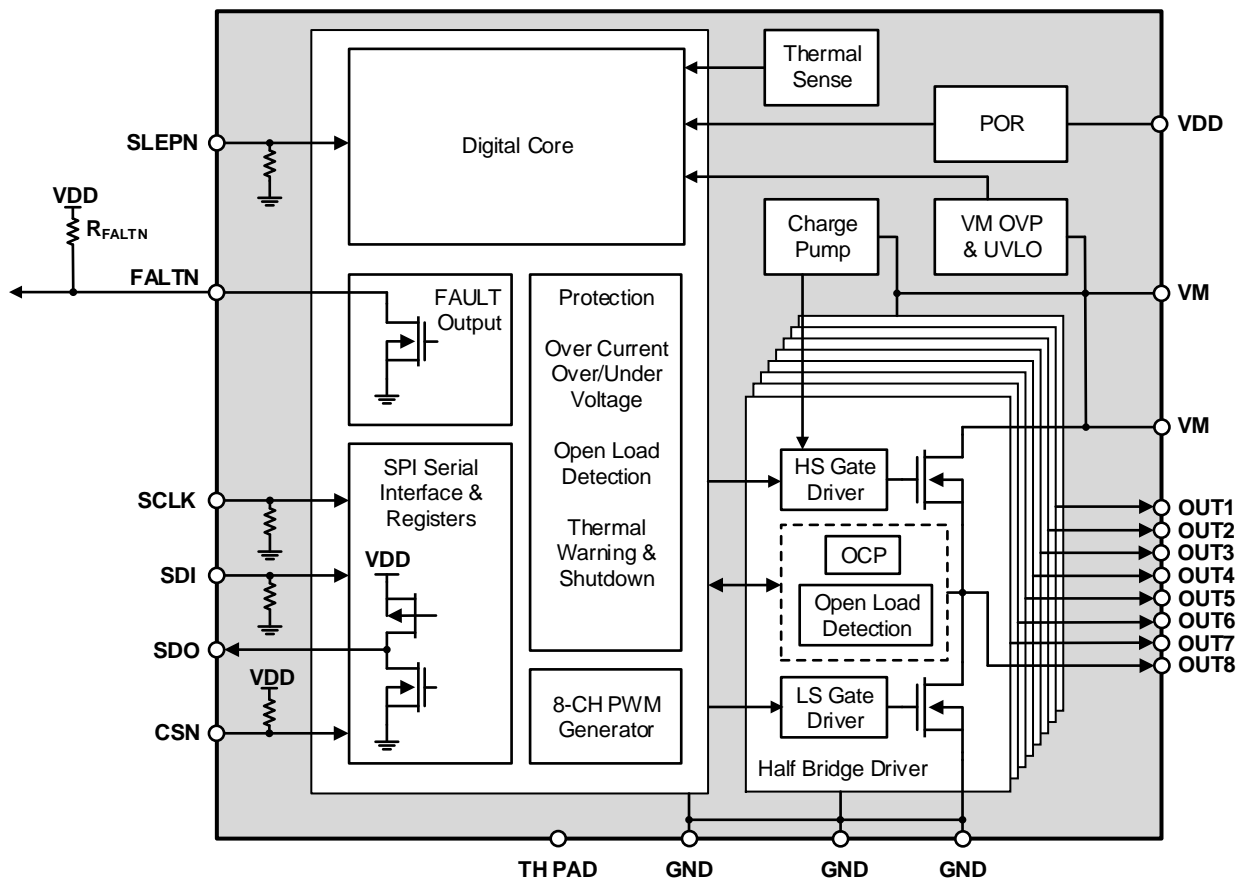


Figure 1, block diagram

FUNCTION DESCRIPTION

OVERVIEW

The PT12493 is 4.5V to 32V integrated multi half-bridge drivers which supports a maximum voltage of 40-V for load-dump scenario. The half-bridges are designed to support 1-Amp per half-bridge and 6-Amps from the VM/GND pins.

A standard 16-bit, 5-MHz serial peripheral interface (SPI) provides a simple method for configuring the various device settings and reading fault diagnostic information through an external controller. The device is also equipped with a daisy-chain functionality which allows connecting multiple devices using a single CSN line and saving on multiple resources.

This device has 8 internal PWM generators which can be mapped to any of the half-bridge through SPI registers. The PWM frequency (4 options) and duty (8-bit resolution) for each channel can be selected using the SPI registers. This PWM mode is useful for implementing the current control of motor or dimming control of LEDs.

The device also has numerous integrated protection features which protects the device in case of any abnormal scenario. The over-current protection (OCP) ensures the device protection in any short scenarios like the phase short, phase to ground short and phase to supply short conditions. Undervoltage lockout (UVLO) and overvoltage protection (OVP) ensures the driver operation in fluctuating voltages to support the crank-start and load-dump scenario in automotive applications. In addition to this, the open-load detection (OLD) feature ensure the proper load connection. All devices support active OLD, low-current OLD, and negative-current OLD. Passive OLD is only supported on PT12493 devices. Device faults are indicated on the FALTN pin, and detailed information is available in the device SPI registers.

The device integrates a spread spectrum clocking feature for both the internal digital oscillator and internal charge pump. This feature combined with programmable output slew-rate control minimizes the radiated emissions from the device.

The device is available in a 24-pin HTSSOP package with a thermal pad.

FEATURE DESCRIPTION

HALF BRIDGE DRIVERS

CONTROL MODES

The half-bridge drivers can be programmed to drive loads (motor, solenoids, LEDs) continuously (without PWM) or in chopping mode (with PWM) and in parallel operation for driving high current.

CONTINUOUS MODE (WITHOUT PWM)

The half-bridges are configured to operate in the continuous mode without using any PWM switching by default. Any high-side or low-side switch is switched on by individually setting the high-side enable bits (HBX_HS_EN) and low-side enable bits (HBX_LS_EN) in operation control registers (OP_CTRL_1, OP_CTRL_2 and OP_CTRL_3).

NOTE

If the high-side enable bit (HBX_HS_EN) and low-side enable bit (HBX_LS_EN) of a particular half-bridge is set high (shoot-through configuration), then the particular half-bridge driver will remain in Hi-Z state until the shoot-through condition is cleared.

The high-side and low-side enable bits of a particular half-bridge are configured to drive the motor in forward mode, reverse mode, brake mode and coast mode as shown in Table 1.

SLEPN	HALF-BRIDGE-1	HALF-BRIDGE-2	OUT1	OUT2	BRIDGE OPERATION (DC MOTOR)
0	HB1_HS_EN = Don't Care HB1_LS_EN = Don't Care	HB2_HS_EN = Don't Care HB2_LS_EN = Don't Care	Z	Z	Sleep Mode
1	HB1_HS_EN = 0 HB1_LS_EN = 0	HB2_HS_EN = 0 HB2_LS_EN = 0	Z	Z	Motor Coast
1	HB1_HS_EN = 1 HB1_LS_EN = 0	HB2_HS_EN = 0 HB2_LS_EN = 1	H	L	Forward Direction
1	HB1_HS_EN = 0 HB1_LS_EN = 1	HB2_HS_EN = 1 HB2_LS_EN = 0	L	H	Reverse Direction
1	HB1_HS_EN = 0 HB1_LS_EN = 1	HB2_HS_EN = 0 HB2_LS_EN = 1	L	L	Motor Brake (Low-Side)
1	HB1_HS_EN = 1 HB1_LS_EN = 0	HB2_HS_EN = 1 HB2_LS_EN = 0	H	H	Motor Brake (High-Side)
1	HB1_HS_EN = 1 HB1_LS_EN = 1	HB2_HS_EN = 1 HB2_LS_EN = 1	Z	Z	Motor Coast

Table 1. Motor Operation in Continuous Mode (Motor Connected between HB1 and HB2)

Figure 2 shows the bridge configuration for motor operation in forward direction with high-side FET of OUT1 and low-side FET of OUT2 in conducting state with current flowing from OUT1 to OUT2. Similarly, the motor operation in reverse direction is achieved by switching ON the high-side FET of OUT2 and low-side FET of OUT1 such that current flows from OUT2 to OUT1 as shown in Figure 3.

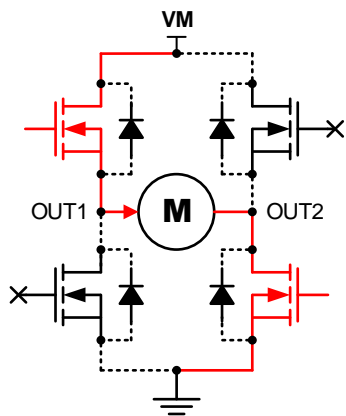


Figure 2. Continuous Mode (Forward Direction)

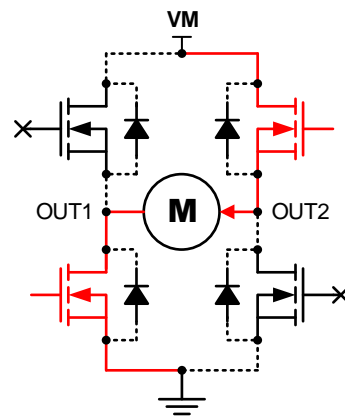


Figure 3. Continuous Mode (Reverse Direction)

Figure 4 and Figure 5 shows the bridge operation in coast mode with motor initially running in forward and reverse direction respectively. As shown in these figures, due to the energy stored in motor's inductance, the current will continue to flow in motor and take the path flow through the body diodes of FETs.

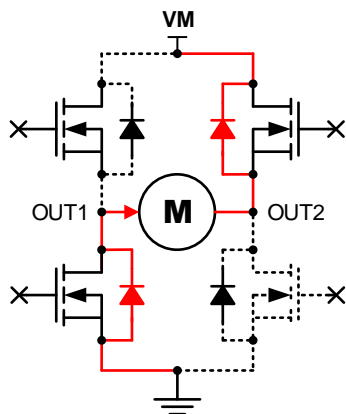


Figure 4. Continuous Mode (Coast - From Forward Direction)

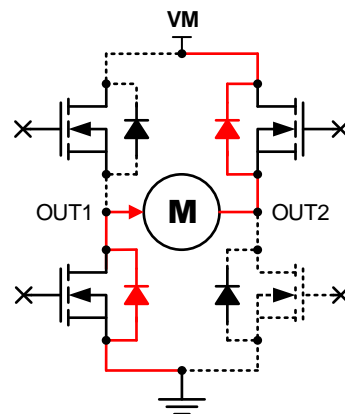


Figure 5. Continuous Mode (Coast- From Reverse Direction)

Figure 6 shows the low-side braking of the motor when both low-side FET's of the driver are turned ON. In this case, the motor is considered to be operating in forward direction (current flow from OUT1 to OUT2) and then braking is applied. Similarly, for the high-side braking, both high-side FET's of the driver are turned ON as shown in Figure 7.

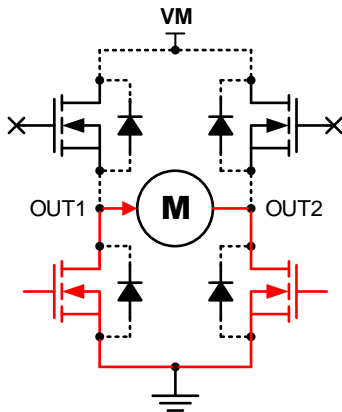


Figure 6. Continuous Mode (Brake - Low-Side)

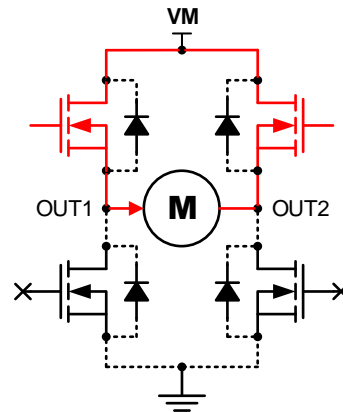


Figure 7. Continuous Mode (Brake - High-Side)

CHOPPING MODE (WITH PWM)

The half-bridges can be configured in the chopping mode by enabling the PWM switching on any particular half-bridge or both half-bridges. Each half-bridge can be mapped to any of the 4 PWM channels for which frequency and duty can be controlled independently. User has the flexibility to select the PWM frequency of channels out of 4 settings of 80-Hz, 100-Hz, 200-Hz and 2-kHz. Moreover, duty (8-bit resolution) of the 4 PWM generators can be adjusted independently.

The PWM chopping mode operation is done in five steps as follows and explained in detail below.

1. PWM Configuration
2. Free-Wheeling Mode (Synchronous Rectification) Disable / Enable
3. PWM Channels Mapping
4. PWM Channels Configuration (PWM Frequency and PWM Duty)
5. Half-Bridge Enable

PWM CONFIGURATION

The operation of selected half-bridge to operate in continuous mode or chopping mode (PWM mode) is selected using the PWM control register (PWM_CTRL_1 and PWM_CTRL_2). The HBX_PWM bit in PWM control register is set to enable the PWM switching in half-bridge.

NOTE

The default mode of any half-bridge is continuous mode. If the corresponding HBx_PWM bit in PWM_CTRL_X register is not set, then the particular half-bridge will operate in continuous mode.

FREE-WHEELING MODE (SYNCHRONOUS RECTIFICATION) DISABLE / ENABLE

The synchronous rectification of the half-bridge operating in PWM can be enabled by setting the HBX_FW bit in free-wheeling control registers (FW_CTRL_1 and FW_CTRL_2). Figure 8 shows the operation of the driver when the synchronous rectification mode is disabled. As shown in this figure, during the PWM off time, the high-side diode of the OUT2 conducts to close the current path required for motor.

When synchronous rectification mode is enabled, if either of the low-side or high-side of the half-bridge operates in the PWM switching, then the other switch of the same half-bridge operates in complementary fashion. Figure 9 shows such example of the synchronous rectification, where the high-side FET of OUT2 half-bridge is turned ON when the low-side FET of same half-bridge is turned off in a PWM cycle.

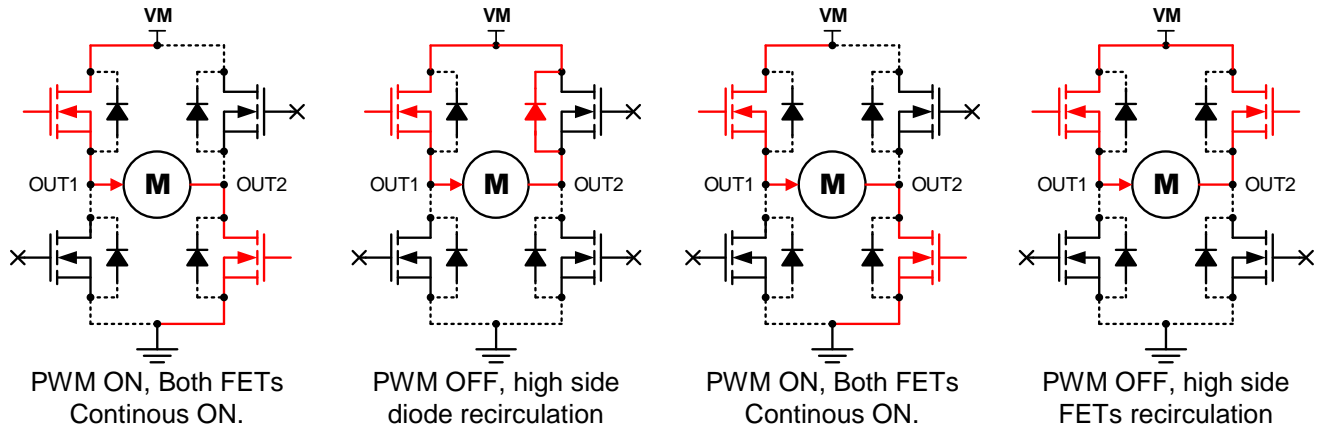


Figure 8. PWM Mode (Synchronous Rectification = OFF)

Figure 9. PWM Mode (Synchronous Rectification = ON)

NOTE

The default mode of any half-bridge is asynchronous rectification mode. If the corresponding bit in FW_CTRL_X register is not set, then the particular half-bridge will operate in asynchronous rectification mode.

PWM CHANNELS MAPPING

PT12493 includes 8 PWM generators which can be mapped to any of the OUTX half bridge outputs using the PWM map control registers. The HBx_PWM_MAP bits in the PWM_MAP_CTRL_X registers are used to map any of the 8 channels in PT12493 to the OUTX outputs as shown in Table 2.

HBX_PWM MAP BITS	PWM CHANNEL
HBX_PWM_MAP = 00b	Channel 1 Selected for OUTX
HBX_PWM_MAP = 01b	Channel 2 Selected for OUTX
HBX_PWM_MAP = 10b	Channel 3 Selected for OUTX
HBX_PWM_MAP = 11b	Channel 4 Selected for OUTX

Table 2. PWM Mapping of PT12493

NOTE

Any half-bridge is mapped to PWM channel 1 by default.

PWM CHANNELS CONFIGURATION (PWM FREQUENCY AND PWM DUTY)

The frequency and duty of each PWM generator can be controlled independently. The PWM_CHx_FREQ bits of PWM frequency control register (PWM_FREQ_CTRL) is used to select the frequency of PWM generator as shown in Table 3. The PWM duty of each channel is controlled by the PWM duty control register (PWM_DUTY_CTRL_X).

HBX_PWM MAP BITS	PWM CHANNEL
PWM_CHx_FREQ = 00b	80 Hz
PWM_CHx_FREQ = 01b	100 Hz
PWM_CHx_FREQ = 10b	200 Hz
PWM_CHx_FREQ = 11b	2000 Hz

Table 3. PWM Frequency

HALF-BRIDGE ENABLE

The four steps of PWM mode enable, free-wheeling mode configuration, PWM channel mapping and PWM channels configuration ensure the proper configuration of PWM mode. Once the half-bridge is configured for

the PWM generation, the half-bridge is enabled by enabling either of the high-side or low-side switch by individually setting the high-side enable bits (HBX_HS_EN) or low-side enable bits (HBX_LS_EN) in operation control registers (OP_CTRL_1, OP_CTRL_2 and OP_CTRL_3).

NOTE

The PWM is applicable to either of the high-side or low-side switch depending upon the HBX_HS_EN and HBX_LS_EN bits in OP_CTRL_X registers. In synchronous rectification mode, the opposite side switch will conduct in PWM off time.

PARALLEL MODE (CONTINUOUS OPERATION)

Parallel mode in PT12493 device is implemented to support higher current loads which cannot be supported by a single channel. This mode can also be used for reducing the effective on-state resistance ($R_{DS(ON)}$) for achieving a better thermal performance of the device.

The configuration of various mode is very similar to the single half-bridge operation as explained in *Continuous Mode (Without PWM)* section. Considering six half-bridges for the parallel operation (OUT1, OUT2, OUT3 as group - 'X' and OUT4, OUT5, OUT6 as group 'Y'), various modes can be summarized in Table 4.

SLEPN	HALF-BRIDGE-1 HALF-BRIDGE-2 HALF-BRIDGE-3 (X)	HALF-BRIDGE-4 HALF-BRIDGE-5 HALF-BRIDGE-6 (Y)	OUT1 OUT2 OUT3	OUT4 OUT5 OUT6	BRIDGE OPERATION (DC MOTOR)
0	HBX_HS_EN = Don't Care HBX_LS_EN = Don't Care	HBX_HS_EN = Don't Care HBX_LS_EN = Don't Care	Z	Z	Sleep Mode
1	HBX_HS_EN = 0 HBX_LS_EN = 0	HBX_HS_EN = 0 HBX_LS_EN = 0	Z	Z	Motor Coast
1	HBX_HS_EN = 1 HBX_LS_EN = 0	HBX_HS_EN = 0 HBX_LS_EN = 1	H	L	Forward Direction
1	HBX_HS_EN = 0 HBX_LS_EN = 1	HBX_HS_EN = 1 HBX_LS_EN = 0	L	H	Reverse Direction
1	HBX_HS_EN = 0 HBX_LS_EN = 1	HBX_HS_EN = 0 HBX_LS_EN = 1	L	L	Motor Brake (Low-Side)
1	HBX_HS_EN = 1 HBX_LS_EN = 0	HBX_HS_EN = 1 HBX_LS_EN = 0	H	H	Motor Brake (High-Side)
1	HBX_HS_EN = 1 HBX_LS_EN = 1	HBX_HS_EN = 1 HBX_LS_EN = 1	Z	Z	Motor Coast

**Table 4. Motor Operation in Parallel Mode (Continuous Operation)
(with Motor Connected between OUT1/2/3 and OUT4/5/6)**

NOTE

For parallel mode operation, the device operation under safe operating area (SOA) is recommended for supply voltage, $V_{VM} \leq 20\text{-V}$, $HBX_SR = HBX_SR = 1b$, $t_{OCP} \leq 10\text{-}\mu\text{s}$ and $PL_MODE_EN = 01b$.

Figure 10 shows four half-bridges (OUT1, OUT2, OUT3 and OUT4) operating as a parallel high-side switch and other four half-bridges (OUT5, OUT6, OUT7 and OUT8) are operating as a parallel low-side switch for achieving a forward motor operation. Similarly, the reverse direction of motor is achieved by operation of OUT1, OUT2, OUT3 and OUT4 as a parallel low-side switch and other four half-bridges OUT5, OUT6, OUT7 and OUT8) as parallel high-side switch as shown in Figure 11.

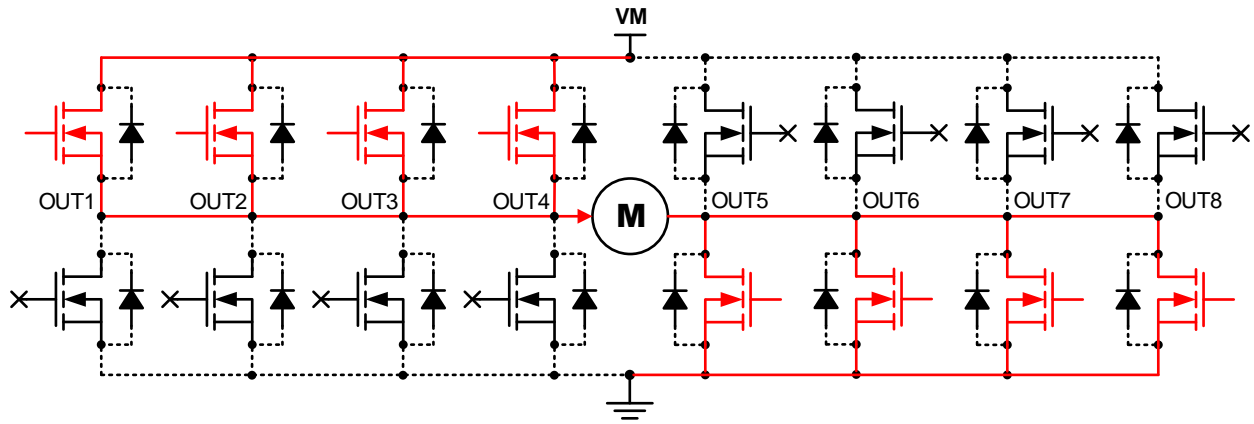


Figure 10. Parallel Mode (Forward Direction)

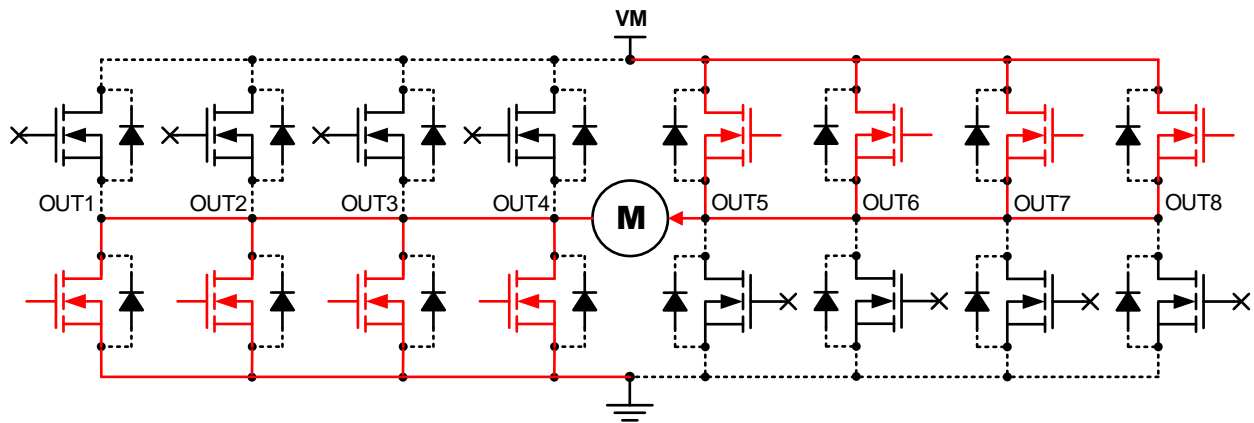


Figure 11. Parallel Mode (Reverse Direction)

Figure 12 and Figure 13 shows the bridge operation in coast mode with motor initially running in forward and reverse direction respectively. As shown in these figures, the body diodes of the FETs conduct to continue the current flow path due to energy stored in motor's inductance.

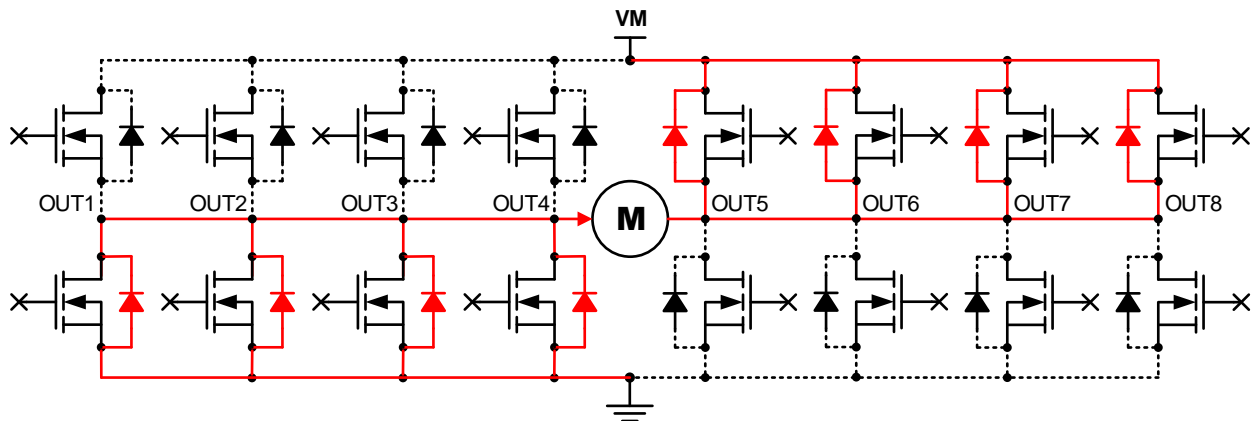


Figure 12. Parallel Mode (Coast from Forward Direction)

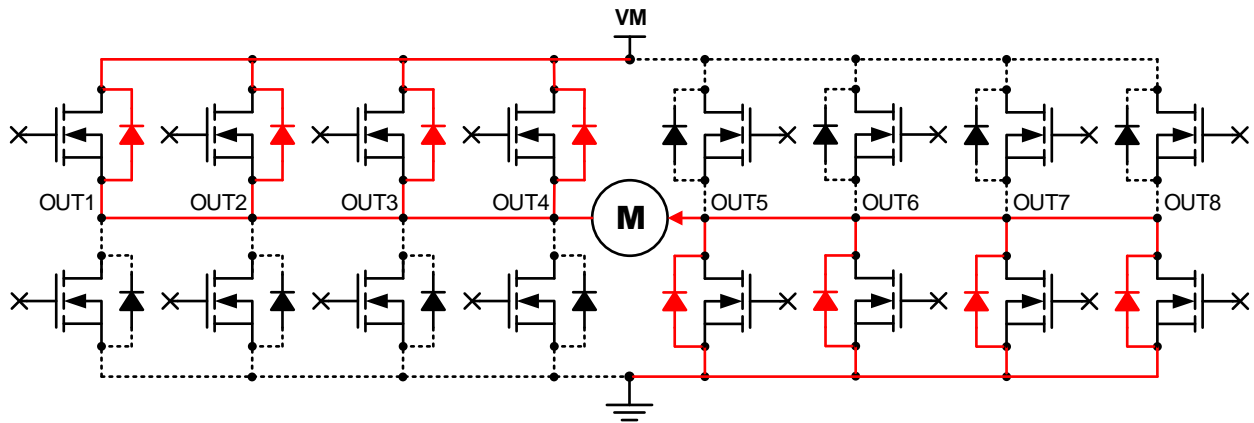


Figure 13. Parallel Mode (Coast from Reverse Direction)

The low-side braking of the motor during all the low-side FET's of the driver turning ON is shown in Figure 14. In this case, the motor is considered to be operating in forward direction (current flow from OUT1/2/3 to OUT4/5/6) and then braking is applied. Similarly, for the high-side braking, all high-side FET's of the driver are turned ON as shown in Figure 15.

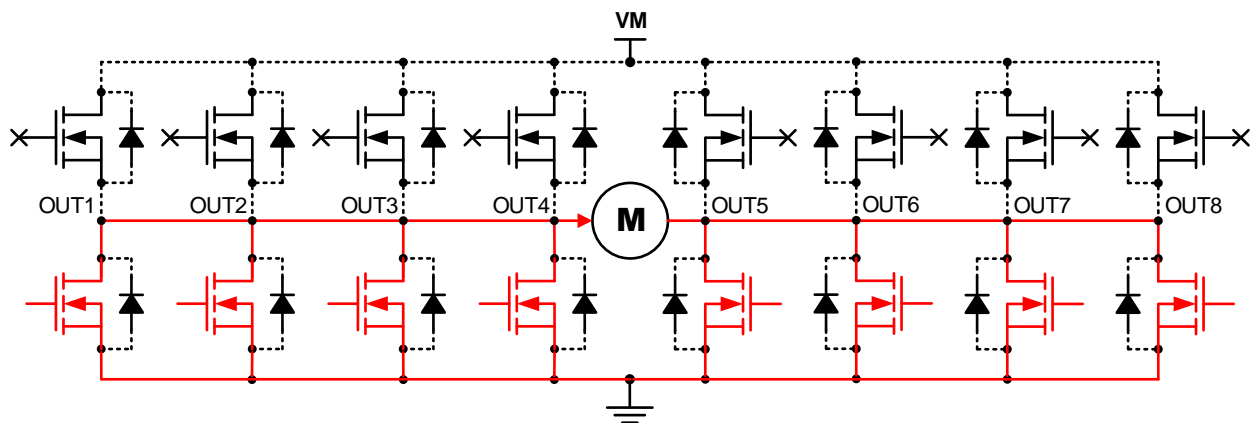


Figure 14. Parallel Mode (Brake - Low-Side)

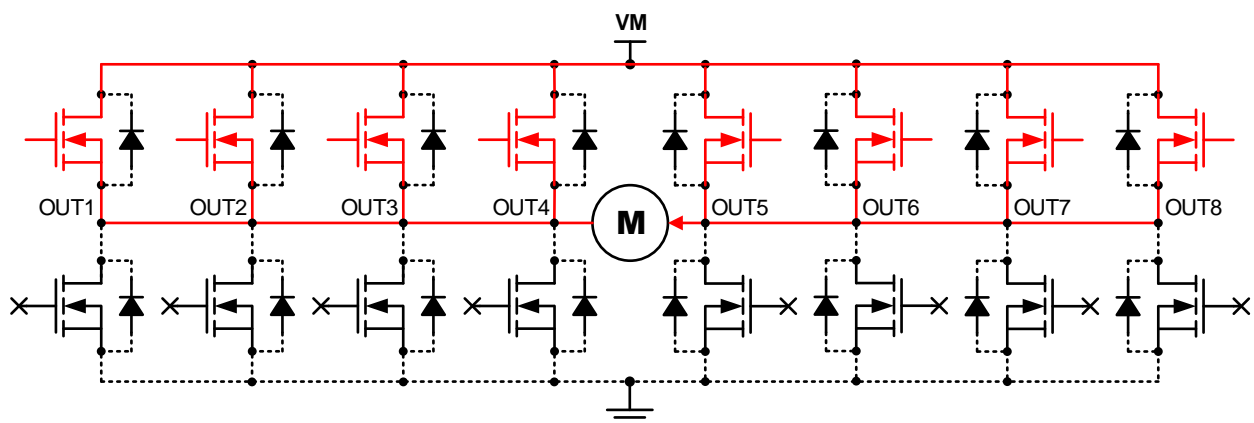


Figure 15. Parallel Mode (Brake - High-Side)

PARALLEL MODE (PWM OPERATION)

The half-bridges connected in parallel mode can be configured in the chopping mode by enabling the PWM switching on any particular group of high-side or low-side half-bridges or both group of half-bridges. For PWM operation in parallel mode, all half-bridges are to be mapped to a single PWM channel selected from any of the 4 PWM channels to avoid any delay in the PWM durations which can lead to undesired OCP condition. The user has the flexibility to select the PWM frequency of channels out of 4 settings of 80-Hz, 100-Hz, 200-Hz and 2-kHz and the duty adjustment which supports 8-bit resolution. Following steps enable the PWM operation with driver connected for parallel mode and are explained below.

1. PWM Configuration
2. Free-Wheeling Mode (Synchronous Rectification) Disable / Enable
3. PWM Channels Mapping
4. PWM Channels Configuration (PWM Frequency and PWM Duty)
5. PWM Generators Disable
6. Half-Bridge Enable
7. PWM Generators Enable

PWM CONFIGURATION

The PWM control register (PWM_CTRL_1 and PWM_CTRL_2) are used to select the operation of particular half-bridges in the PWM mode. Considering a case for the motor movement in forward direction as shown in Figure 12, with low-side FETs of OUT4, OUT5 and OUT6 operating in PWM mode. The HBX_PWM bit in PWM control register is set to enable the PWM switching in selected half-bridges as shown below:

- HB4_PWM = 1b
- HB5_PWM = 1b
- HB6_PWM = 1b

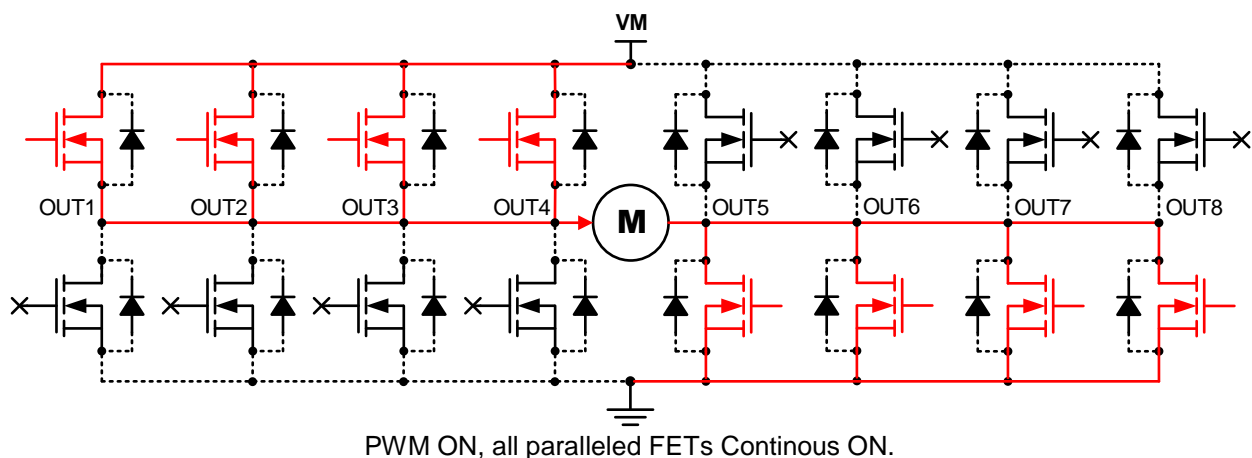
FREE-WHEELING MODE (SYNCHRONOUS RECTIFICATION) DISABLE / ENABLE

The synchronous rectification of the half bridges operating in PWM mode (OUT4, OUT5 and OUT6) are enabled by setting the corresponding HBX_FW bits in free-wheeling control register (FW_CTRL_1 and FW_CTRL_2). By default, the synchronous rectification mode is disabled.

- HB4_FW = 1b
- HB5_FW = 1b
- HB6_FW = 1b

Figure 16 shows the parallel operation of half-bridges in PWM mode with synchronous rectification disabled. As shown in this figure, during the PWM off time, the high-side diode of the OUT4, OUT5 and OUT6 conducts to close the current path required for motor.

When synchronous rectification mode is enabled, the high-side FETs of OUT4, OUT5 and OUT6 starts conducting during the PWM OFF time to close the motor current path as shown in Figure 17.



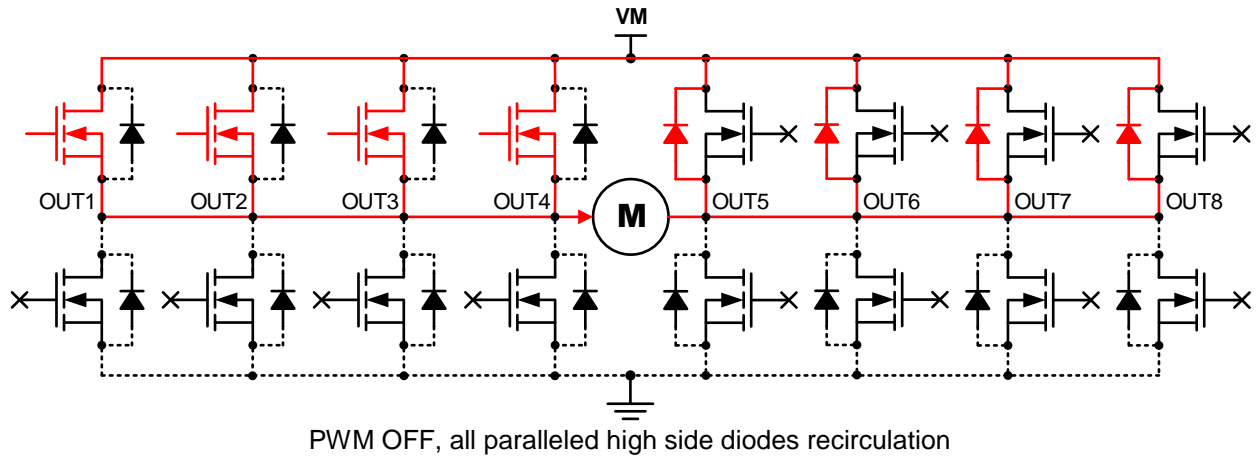


Figure 16. Parallel Mode (PWM with Synchronous Rectification = OFF)

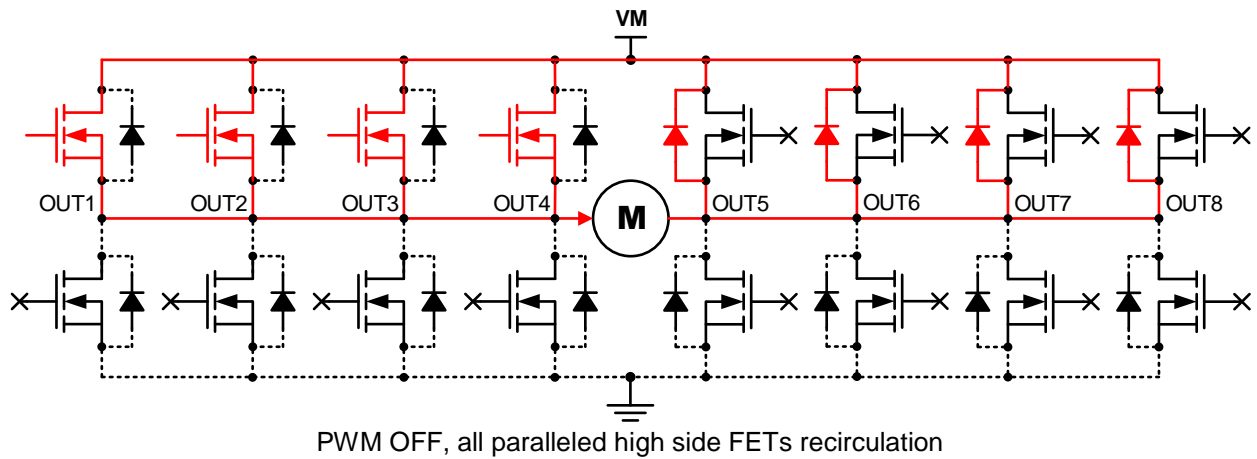
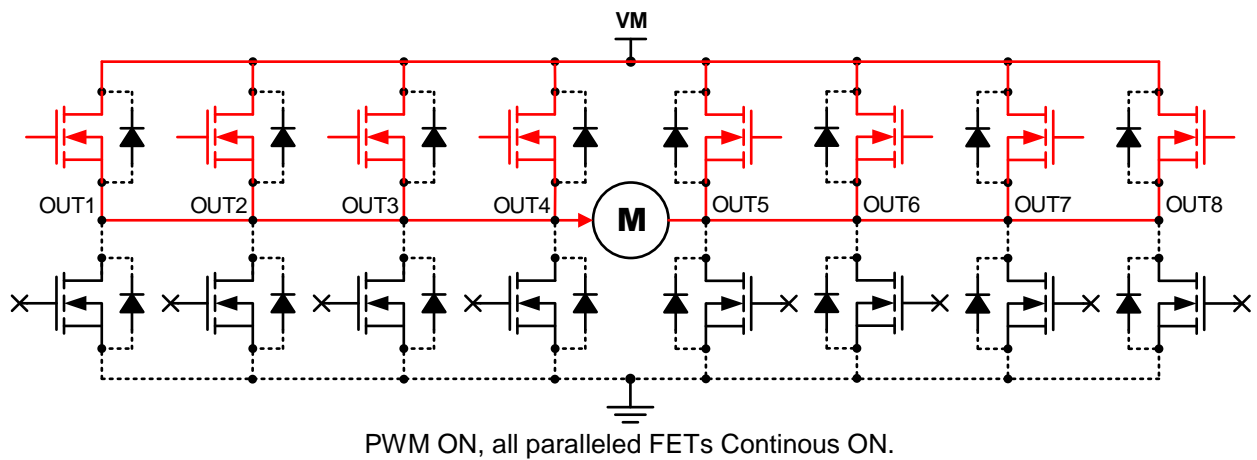


Figure 17. Parallel Mode (PWM with Synchronous Rectification = ON)

PWM CHANNELS MAPPING

The low-side FET's of half-bridges OUT4, OUT5 and OUT6 are mapped to any of the PWM generator by using the HBX_PWM_MAP bits in PWM mapping control registers. For parallel operation, all the half-bridges operating in PWM mode is mapped to a single PWM generator. Considering that PWM generator-4 is used for the mapping of half-bridges, following bits of the PWM_MAP_CTRL_X registers are affected:

- HB4_PWM_MAP = 11b
- HB5_PWM_MAP = 11b
- HB6_PWM_MAP = 11b

NOTE

If the PWM of any channel is enabled, then it is mapped to PWM generator-1 by default.

PWM CHANNELS CONFIGURATION (PWM FREQUENCY AND PWM DUTY)

The PWM_CHx_FREQ bits of PWM frequency control registers (PWM_FREQ_CTRL_X) is used to select the frequency of PWM generator. Moreover, the PWM duty of each channel is controlled by the PWM duty control register (PWM_DUTY_CTRL_X). Considering a frequency of 2-kHz is selected for the PWM operation (for PWM Generator-4), following frequency control and duty control registers are effected:

- PWM_CH4_FREQ = 11b
- PWM_CH4_FREQ = '8-bit duty'

PWM GENERATORS DISABLE

The PWM generators are disabled to ensure that all the half-bridges are turned-on at same time to avoid false OCP conditions for supporting higher current operation. The false OCP condition can arise due to the minimum time required for the SPI delay to switch on various half-bridges available in different registers. This can cause higher current (OCP condition) in one of the paralleled half-bridge while other half-bridge turning ON is delayed to the SPI register write delay and the propagation delay. Therefore, this sequence includes disabling the PWM generators initially, then enabling half-bridges and followed by enabling the PWM generators to avoid such issue. The PWM generator-4 is disabled by using the following command in the PWM_CTRL_X registers:

PWM_CH4_DIS = 1b

NOTE

All PWM generators are enabled by default (Default value of PWM_CTRL_X registers is 0h).

HALF-BRIDGE ENABLE

Once the PWM generators are disabled, the high-side and low-side FETs in half-bridges to be paralleled are enabled. High-side switches (connected in parallel) operating in continuous mode are enabled using the following bits in the OP_CTRL_X registers:

- HB1_HS_EN = 1b
- HB2_HS_EN = 1b
- HB3_HS_EN = 1b

Moreover, the low-side switches (connected in parallel) operating in PWM mode are enabled using the following bits in the OP_CTRL_X:

- HB4_LS_EN = 1b
- HB5_LS_EN = 1b
- HB6_LS_EN = 1b

PWM GENERATORS ENABLE

After the half-bridges are enabled, the PWM generators are also enabled for tuning-on the respective FETs operating in PWM mode. For this case, the low-side FETs of OUT4, OUT5 and OUT6 are turned ON for PWM operation connected to PWM generator-4. The PWM generator is enabled by the bits in the PWM_CTRL_X registers as shown:
PWM_CH4_DIS = 0b

HALF-BRIDGE DRIVE ARCHITECTURE

SLEW RATE

An adjustable gate-drive current control to the MOSFETs of half-bridges is implemented to achieve the slew rate control. The MOSFET VDS slew rates are a critical factor for optimizing radiated emissions, energy and duration of diode recovery spikes and switching voltage transients related to parasites. These slew rates are predominantly determined by the rate of gate charge to internal MOSFETs as shown in Figure 18.

The slew rate of each half-bridge can be adjusted by HBX_SR bits in Slew Rate control register (SR_CTRL_1 and SR_CTRL_2). Each half-bridge can be selected to a slew rate of 0.6-V/ μ s or 2.5-V/ μ s. The slew rate is calculated by the rise-time and fall-time of the voltage on OUTx pin as shown in Figure 19.

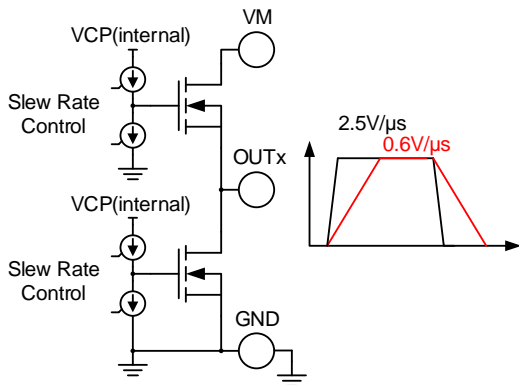


Figure 18. Slew Rate Circuit Implementation

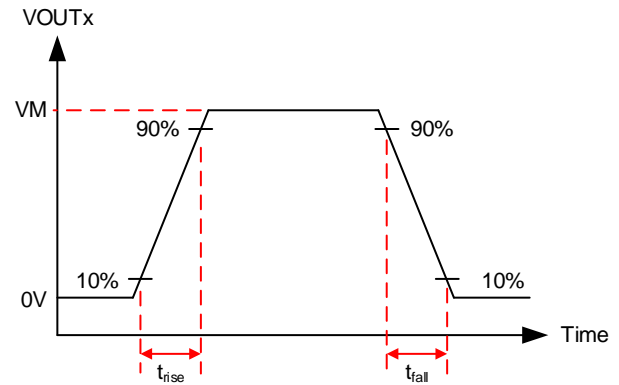


Figure 19. Slew Rate Timings

CROSS CONDUCTION (DEAD TIME)

The device is fully protected for any cross conduction of MOSFETs. In half-bridge configuration, the operation of high-side and low-side MOSFETs are ensured to avoid any shoot through currents by inserting a dead time (t_{dead}). This is implemented by sensing the gate-source voltage (V_{GS}) of the high-side and low-side MOSFETs and ensured that V_{GS} of high-side MOSFET has reached below turn-off levels before switching on the low-side MOSFET of same half-bridge as shown in Figure 20 and Figure 21.

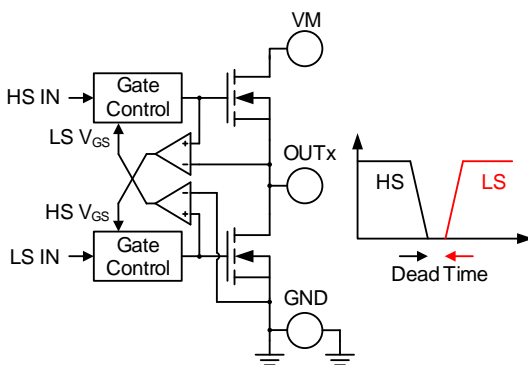


Figure 20. Cross Conduction Protection

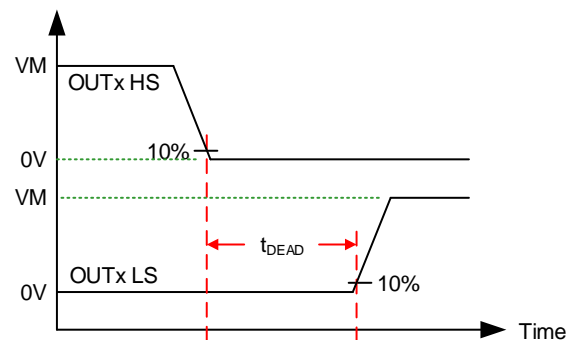


Figure 21. Dead Time

PROPAGATION DELAY

Propagation delay refers to the delay time from SPI valid condition to OUTx going high (10% level) as shown in Figure 22. The propagation constitutes of three major parameters.

1. Digital delay for SPI command decode.
2. Analog delay for driver switch-on and gate current charging delay.
3. Slew rate delay for OUTx node to reach 10% of the final settling value.

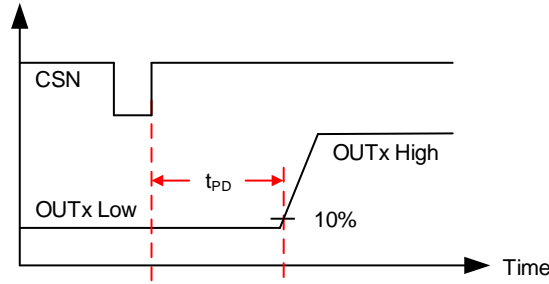


Figure 22. Propagation Delay

PIN DIAGRAMS

This section presents the I/O structure of all digital input and output pins.

Logic Level Input Pin (SLEPN, SCLK and SDI)

Figure 23 shows the input structure for the logic levels pins, SLEPN, SCLK and SDI. The input can be with a voltage or external resistor. It is recommended to put SCLK and SDI pin low in device sleep mode to reduce leakage current through internal pull-down resistors.

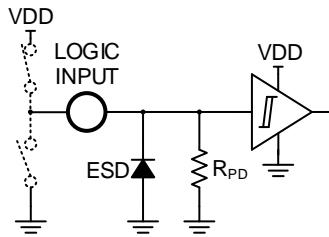


Figure 23. Logic Level Input Pin Structure (SLEPN, SCLK and SDI)

Push Pull Output Pin (SDO)

Figure 24 shows the structure of push-pull pin, SDO.

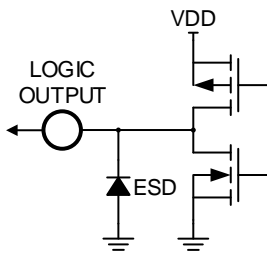


Figure 24. Push Pull Output Pin Structure (SDO)

Logic Level Input Pin (CSN)

Figure 25 shows the input structure for the logic levels pin, CSN. The input can be with a voltage or external resistor

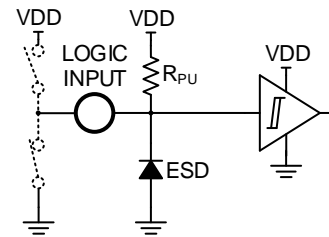


Figure 25. Logic Level Input Pin Structure (CSN)

Open Drain Output Pin (FALTN)

Figure 26 shows the structure of the open-drain output pin, FALTN. The open-drain output requires an external pullup resistor to function properly.

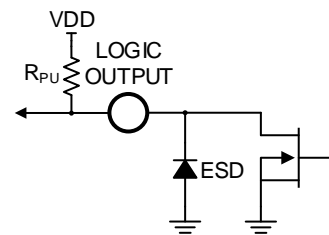


Figure 26. Open Drain Output Pin Structure (FALTN)

PROTECTION CIRCUITS

The PT12493 device is fully protected against undervoltage, overcurrent, and over-temperature events.

VM SUPPLY UNDERVOLTAGE LOCKOUT (UVLO)

If at any time the input supply voltage on the VM pin falls below the V_{UVLO} threshold, all of the half-bridges are disabled, the charge pump is disabled, and the FALTN pin is driven low as shown in Figure 27. The UVLO bit is also latched high in the IC status (IC_STAT) register. Normal operation resumes (driver operation and the FALTN pin is released) when the VM undervoltage condition is removed. The UVLO bit remains set until cleared through the CLR_FLT bit.

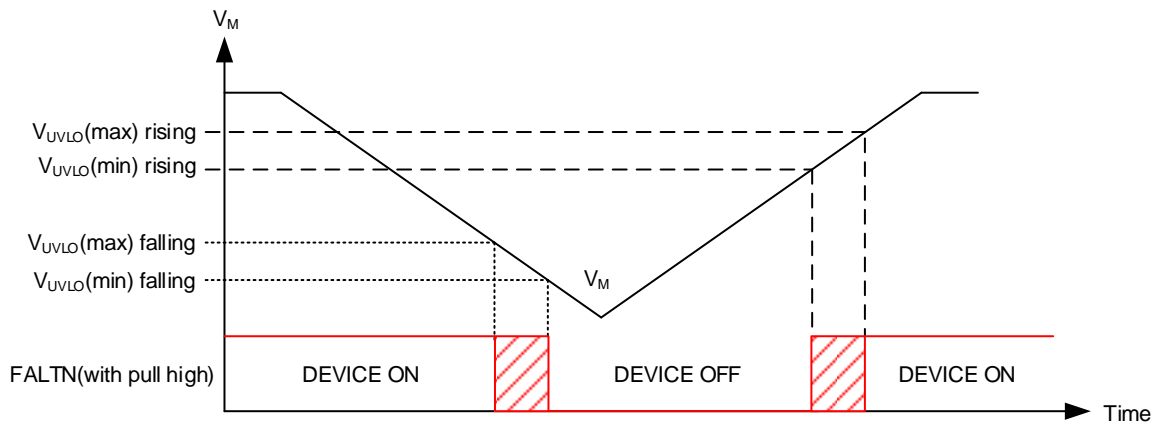


Figure 27. VM UVLO Operation

VM SUPPLY OVERVOLTAGE PROTECTION (OVP)

If at any time the input supply voltage on the VM pin rises above the V_{OVP} threshold, all of the half-bridges are disabled, the charge pump is disabled, and the FALTN pin is driven low as shown in Figure 28. The OVP bit is also latched high in the IC status (IC_STAT) register. Normal operation resumes (driver operation and the FALTN pin is released) when the VM overvoltage condition is removed. The OVP bit remains set until cleared through the CLR_FLT bit.

An extended overvoltage operation is also supported in this device for higher over-voltage range up to 32-V. This operation is enabled by setting the EXT_OVP bit in the configuration (CONFIG_CTRL) register.

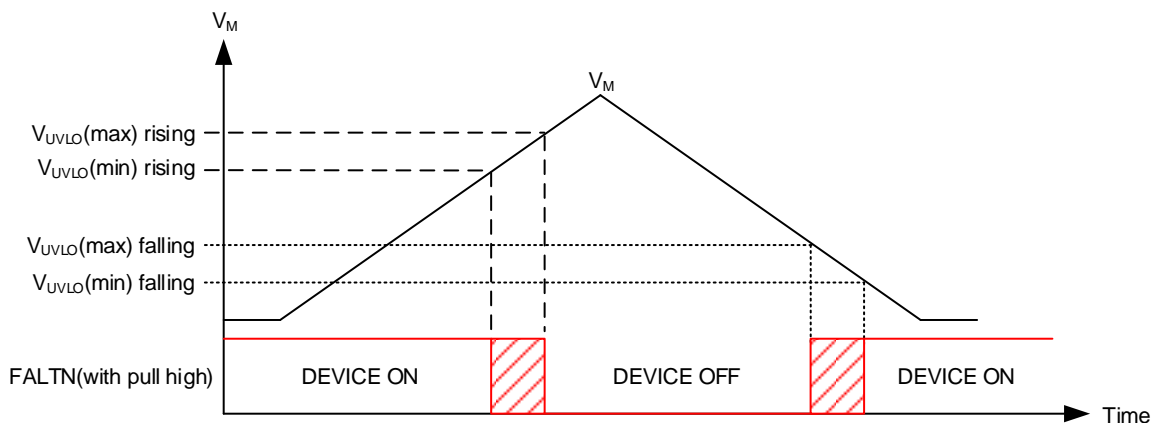


Figure 28. Over Voltage Protection

LOGIC SUPPLY POWER ON RESET (POR)

If at any time the input logic supply voltage on the VDD pin falls below the V_{POR} threshold or the SLEPN pin is toggled (high to low), all of the half-bridges are disabled and the charge pump is disabled, as shown in Figure 29. Normal operation resumes (driver operation) when the VDD undervoltage condition is removed or the SLEPN pin is latched high. The NPOR bit is reset and latched low in the IC status (IC_STAT) register once the device presumes VDD. The NPOR bit remains in reset condition until cleared through the CLR_FLT bit.

If the device has successfully waked up, then the NPOR bit is automatically latched high once the CLR_FLT command is issued.

NOTE

NPOR is not reported to FALTN pin.

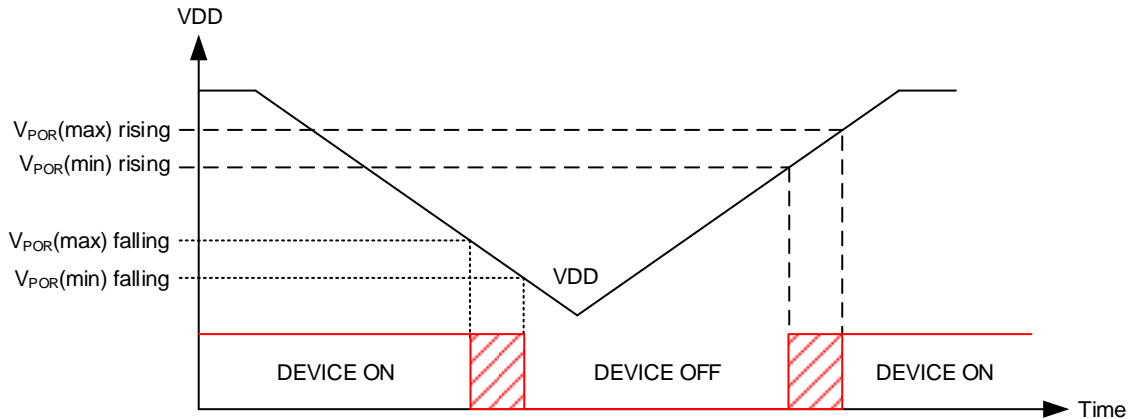


Figure 29. VDD UVLO Operation

OVERCURRENT PROTECTION (OCP)

A current-limit circuit on each MOSFET limits the current through the MOSFET by removing the gate drive signal. If this current limit stays active for longer than the t_{OCP} deglitch time, the high-side and the low-side FETs in the corresponding half bridge are disabled and the FALTN pin is driven low. The OCP bit in the IC status (IC_STAT) register and corresponding bit in overcurrent protection status register (OCP_STAT_X) register is latched high. The charge pump remains active during this condition. The OCP bit in the IC status (IC_STAT) register and corresponding bits (HBX_HS_OCP / HBX_LS_OCP) in overcurrent protection status register (OCP_STAT_X) register remains set until cleared through the CLR_FLT bit.

User also has the programmability of disabling the OCP fault on the FALTN pin by setting the OCP_REP bit in the CONFIG_CTRL register.

The device also provides two slew-rate options for the device turn-off during an OCP event which can be programmed via the PL_MODE_EN bits in OLD_CTRL_2 register. The default option (PL_MODE_EN = 00b) is the faster slew rate option (typical around $1\mu s$) which can be used for the single bridge operation. The slower option (PL_MODE_EN = 01b) provides a slower slew rate (half-bridge slew rate, HBX_SR) which can be used for the higher current applications in device parallel mode operation.

Drive Current	BRIDGE CONFIGURATION	REGISTER SETTINGS	BRIDGE STATE	FALTN PIN		BITS AFFECTED	RECOVERY
				OCP_REP = 0	OCP_REP = 1		
$I_{LOAD} < I_{OCP}$	OUT1 High-Side ON	HB1_HS_EN = 1	ENABLED	HIGH	HIGH	N/A	N/A
	OUT2 Low-Side ON	HB1_LS_EN = 1	ENABLED	HIGH	HIGH		
$I_{LOAD} < I_{OCP}$	Full Bridge (OUT1/2) Forward Direction	HB1_HS_EN = 1 HB2_LS_EN = 1	ENABLED	HIGH	HIGH		
	Full Bridge (OUT1/2) Reverse Direction	HB1_LS_EN = 1 HB2_HS_EN = 1	ENABLED	HIGH	HIGH		
I_{SHORT} or $I_{LOAD} > I_{OCP}$	OUT1 High-Side ON OUT1 Short to GND	HB1_HS_EN = 1	Hi-Z	LOW	HIGH	OCP = 1 (IC_STAT) HB1_HS_OCP = 1	OCP Condition Removed CLR_FLT=1
	OUT1 Low-Side ON OUT1 Short to VM	HB1_LS_EN = 1	Hi-Z	LOW	HIGH	OCP = 1 (IC_STAT) HB1_LS_OCP = 1	
I_{SHORT} or $I_{LOAD} > I_{OCP}$	Full Bridge (OUT1/2) Forward Direction OUT1 / OUT2 Short	HB1_HS_EN = 1 HB2_LS_EN = 1	Hi-Z	LOW	HIGH	OCP = 1 (IC_STAT) HB1_HS_OCP = 1 or HB2_LS_OCP = 1 ⁽¹⁾	
	Full Bridge (OUT1/2) Reverse Direction OUT1 / OUT2 Short	HB1_LS_EN = 1 HB2_HS_EN = 1	Hi-Z	LOW	HIGH	OCP = 1 (IC_STAT) HB1_LS_OCP = 1 or HB2_HS_OCP = 1 ⁽²⁾	

(1) Either of the HB1_HS_OCP or HB2_LS_OCP will set depending upon which half-bridge OCP trigger first.
(2) Either of the HB1_LS_OCP or HB2_HS_OCP will set depending upon which half-bridge OCP trigger first.

Table 5. Overcurrent Protection

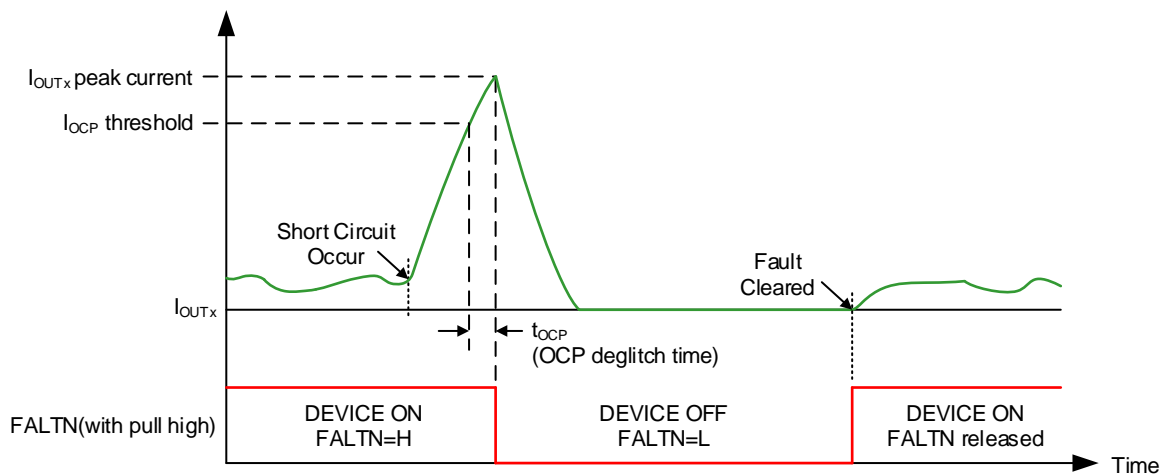


Figure 30. Over Current Protection

OPEN-LOAD DETECTION (OLD)

The PT12493 devices implement multiple open-load detection schemes to allow the controller to determine if a load is connected to the OUTX terminals. The OLD schemes available in PT12493 are listed below. Table 6 summarizes the use-cases for each OLD scheme.

- Low-Current Active OLD
- Negative-Current Active OLD
- Passive OLD

	PASSIVE OLD	ACTIVE OLD	LOW-CURRENT ACTIVE OLD	NEGATIVE-CURRENT ACTIVE OLD
When is it used	Detects open-load condition prior to enabling the outputs	Detects the open-load condition while driving a load	Detects the open-load condition while driving a load with small operating current	Detects the open-load condition during current re-circulation (on high-side or low-side) when synchronous rectification is enabled for both half-bridge and full-bridge configurations
State of OUTx for valid OLD	Hi-Z (outputs disabled)	H/L	L	H/L
OLD Trigger Condition	$V_{OLx_HS(+)} > V_{OLx_HS}$ or $V_{OLx_LS(-)} < V_{OLx_LS}$	$I_{OUTX} < I_{OLD}$	$I_{OUTX} < I_{OLD_LOW}$	$I_{OUTX} > -I_{OLD_NEG}$ $I_{OUTX} < I_{OLD}$
Tradeoffs	Passive OLD sequence is not enabled if any other fault other than OCP/OLD is present.	A false flag can occur during current re-circulation if synchronous rectification is ON. Enabling Negative-current OLD will solve this. A false flag can also occur if the operating current for the load is small (below I_{OLD} threshold). See Low-current OLD for solution.	Only applicable for the current flowing in the low-side FETs. The I_{OCP} for the low-side FET is also reduced by 11 times. The $R_{DS(ON)}$ of the low-side FET will increase by 11 times, hence the thermal performance has to be monitored.	Only functional during current re-circulation, however it works in conjunction with active OLD. This feature is not needed if synchronous rectification is disabled.
Can be used with other OLD schemes	No	Negative-current OLD and low-current OLD	Normal current Active OLD and negative-current OLD	Normal current Active OLD and low-current OLD

Table 6. Summary of OLD features

Active OLD

Active OLD can identify an open-load condition on the OUTX pins while driving a load. As shown in Figure 31, the DRV89xx identifies an open-load fault condition when the current through the MOSFET (I_{OUTX}) is lower than the open-load current threshold (I_{OLD}) for longer than the open-load deglitch time (t_{OLD}). At that point the device takes the following actions.

- OLD bit in the IC status (IC_STAT) register sets to 1
- HBX_HS_OLD or HBX_LS_OLD bit in the open-load status register (OLD_STAT_X) sets to 1 (depending if the fault is on the high-side MOSFET or low-side MOSFET, respectively).
- FALTN pin is driven low to indicate a fault to the controller.

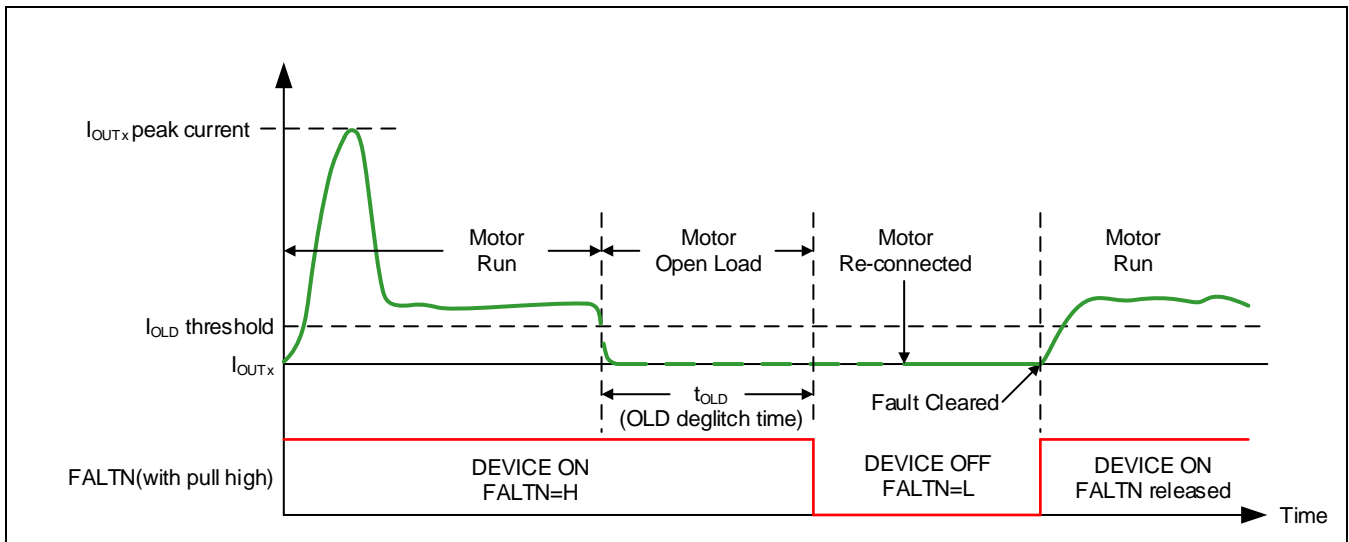


Figure 31. Active open-load detection

Normal operation resumes (driver operation resumes, the FALTN pin goes high, OLD bit is reset to 0) when the open-load condition is removed (the user reconnects the load to the OUTX connection) and the controller writes the CLR_FLT bit to 1.

NOTE

After the open-load fault condition is removed, the FALTN pin will be driven high and the fault status are removed when,

- CLR_FLT command is issued after deglitch time (t_{OLD}) while OUTX is set high.
- CLR_FLT command is issued after OUTX is set to Hi-Z.
- CLR_FLT command is issued after HBX_OLD_DIS bit is set.

By default, OLD on the PT12493 devices is enabled. The OLD control registers (OLD_CTRL_1 and OLD_CTRL_2) allow the user to disable OLD on the OUTX pins with the HBX_OLD_DIS bits. The OLD_OP bit in the OLD_CTRL_2 register determines the response of the device to an active OLD fault. If OLD_OP = 0, the OUTX pins go to the Hi-Z state to stop driving the outputs. If OLD_OP = 1, the OUTX pins stay in their previous state and do not react to the OLD fault unless the user takes action. Similarly, the OLD_REP bit determines if the OLD fault will report on the FALTN pin or only in the IC_STAT register. Table 7 summarizes the open-load detection feature and conditions.

NOTE

By default, the OLD feature is enabled, the outputs disable (go Hi-Z) when the OLD flags, and the FALTN pin will report the OLD.

LOAD / OPEN	REGISTER SETTINGS	OLD_OP	OLD_REP	OUT1	OUT2	FALTN	BITS EFFECTED	RECOVERY
Half- Bridge Load Connected	HB1_HS_EN = 1	X	X	H	X	HIGH	N/A	N/A
	HB1_LS_EN = 1	X	X	L	X	HIGH		
Full-Bridge Load Connected	HB1_HS_EN = 1 HB2_LS_EN = 1	X	X	H	L	HIGH		
	HB1_LS_EN = 1 HB2_HS_EN = 1	X	X	L	H	HIGH		
Half- Bridge Open	HB1_HS_EN = 1	0	0	Hi-Z	X	LOW	OLD = 1 (IC_STAT) HB1_HS_OLD = 1	OLD Condition Removed CLR_FLT = 1
		0	1	Hi-Z	X	HIGH		
		1	0	H	X	LOW		
		1	1	H	X	HIGH		
	HB1_LS_EN = 1	0	0	Hi-Z	X	LOW	OLD = 1 (IC_STAT) HB1_LS_OLD = 1	
		0	1	Hi-Z	X	HIGH		
		1	0	L	X	LOW		
		1	1	L	X	HIGH		
Full-Bridge Open	HB1_HS_EN = 1 HB2_LS_EN = 1	0	0	Hi-Z	Hi-Z	LOW	OLD = 1 (IC_STAT) HB1_HS_OLD = 1 or HB2_LS_OLD = 1 ⁽¹⁾	
		0	1	Hi-Z	Hi-Z	HIGH		
		1	0	H	L	LOW		
		1	1	H	L	HIGH		
	HB1_LS_EN = 1 HB2_HS_EN = 1	0	0	Hi-Z	Hi-Z	LOW	OLD = 1 (IC_STAT) HB1_LS_OLD = 1 or HB2_HS_OLD = 1 ⁽²⁾	
		0	1	Hi-Z	Hi-Z	HIGH		
		1	0	L	H	LOW		
		1	1	L	H	HIGH		
<p>(1) Either of the HB1_HS_OLD or HB2_LS_OLD will set depending upon which half-bridge OLD triggers first.</p> <p>(2) Either of the HB1_LS_OLD or HB2_HS_OLD will set depending upon which half-bridge OLD triggers first.</p>								

Table 7. OLD Configuration

Negative-current OLD

The PT12493 device also includes a negative-current OLD mode. The negative current can flow either through the body diode of high-side FET or the FET itself depending on whether or not the channel is configured for synchronous rectification. Figure 32 shows the current re-circulation through the body diode of the high-side FET when the synchronous rectification mode is OFF (i.e. HB2_FW = 0). In this case, the active OLD will not falsely report an open-load condition since the OLD circuit only enables when the FET is ON. Negative-current OLD will also work during re-circulation through the low-side FETs.

Figure 33 shows the negative current re-circulation through the high-side FET when synchronous rectification is ON (i.e. HB2_FW = 1). In this scenario, for default operation (OLD_NEG_EN = 0), the device can show a false open-load fault since the FET current is lower than the positive OLD threshold. However, when negative-current OLD mode is enabled, the device will only flag an open-load fault if $I_{OUTX} < I_{OLD_NEG}$. This mode is enabled by setting the OLD_NEG_EN bit in OLD_CTRL3 register.

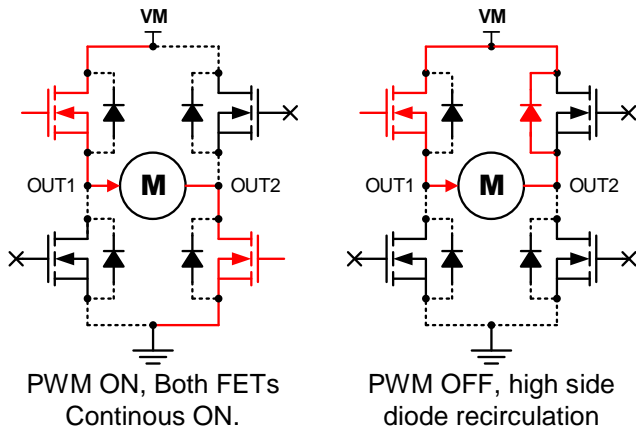


Figure 32. Negative Current Flow in OUT2 by Body Diode of High-Side FET

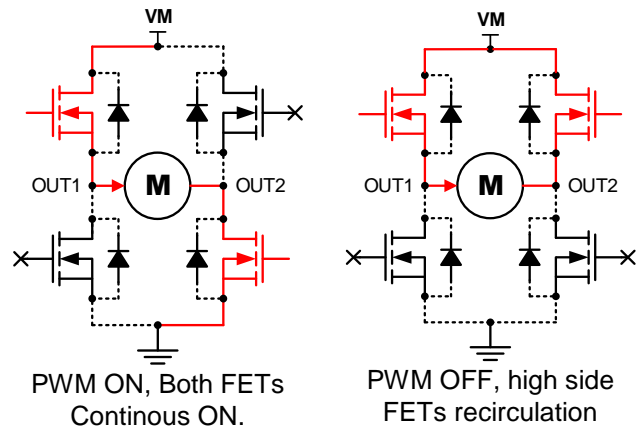


Figure 33. Negative Current Flow in High-Side FET of OUT2 Channel

Figure 34 shows the waveforms of false open-load detection when the negative-current OLD setting is disabled (OLD_NEG_EN = 0). As shown in this figure, the high-side FET of the OUT1 channel is always switched ON and the low-side and high-side FET of the OUT2 channel are operating in complimentary way (i.e. synchronous rectification mode is enabled). In synchronous rectification, the current flows in negative direction from OUT2 to VM (i.e. FET Source to Drain) during the high-side FET conduction. Initially, for the first PWM cycle, the OLD mode is disabled to show the currents in different FETs during the motor operation. When OLD is enabled in second PWM cycle, then the device registers a false open-load detect during the high-side FET conduction as shown in Figure 34. The FALTN pin is pulled low and both high-side and low-side FET of OUT2 channels are disabled. The body diode of the high side FET (OUT2) conducts to complete the motor current path.

This false detection of open load is eliminated by enabling the negative-current OLD setting (OLD_NEG_EN = 1). As shown in Figure 35, the negative OLD current setting (I_{OLD_NEG}) is enabled for the high-side FET of OUT2 channel. This setting allows the negative current path (from source to drain) in high-side FET. The FALTN pin is latched high and OUT2 channel is not disabled when OLD is enabled in second PWM cycle.

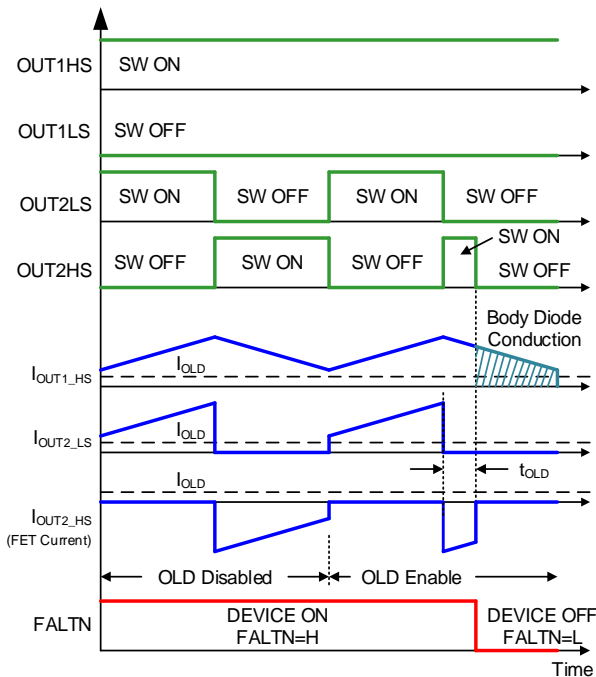


Figure 34. Waveforms Showing False OLD with Negative-Current OLD Disabled

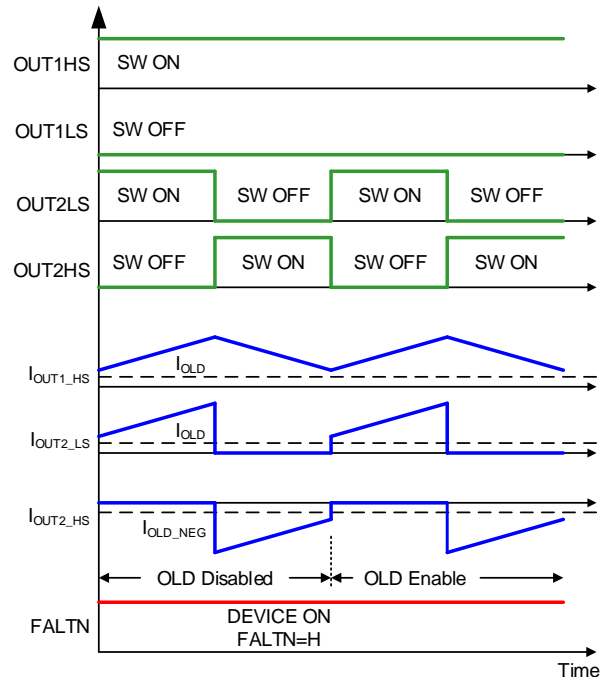


Figure 35. Waveforms Showing Operation with Negative-Current OLD Enabled

Low-current OLD

Low-current open-load detection is another type of active open-load detection in the PT12493 devices. In low-current open-load detection, the current detection threshold is around 10x lower than the active open-load detection scheme. This feature gives the user flexibility to detect a valid open-load condition when driving loads that require low current.

As shown in Figure 36, if the low-side MOSFET is in operating condition (switch-ON) and the current flowing in the particular MOSFET is lower than the low-current active open-load current threshold (I_{OLD_LOW}) for at least open-load detection deglitch time (t_{OLD}), then an open-load condition is detected. The OLD bit in the IC status (IC_STAT) register is set, the HBX_LS_OLD bit in the open-load status register (OLD_STAT_X) is set and FALTN pin is driven low during an open-load detect. Normal operation resumes (driver operation and the FALTN pin is released) when the open-load condition is removed and CLR_FLT command is issued. The OLD bit remains set until cleared through the CLR_FLT bit.

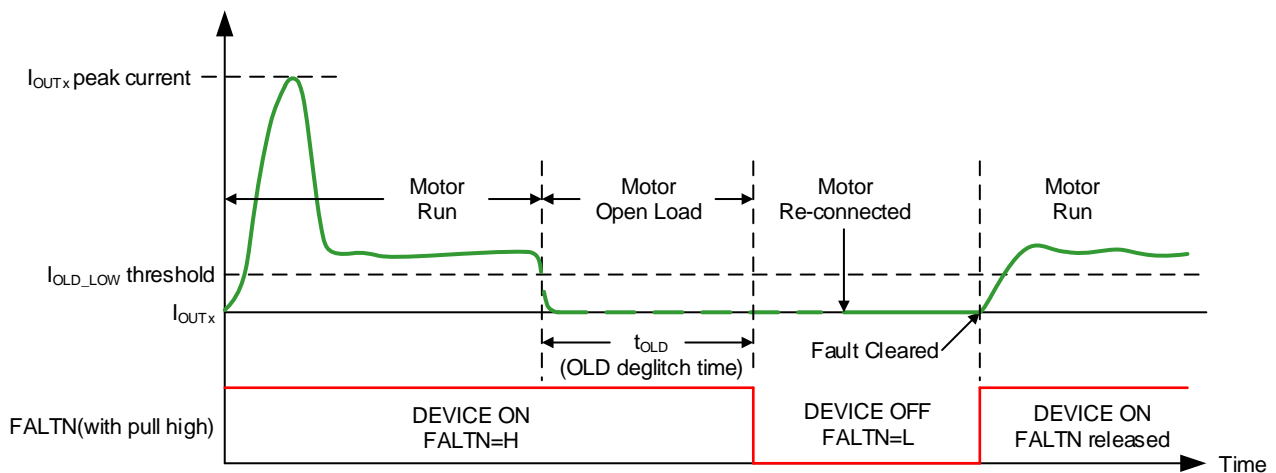


Figure 36. Low-Current OLD

NOTE

The low-current OLD has following limitations

- This feature is only applicable for the current flowing in low-side FET.
- Once this mode is enabled the corresponding over-current threshold for the low-side FET is also reduced by 11 times (~120 mA min.).
- The $R_{DS(on)}$ of the low side FET will increase by 11 times (~7.5 Ω typical), hence the thermal performance has to be monitored. However, for the lower current the thermal dissipation is limited.

Figure 37 shows the flowchart for implementing the low-current active OLD in continuous mode of operation. Following are the steps to configure and detect the low-current active OLD in the PT12493 device.

1. Enable OLD by setting the OLD_OP bit in OLD_CTRL_2 register. This setting will ensure that the OUTX outputs continue to operate when and OLD fault occurs.
2. Enable the full-bridge operation by setting the individual HBX_HS_EN/HBX_LS_EN bits in operation control (OP_CTRL_1, OP_CTRL_2 and OP_CTRL_3) registers.
3. Check for the FALTN pin status and the OLD fault in the IC_STAT register.
4. If the FALTN pin is low and the OLD fault is high, then check for the individual HBX_HS_OLD/HBX_LS_OLD bits in OLD status (OLD_STAT_1, OLD_STAT_2 and OLD_STAT_3) registers.
5. Disable OLD using the HBX_OLD_DIS bits for the OUTX pins acting as high-side drivers.
6. Enable the low-current OLD mode for the half-bridge which low-side is operating by using the HBX_LOLD_EN bit in OLD control (OLD_CTRL_3 and OLD_CTRL_4) registers. This will also disable the high-side OLD for the particular half-bridge.
7. Wait for the open-load deglitch time (t_{OLD}).

8. Issue the clear fault command (CLR_FLT) to release the FALTN pin and clear the OLD bits if low-current OLD is not detected.
9. If the OLD bit is high and the FALTN pin is not released (low), then low-current OLD fault is detected.

NOTE

The low-current OLD is applicable only for low-side FETs. The user has to enable the low-current OLD mode for the corresponding low-side FET.

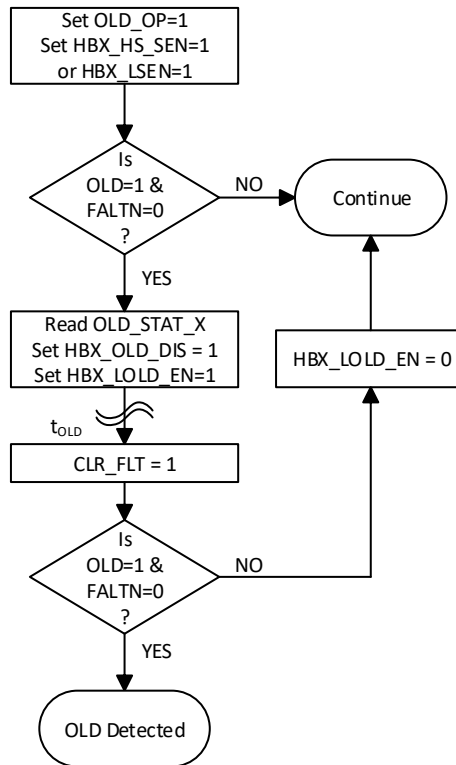


Figure 37. Flowchart for Enabling Low-Current OLD (Continuous Mode)

Passive OLD

In passive OLD, the detection of open load is carried before the driver is turned on. The state of all FETs remains in Hi-Z state, while a minimal amount of current flows through motor for short amount of time to test the motor connection. The diagnostic current is very small to avoid causing the motor rotation.

Figure 38, Figure 39, and Figure 40 show the circuit implementations of passive OLD. As shown in these figures, a constant current source pulls the OUT1 pin to the AVDD (internal fixed voltage) which allows current flow from OUT1 to OUT2 terminal. The current drawn is completely dependent on the motor resistance between OUT1 and OUT2 and limited by the internal current sourcing (I_{OL_PU}) and sinking (I_{OL_PD}) capability of the passive OLD circuitry. Depending on this current and the comparator threshold voltage (V_{OL_HS} and V_{OL_LS}), the comparator output OL1_HS and OL2_LS are either set or reset which determines the open-load status. When an open load is detected, the OLD bit in the IC status (IC_STAT) register is set, the HBX_LS_OLD bit in the open-load status register (OLD_STAT_X) is set and FALTN pin is driven low. The OLD bit remains set until cleared through the CLR_FLT bit. This implementation is applicable for half-bridge driving as shown in Figure 39, and Figure 40.

NOTE

Passive OLD sequence is not disabled by the HBX_OLD_DIS bits.

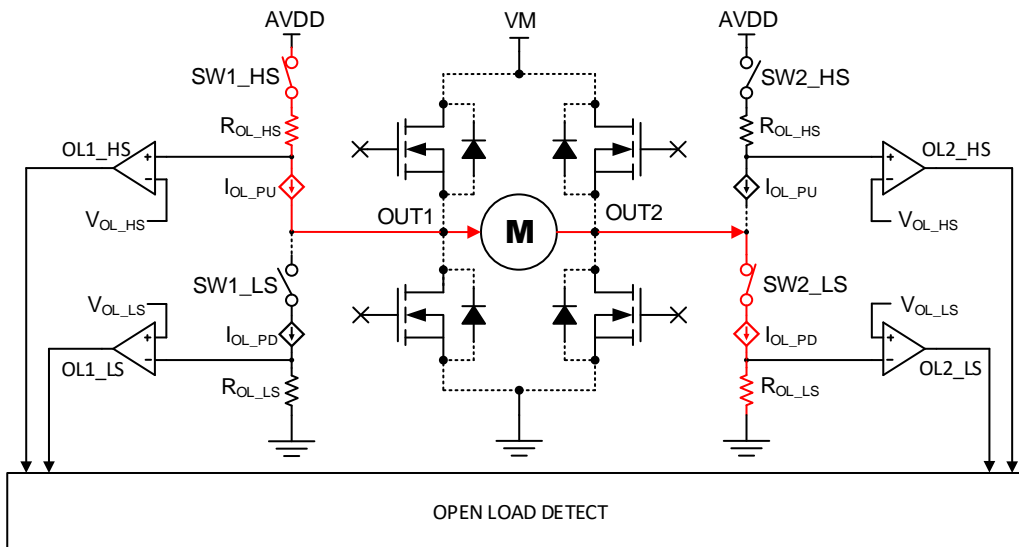


Figure 38. Passive OLD Circuit for a Load Driven in Full-Bridge Operation

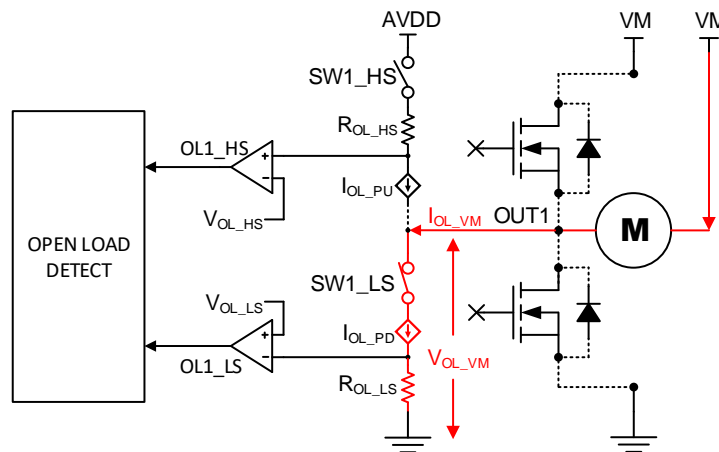


Figure 39. Passive OLD Circuit for Half-Bridge Operation with Load Connected to VM

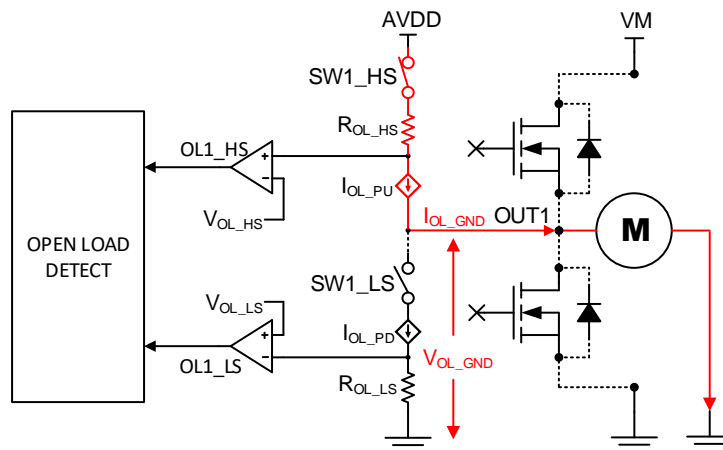


Figure 40. Passive OLD Circuit for Half-Bridge Operation with Load Connected to GND

Following are the steps to configure and detect the passive OLD in the PT12493 device.

1. Enable the passive OLD mode for the individual half-bridges which is to be diagnosed using the Half-bridge passive OLD enable bits (HBX_POLD_EN) in OLD_CTRL_5 register.
2. Configure the half-bridge operation control bits (HBX_HS_EN/HBX_LS_EN) in operation control register (OP_CTRL_X) to determine the high-side and low-side OLD check. Note that these bits are now used for the passive OLD configuration. If anytime, the HBX_POLD_EN is reset then the bridge starts operating.
3. Enable the passive OLD using the Passive OLD Enable bit (POLD_EN) in CONFIG_CTRL register. Setting the POLD_EN bit enables the passive OLD detection circuit on all OUTx pin for which the corresponding HBX_HS_EN or HBX_LS_EN are set to 1.
4. Wait for the passive OLD time as determined by the user.
5. After the completion of passive OLD time, disable the passive OLD enable bit (POLD_EN).
6. Monitor the FALTN pin / OLD bit in Status register (IC_STAT) and the HBX_HS_OLD/HBX_LS_OLD bit in the OLD status registers (OLD_STAT_X) for any open-load detection.
7. Restart the sequence for other half-bridges / full-bridges.

During normal driving, HBX_HS_EN and HBX_LS_EN bits control the state of OUTX. However, when POLD_EN and HBX_POLD_EN are 1, the OUTX channel is disabled, and HBX_HS_EN and HBX_LS_EN control SWX_HS and SWX_LS used for passive OLD (see schematic representation in Figure 38). Table 8 shows the truth table for this operation.

HBX_POLD_EN	HBX_HS_EN	HBX_LS_EN	OUTX	SWX_HS	SWX_LS	OPEN LOAD SEQUENCE
0	X	X	Follows HBX_HS_EN and HBX_LS_EN	Open	Open	Passive OLD for the channel is disabled and HBX_HS_EN/ HBX_LS_EN set output OUTx state
1	0	0	Z	Open	Open	Off state - no passive OLD
1	0	1	Z	Open	Closed	Valid passive OLD for VM-connected load
1	1	0	Z	Closed	Open	Valid passive OLD for GND-connected load
1	1	1	Z	Open	Open	Invalid state

Table 8. Truth Table for Passive OLD

NOTE

The OLD_REP bit works in a similar way as for the active OLD. The OLD_OP bit is not applicable for passive OLD operation since the outputs are already disabled.

NOTE

Passive OLD sequence is not enabled if any other fault (other than OCP/OLD) is present.

Table 9 shows an example for configuring passive OLD for various loads. The HBX_VM_POLD bits can be enabled for any loads that connect directly to VM. In cases where VM is low, the passive OLD current may need to be larger so passive OLD does not falsely indicate an open load. Setting HBX_VM_POLD = 1 chooses a smaller R_{OL} so more current flows and the device can properly detect an open load.

CONNECTION	HB1_VM_POLD	HB2_VM_POLD	HB1_HS_EN	HB1_LS_EN	HB2_HS_EN	HB2_LS_EN	OPEN-LOAD DETECTION
Full-Bridge Operation (Motor Connected Between OUT1 and OUT2)	0	0	1	0	0	1	Detection based on resistance threshold (Forward Connection)
	0	0	0	1	1	0	Detection based on resistance threshold (Reverse Connection)
	0	0	1	0	1	0	Invalid case (both high-side OLD circuitry operating)
	0	0	0	1	0	1	Invalid case (both low-side OLD circuitry operating)
Half-Bridge Operation (Load Connected Between OUT1/2 and VM)	1	X	0	1	0	0	Detection only for OUT1 channel based on resistance threshold
	X	1	0	0	0	1	Detection only for OUT2 channel based on resistance threshold
	1	1	0	1	0	1	Detection for both outputs based on resistance threshold
	X	X	1	0	0	0	Invalid case (OUT1 high-side OLD circuitry is operating for VM connected load)
	X	X	0	0	1	0	Invalid case (OUT2 high-side OLD circuitry is operating for VM connected load)
	X	X	1	0	1	0	Invalid case (both high-side OLD circuitry is operating for VM connected load)
Half-Bridge Operation (Load Connected Between OUT1/2 and GND)	0	0	1	0	0	0	Detection only for OUT1 channel based on resistance threshold
	0	0	0	0	1	0	Detection only for OUT2 channel based on resistance threshold
	0	0	1	0	1	0	Detection for both outputs based on resistance threshold
	0	0	0	1	0	0	Invalid case (OUT1 low-side OLD circuitry is operating for GND connected load)
	0	0	0	0	0	1	Invalid case (OUT2 low-side OLD circuitry is operating for GND connected load)
	0	0	0	1	0	1	Invalid case (both low-side OLD circuitry is operating for GND connected load)

Table 9. Passive OLD Configurations

THERMAL WARNING (OTW)

If the die temperature exceeds the trip point of the thermal warning (T_{OTW}), the OTW bit is set in the IC status (IC_STAT) register. The reporting of OTW on the FALTN pin can be enabled by setting the over-temperature warning reporting (OTW_REP) bit in the configuration control (CONFIG_CTRL) register. The device performs no additional action and continues to function. In this case, the FALTN pin releases when the die temperature decreases below the hysteresis point of the thermal warning (T_{OTW_HYS}). The OTW bit remains set until cleared through the CLR_FLT bit and the die temperature is lower than thermal warning trip (T_{OTW}).

NOTE

Over Temperature warning is not reported on FALTN pin by default.

THERMAL SHUTDOWN (OTSD)

If the die temperature exceeds the trip point of the thermal shutdown limit (T_{OTSD}), all half-bridge drivers are disabled, the charge pump is shut down, and the FALTN pin is driven low. In addition, the OTSD bit is latched high in IC status (IC_STAT) register. Normal operation resumes (driver operation and the FALTN pin is released) when the overtemperature shutdown condition is removed and die temperature decreases below the hysteresis point of the thermal warning (T_{OTSD_HYS}). The OTSD bit remains latched high indicating that a thermal event occurred until a clear fault command is issued through the CLR_FLT bit. This protection feature cannot be disabled.

DEVICE FUNCTIONAL MODES

SLEEP MODE (SLEPN = 0)

The SLEPN pin manages the state of the PT12493 device. When the SLEPN pin is low, the device enters a low-power sleep mode. In sleep mode, all half-bridge drivers are disabled, the internal charge pump is disabled, the internal regulators are disabled, and the SPI bus is disabled. The t_{SLEEP} time must elapse after a falling edge on the SLEPN pin before the device enters sleep mode. The device comes out of sleep mode automatically if the SLEPN pin is pulled high. The t_{WAKE} time must elapse before the device is ready for inputs.

OPERATING MODE (SLEPN = 1)

When the SLEPN pin is high and $V_{VM} > V_{UVLO}$, the device enters operating mode. The t_{WAKE} time must elapse before the device is ready for inputs. In this mode the half bridge drivers, charge pump, internal regulators, and SPI bus are active. Table 10 summarizes the different operating modes of PT12493 device.

MODE	CONDITION	HALF-BRIDGES	INTERNAL CIRCUITS
Operating	4.5-V < V_{VM} < 20-V (EXT_OVP = 0b) 4.5-V < V_{VM} < 32-V (EXT_OVP = 1b) SLEPN Pin = High	Operating	Operating
Sleep	4.5-V < V_{VM} < 32-V SLEPN Pin = Low	Disabled	Disabled
Fault	Any Fault Condition Met	Depends on Fault	Depends on Fault

Table 10. Functional Modes

FAULT MODE

The PT12493 is protected against various faults as summarized in Table 11

FAULT	CONDITION	CONFIGURATION	REPORT	HALF-BRIDGE	LOGIC	RECOVERY
VM Undervoltage (UVLO)	$V_{VM} < V_{UVLO}$ (Max. 4.5-V)	—	FALTN Pin IC_STAT Register	Hi-Z	Active	Automatic: $V_{VM} > V_{UVLO}$
VDD Undervoltage (UVLO)	$V_{VDD} < V_{POR}$ (Max 3-V)	—	IC_STAT Register	Hi-Z	Reset	Automatic: $V_{DD} > V_{POR}$
VM Overvoltage (OVP)	$V_{VM} > V_{OVP}$ (Min. 20-V)	EXT_OVP = 0	FALTN Pin IC_STAT Register	Hi-Z	Active	Automatic: $V_{VM} < V_{OVP}$
	$V_{VM} > V_{OVP}$ (Min. 32-V)	EXT_OVP = 1				
Over Current Protection (OCP)	$I_{OUT} > I_{OCP}$ (Min. 1.3-A)	OCP_REP = 0	FALTN Pin IC_STAT Register	Hi-Z	Active	CLR_FLT = 1 & $I_{OUT} < I_{OCP}$
		OCP_REP = 1	IC_STAT Register	Hi-Z	Active	
Open-Load Detect (OLD)	$I_{OUT} < I_{OLD}$ (Max. 15-mA)	OLD_OP = 0 OLD_REP = 0	FALTN Pin IC_STAT Register	Hi-Z	Active	CLR_FLT = 1 & $I_{LOAD} > I_{OLD}$
		OLD_OP = 0 OLD_REP = 1	IC_STAT Register	Hi-Z	Active	
		OLD_OP = 1 OLD_REP = 0	FALTN Pin IC_STAT Register	Operating	Active	
		OLD_OP = 1 OLD_REP = 1	IC_STAT Register	Operating	Active	
	$R_{LOAD} > R_{OLD}$ (Max. 100-kΩ)	OLD_REP = 0	FALTN Pin IC_STAT Register	N/A	Active	CLR_FLT = 1 & OLD Sequenced & $R_{LOAD} < R_{OLD}$
		OLD_REP = 1	IC_STAT Register	N/A	Active	
Over-Temperature Warning (OTW)	$T_J > T_{OTW}$ (Min. 120°C)	OTW_REP = 0	IC_STAT Register	Operating	Active	No Action
		OTW_REP = 1	FALTN Pin IC_STAT Register	Operating	Active	Automatic: $T_J < T_{OTW} - T_{OTW_HYS}$
Over-Temperature Shutdown (OTSD)	$T_J > T_{OTSD}$ (Min. 150°C)	—	FALTN Pin IC_STAT Register	Hi-Z	Active	Automatic: $T_J < T_{OTSD} - T_{OTSD_HYS}$

Table 11. Fault Action and Response

PROGRAMMING

SPI

SPI bus is used to set device configurations, operating parameters, and read out diagnostic information on the PT12493 device. The SPI operates in slave mode and connects to a master controller. The SPI input data (SDI) word consists of a 16 bit word, with an 8-bit command and 8 bits of data. The SPI output data (SDO) word consists of 8-bit register data and the first 8 bits make up the Status Register with Fault Status indication. The data sequence between the MCU and the SPI slave driver is shown in Figure 41.

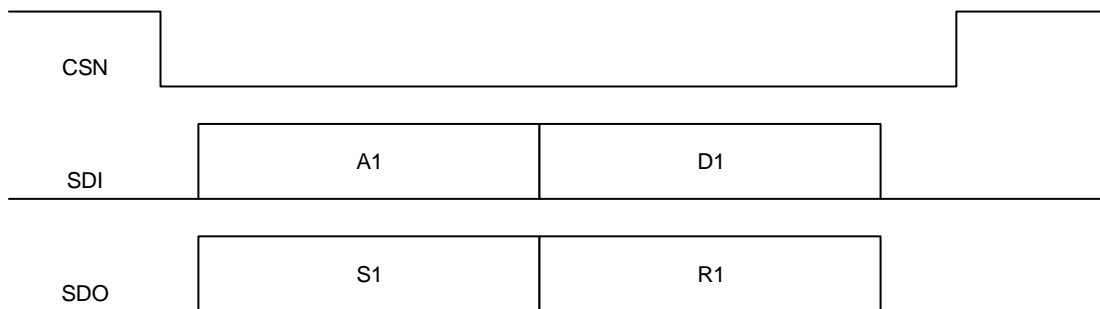


Figure 41. SPI Data Frame

A valid frame must meet the following conditions:

- The SCLK pin should be low when the CSN pin transitions from high to low and from low to high.
- The CSN pin should be pulled high for at least 400 ns between words.
- When the CSN pin is pulled high, any signals at the SCLK and SDI pins are ignored and the SDO pin is placed in the Hi-Z state.
- Data is captured on the falling edge of SCLK and data is propagated on the rising edge of SCLK.
- The most significant bit (MSB) is shifted in and out first.
- A full 16 SCLK cycles must occur for transaction to be valid.
- If the data word sent to the SDI pin is less than or more than 16 bits, a frame error occurs and the data word is ignored.
- For a write command, the existing data in the register being written to is shifted out on the SDO pin following the 8-bit command data.

SPI FORMAT

The SDI input data word is 16 bits long and consists of the following format:

- 1 read or write bit, W (bit B14)
- 6 address bits, A (bits B13 through B8)
- 8 data bits, D (bits B7 through B0)

The SDO output data word is 16 bits long and the first 8 bits makes up the IC status register. The report word is the content of the register being accessed.

For a write command ($W0 = 0$), the response word on the SDO pin is the data currently in the register being written to.

For a read command ($W0 = 1$), the response word is the data currently in the register being read.

		R/W	Address						Data							
Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Data	0	W0	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

Table 12. SDI Input Data Word Format

	IC Status								Report							
Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Data	1	1	OT	OLD	OCF	UVLO	OVP	NPOR	D7	D6	D5	D4	D3	D2	D1	D0

Table 13. SDO Output Data Word Format

SPI INTERFACE FOR MULTIPLE SLAVES

Multiple PT12493 devices can be connected to the master controller with and without the daisy chain. For connecting a 'n' number of PT12493 to a master controller without using a daisy chain, 'n' number of I/O resources from master controller has to be utilized for CSN pins as shown Figure 42. Whereas, if the daisy chain configuration is used, then a single CSN line can be used for connecting multiple PT12493 devices as shown in Figure 43.

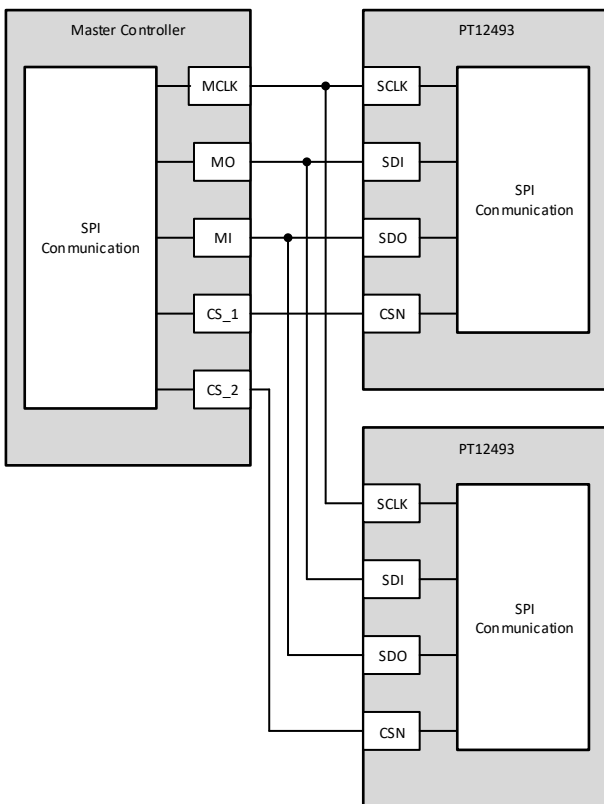


Figure 42. SPI Operation Without Daisy Chain

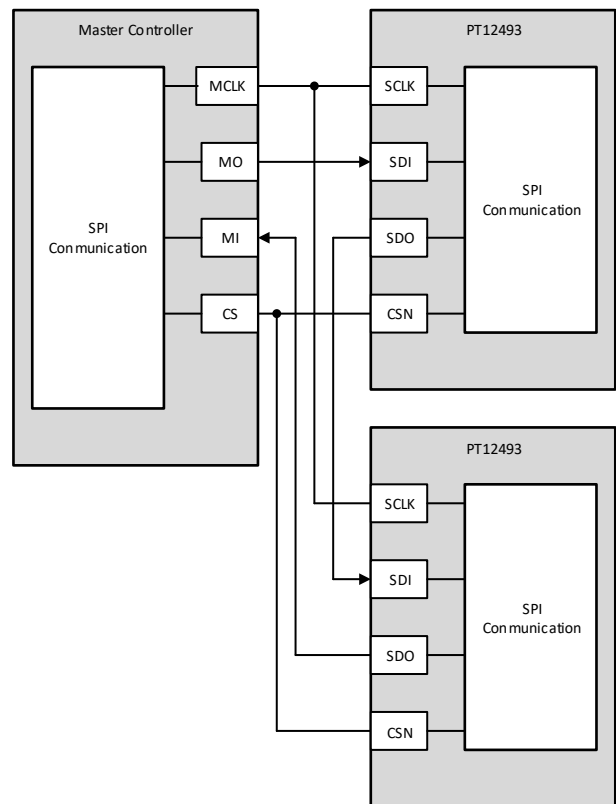


Figure 43. SPI Operation With Daisy Chain

SPI INTERFACE FOR MULTIPLE SLAVES IN DAISY CHAIN

The PT12493 device can be connected in a daisy chain configuration to save GPIO ports when multiple devices are communicating to the same MCU. Figure 44 shows the topology when 3 devices are connected in series with waveforms.

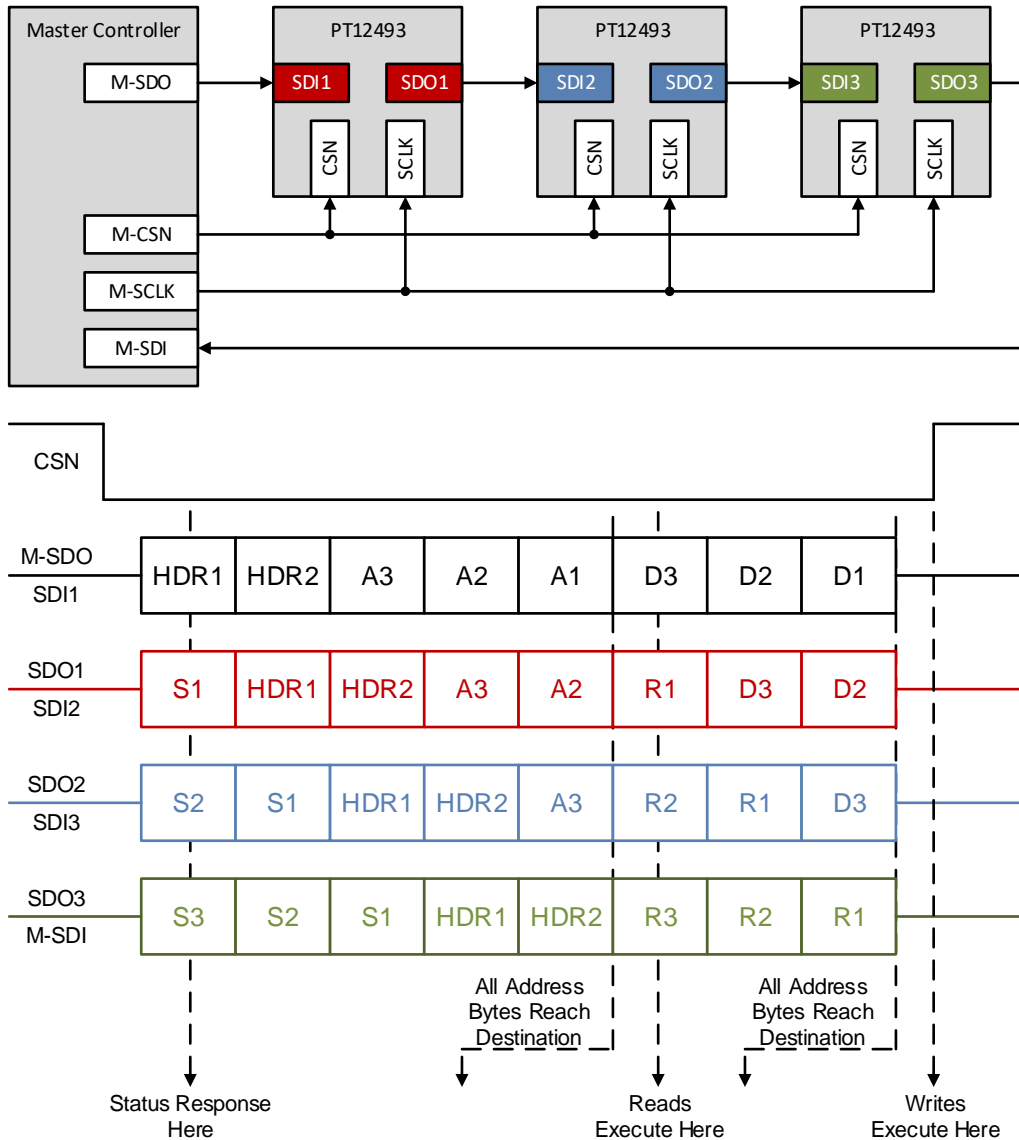


Figure 44. Daisy Chain SPI Operation

The first device in the chain shown above receives data from the master controller in the following format. See SDI1 in Figure 44

- 2 bytes of Header
- 3 bytes of Address
- 3 bytes of Data

After the data has been transmitted through the chain, the master controller receives it in the following format. See SDO3 in Figure 44

- 3 bytes of Status
- 2 bytes of Header (should be identical to the information controller sent)
- 3 bytes of Report

The Header bytes contain information of the number of devices connected in the chain, and a global clear fault command that will clear the fault registers of all the devices on the rising edge of the chip select (CSN) signal. N5 through N0 are 6 bits dedicated to show the number of devices in the chain as shown in Figure 45. Up to 63 devices can be connected in series per daisy chain connection.

The 5 LSBs of the HDR2 register are don't care bits that can be used by the MCU to determine integrity of the daisy chain connection. Header bytes must start with 1 and 0 for the two MSBs.

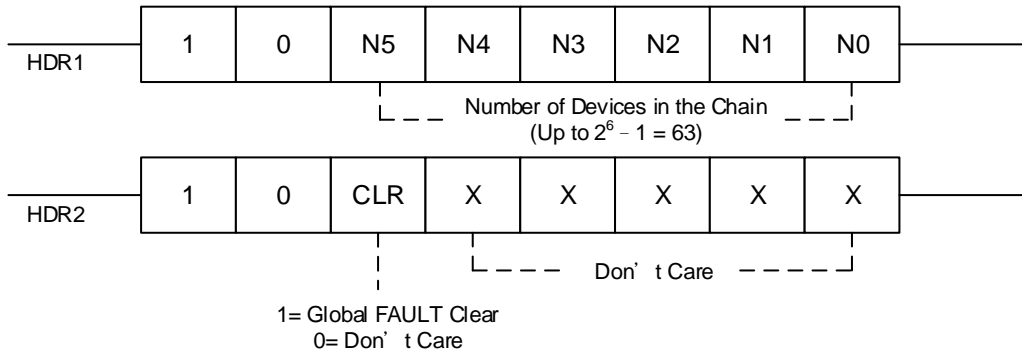


Figure 45. Header Bits

The Status byte provides information about the fault status register for each device in the daisy chain as shown in Figure 46. That way the master controller does not have to initiate a read command to read the fault status from any particular device. This saves the controller additional read commands and makes the system more efficient to determine fault conditions flagged in a device.

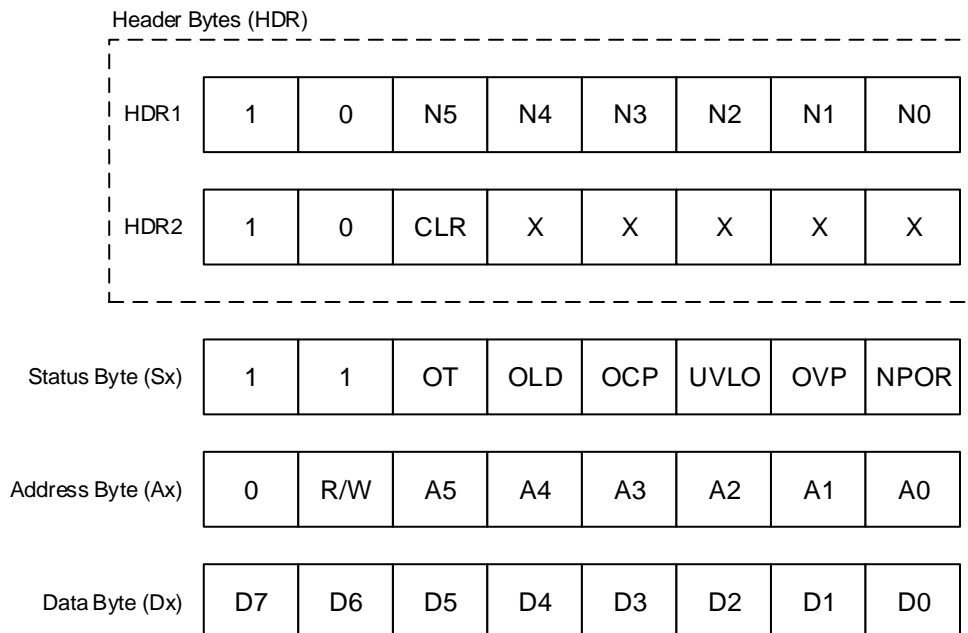


Figure 46. Daisy Chain Read Registers

When data passes through a device, it determines the position of itself in the chain by counting the number of Status bytes it receives following by the first Header byte. For example, in this 3 devices configuration, device 2 in the chain will receive two Status bytes before receiving HDR1 byte, followed by HDR2 byte.

From the two Status bytes it knows that its position is second in the chain, and from HDR2 byte it knows how many devices are connected in the chain. That way it only loads the relevant address and data byte in its buffer and bypasses the other bits. This protocol allows for faster communication without adding latency to the system for up to 63 devices in the chain.

The address and data bytes remain the same with respect to a single device connection. The Report bytes (R1 through R3), as shown in the figure above, is the content of the register being accessed.

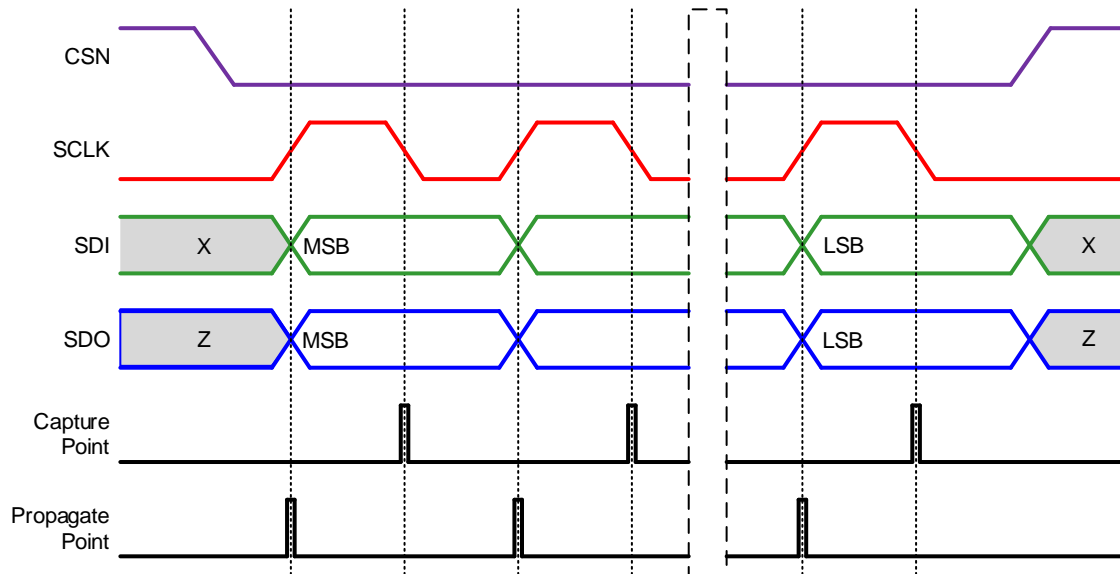


Figure 47. SPI Slave Timing Diagram

REGISTER MAP

This section contains the register maps and bit descriptions contains the register maps and register descriptions for PT12493, in Table 14

DEVICE	NUMBER OF HALF-BRIDGES	NUMBER OF PWM GENERATORS	OPEN-LOAD DETECTION SCHEMES	REGISTER MAP
PT12493	8	8	Passive OLD, Active OLD, Low-Current Active OLD, Negative-Current Active OLD	Table 16

Table 14. Summary of PT12493 Register Map

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

Table 15. Control Registers Access Type Codes

Name	7	6	5	4	3	2	1	0	Type	Address
IC_STAT	Reserved	OTSD	OTW	OLD	OCP	UVLO	OVP	NPOR	R	00h
OCP_STAT_1	HB4_HS_OCP	HB4_LS_OCP	HB3_HS_OCP	HB3_LS_OCP	HB2_HS_OCP	HB2_LS_OCP	HB1_HS_OCP	HB1_LS_OCP	R	01h
OCP_STAT_2	HB8_HS_OCP	HB8_LS_OCP	HB7_HS_OCP	HB7_LS_OCP	HB6_HS_OCP	HB6_LS_OCP	HB5_HS_OCP	HB5_LS_OCP	R	02h
OCP_STAT_3	Reserved								R	03h
OLD_STAT_1	HB4_HS_OLD	HB4_LS_OLD	HB3_HS_OLD	HB3_LS_OLD	HB2_HS_OLD	HB2_LS_OLD	HB1_HS_OLD	HB1_LS_OLD	R	04h
OLD_STAT_2	HB8_HS_OLD	HB8_LS_OLD	HB7_HS_OLD	HB7_LS_OLD	HB6_HS_OLD	HB6_LS_OLD	HB5_HS_OLD	HB5_LS_OLD	R	05h
OLD_STAT_3	Reserved								R	06h
CONFIG_CTRL	POLD_EN	IC_ID			OCP_REP	OTW_REP	EXT_OVP	CLR_FLT	RW	07h
OP_CTRL_1	HB4_HS_EN	HB4_LS_EN	HB3_HS_EN	HB3_LS_EN	HB2_HS_EN	HB2_LS_EN	HB1_HS_EN	HB1_LS_EN	RW	08h
OP_CTRL_2	HB8_HS_EN	HB8_LS_EN	HB7_HS_EN	HB7_LS_EN	HB6_HS_EN	HB6_LS_EN	HB5_HS_EN	HB5_LS_EN	RW	09h
OP_CTRL_3	Reserved								RW	0Ah
PWM_CTRL_1	HB8_PWM	HB7_PWM	HB6_PWM	HB5_PWM	HB4_PWM	HB3_PWM	HB2_PWM	HB1_PWM	RW	0Bh
PWM_CTRL_2	PWM_CH8_DIS	PWM_CH7_DIS	PWM_CH6_DIS	PWM_CH5_DIS	PWM_CH4_DIS	PWM_CH3_DIS	PWM_CH2_DIS	PWM_CH1_DIS	RW	0Ch
FW_CTRL_1	HB8_FW	HB7_FW	HB6_FW	HB5_FW	HB4_FW	HB3_FW	HB2_FW	HB1_FW	RW	0Dh
FW_CTRL_2	Reserved								RW	0Eh
PWM_MAP_CTRL_1	Reserved		HB2_PWM_MAP			HB1_PWM_MAP			RW	0Fh
PWM_MAP_CTRL_2 ⁽¹⁾	Reserved		HB4_PWM_MAP			HB3_PWM_MAP			RW	10h
PWM_MAP_CTRL_3	Reserved		HB6_PWM_MAP			HB5_PWM_MAP			RW	11h
PWM_MAP_CTRL_4	Reserved		HB8_PWM_MAP			HB7_PWM_MAP			RW	12h
PWM_FREQ_CTRL_1	PWM_CH4_FREQ		PWM_CH3_FREQ		PWM_CH2_FREQ		PWM_CH1_FREQ		RW	13h
PWM_FREQ_CTRL_2	PWM_CH8_FREQ		PWM_CH7_FREQ		PWM_CH6_FREQ		PWM_CH5_FREQ		RW	14h
PWM_DUTY_CTRL_1	PWM_DUTY_CH1								RW	15h
PWM_DUTY_CTRL_2	PWM_DUTY_CH2								RW	16h
PWM_DUTY_CTRL_3	PWM_DUTY_CH3								RW	17h
PWM_DUTY_CTRL_4	PWM_DUTY_CH4								RW	18h
PWM_DUTY_CTRL_5	PWM_DUTY_CH5								RW	19h
PWM_DUTY_CTRL_6	PWM_DUTY_CH6								RW	1Ah
PWM_DUTY_CTRL_7	PWM_DUTY_CH7								RW	1Bh
PWM_DUTY_CTRL_8	PWM_DUTY_CH8								RW	1Ch
SR_CTRL_1	HB8_SR	HB7_SR	HB6_SR	HB5_SR	HB4_SR	HB3_SR	HB2_SR	HB1_SR	RW	1Dh
SR_CTRL_2	Reserved								RW	1Eh

Name	7	6	5	4	3	2	1	0	Type	Address	
OLD_CTRL_1	HB8_OLD_DIS	HB7_OLD_DIS	HB6_OLD_DIS	HB5_OLD_DIS	HB4_OLD_DIS	HB3_OLD_DIS	HB2_OLD_DIS	HB1_OLD_DIS	RW	1Fh	
OLD_CTRL_2	OLD_REP	OLD_OP	PL_MODE_EN		Reserved					RW	20h
OLD_CTRL_3	OCP_DEG			OLD_NEG_EN	Reserved					RW	21h
OLD_CTRL_4	HB8_LOLD_EN	HB7_LOLD_EN	HB6_LOLD_EN	HB5_LOLD_EN	HB4_LOLD_EN	HB3_LOLD_EN	HB2_LOLD_EN	HB1_LOLD_EN	RW	22h	
OLD_CTRL_5	HB8_POLD_EN	HB7_POLD_EN	HB6_POLD_EN	HB5_POLD_EN	HB4_POLD_EN	HB3_POLD_EN	HB2_POLD_EN	HB1_POLD_EN	RW	23h	
OLD_CTRL_6	HB8_VM_POLD	HB7_VM_POLD	HB6_VM_POLD	HB5_VM_POLD	HB4_VM_POLD	HB3_VM_POLD	HB2_VM_POLD	HB1_VM_POLD	RW	24h	

Table 16. PT12493 Register Map

STATUS REGISTERS

The status registers are used to report warning and fault conditions. The status registers are read-only registers.

Table 17 lists the memory-mapped registers for the status registers. All register offset addresses not listed in Table 17 should be considered as reserved locations and the register contents should not be modified.

Address	Register Name	Section
0x00	IC Status	Go
0x01	Overcurrent Protection (OCP) Status 1	Go
0x02	Overcurrent Protection (OCP) Status 2	Go
0x03	Overcurrent Protection (OCP) Status 3	Go
0x04	Open-Load Detect (OLD) Status 1	Go
0x05	Open-Load Detect (OLD) Status 2	Go
0x06	Open-Load Detect (OLD) Status 3	Go

Table 17. Status Registers Summary Table

IC STATUS (IC_STAT) REGISTER, (ADDRESS = 0X00) [RESET = 0X00]

The IC status (IC_STAT) register is shown in Figure 48 and described in Table 18.

Register access type: Read only

7	6	5	4	3	2	1	0
Reserved	OTSD	OTW	OLD	OCP	UVLO	OVP	NPOR
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Figure 48. IC Status Register

Bit	Field	Type	Default	Description
7	Reserved	R	0b	Reserved
6	OTSD	R	0b	0b = No over-temperature shutdown is detected 1b = Overcurrent condition is detected
5	OTW	R	0b	0b = No over-temperature warning is detected 1b = Overcurrent condition is detected
4	OLD	R	0b	0b = No open-load condition is detected 1b = Open-load condition is detected
3	OCP	R	0b	0b = No overcurrent condition is detected 1b = Overcurrent condition is detected
2	UVLO	R	0b	0b = No undervoltage lock-out condition is detected 1b = Under-voltage lock-out condition is detected
1	OVP	R	0b	0b = No overvoltage condition is detected 1b = Overvoltage condition is detected
0	NPOR	R	0b	0b = Power-on-reset condition is detected 1b = No power-on-reset condition is detected

Table 18. IC Status Register Field Descriptions

OVERCURRENT PROTECTION (OCP) STATUS 1 (OCP_STAT_1) REGISTER (ADDRESS = 0X01) [RESET = 0X00]

The overcurrent protection (OCP) status 1 register is shown in Figure 49 and described in Table 19.
Register access type: Read only

7	6	5	4	3	2	1	0
HB4_HS_OCP	HB4_LS_OCP	HB3_HS_OCP	HB3_LS_OCP	HB2_HS_OCP	HB2_LS_OCP	HB1_HS_OCP	HB1_LS_OCP
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Figure 49. Overcurrent Protection (OCP) Status 1 Register

Bit	Field	Type	Default	Description
7	HB4_HS_OCP	R	0b	0b = No overcurrent detected on high-side switch of half-bridge 4 1b = Overcurrent detected on high-side switch of half-bridge 4
6	HB4_LS_OCP	R	0b	0b = No overcurrent detected on low-side switch of half-bridge 4 1b = Overcurrent detected on low-side switch of half-bridge 4
5	HB3_HS_OCP	R	0b	0b = No overcurrent detected on high-side switch of half-bridge 3 1b = Overcurrent detected on high-side switch of half-bridge 3
4	HB3_LS_OCP	R	0b	0b = No overcurrent detected on low-side switch of half-bridge 3 1b = Overcurrent detected on low-side switch of half-bridge 3
3	HB2_HS_OCP	R	0b	0b = No overcurrent detected on high-side switch of half-bridge 2 1b = Overcurrent detected on high-side switch of half-bridge 2
2	HB2_LS_OCP	R	0b	0b = No overcurrent detected on low-side switch of half-bridge 2 1b = Overcurrent detected on low-side switch of half-bridge 2
1	HB1_HS_OCP	R	0b	0b = No overcurrent detected on high-side switch of half-bridge 1 1b = Overcurrent detected on high-side switch of half-bridge 1
0	HB1_LS_OCP	R	0b	0b = No overcurrent detected on low-side switch of half-bridge 1 1b = Overcurrent detected on low-side switch of half-bridge 1

Table 19. Overcurrent Protection (OCP) Status 1 Register Field Descriptions

OVERCURRENT PROTECTION (OCP) STATUS 2 (OCP_STAT_2) REGISTER (ADDRESS = 0X02) [RESET = 0X00]

The overcurrent protection (OCP) status 2 register is shown in Figure 50 and described in Table 20.
Register access type: Read only

7	6	5	4	3	2	1	0
HB8_HS_OCP	HB8_LS_OCP	HB7_HS_OCP	HB7_LS_OCP	HB6_HS_OCP	HB6_LS_OCP	HB5_HS_OCP	HB5_LS_OCP
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Figure 50. Overcurrent Protection (OCP) Status 2 Register

Bit	Field	Type	Default	Description
7	HB8_HS_OCP	R	0b	0b = No overcurrent detected on high-side switch of half-bridge 8 1b = Overcurrent detected on high-side switch of half-bridge 8
6	HB8_LS_OCP	R	0b	0b = No overcurrent detected on low-side switch of half-bridge 8 1b = Overcurrent detected on low-side switch of half-bridge 8
5	HB7_HS_OCP	R	0b	0b = No overcurrent detected on high-side switch of half-bridge 7 1b = Overcurrent detected on high-side switch of half-bridge 7
4	HB7_LS_OCP	R	0b	0b = No overcurrent detected on low-side switch of half-bridge 7 1b = Overcurrent detected on low-side switch of half-bridge 7

3	HB6_HS_OCP	R	0b	0b = No overcurrent detected on high-side switch of half-bridge 6 1b = Overcurrent detected on high-side switch of half-bridge 6
2	HB6_LS_OCP	R	0b	0b = No overcurrent detected on low-side switch of half-bridge 6 1b = Overcurrent detected on low-side switch of half-bridge 6
1	HB5_HS_OCP	R	0b	0b = No overcurrent detected on high-side switch of half-bridge 5 1b = Overcurrent detected on high-side switch of half-bridge 5
0	HB5_LS_OCP	R	0b	0b = No overcurrent detected on low-side switch of half-bridge 5 1b = Overcurrent detected on low-side switch of half-bridge 5

Table 20. Overcurrent Protection (OCP) Status 2 Register Field Descriptions

OVERCURRENT PROTECTION (OCP) STATUS 3 (OCP_STAT_3) REGISTER (ADDRESS = 0X03) [RESET = 0X00]

The overcurrent protection (OCP) status 3 register is shown in Figure 51 and described in Table 21.
Register access type: Read only

7	6	5	4	3	2	1	0
Reserved							
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Figure 51. Overcurrent Protection (OCP) Status 3 Register

Bit	Field	Type	Default	Description
7-0	Reserved	R	0b	Reserved.

Table 21. Overcurrent Protection (OCP) Status 3 Register Field Descriptions

OPEN-LOAD DETECT (OLD) STATUS 1 (OLD_STAT_1) REGISTER (ADDRESS = 0X04) [RESET = 0X00]

The open-load detect (OLD) status 1 register is shown in Figure 52 and described in Table 22.
Register access type: Read only

7	6	5	4	3	2	1	0
HB4_HS_OLD	HB4_LS_OLD	HB3_HS_OLD	HB3_LS_OLD	HB2_HS_OLD	HB2_LS_OLD	HB1_HS_OLD	HB1_LS_OLD
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Figure 52. Open-Load Detect (OLD) Status 1 Register

Bit	Field	Type	Default	Description
7	HB4_HS_OLD	R	0b	0b = No open load detected on high-side switch of half-bridge 4 1b = Open load detected on high-side switch of half-bridge 4
6	HB4_LS_OLD	R	0b	0b = No open load detected on low-side switch of half-bridge 4 1b = Open load detected on low-side switch of half-bridge 4
5	HB3_HS_OLD	R	0b	0b = No open load detected on high-side switch of half-bridge 3 1b = Open load detected on high-side switch of half-bridge 3
4	HB3_LS_OLD	R	0b	0b = No open load detected on low-side switch of half-bridge 3 1b = Open load detected on low-side switch of half-bridge 3
3	HB2_HS_OLD	R	0b	0b = No open load detected on high-side switch of half-bridge 2 1b = Open load detected on high-side switch of half-bridge 2
2	HB2_LS_OLD	R	0b	0b = No open load detected on low-side switch of half-bridge 2 1b = Open load detected on low-side switch of half-bridge 2
1	HB1_HS_OLD	R	0b	0b = No open load detected on high-side switch of half-bridge 1 1b = Open load detected on high-side switch of half-bridge 1

0	HB1_LS_OLD	R	0b	0b = No open load detected on low-side switch of half-bridge 1 1b = Open load detected on low-side switch of half-bridge 1
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Table 22. Open-Load Detect (OLD) Status 1 Register Field Descriptions

OPEN-LOAD DETECT (OLD) STATUS 2 (OLD_STAT_2) REGISTER (ADDRESS = 0X05)

[RESET = 0X00]

The open-load detect (OLD) status 2 register is shown in Figure 53 and described in Table 23.

Register access type: Read only

7	6	5	4	3	2	1	0
HB8_HS_OLD	HB8_LS_OLD	HB7_HS_OLD	HB7_LS_OLD	HB6_HS_OLD	HB6_LS_OLD	HB5_HS_OLD	HB5_LS_OLD
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Figure 53. Open-Load Detect (OLD) Status 2 Register

Bit	Field	Type	Default	Description
7	HB8_HS_OLD	R	0b	0b = No open load detected on high-side switch of half-bridge 8 1b = Open load detected on high-side switch of half-bridge 8
6	HB8_LS_OLD	R	0b	0b = No open load detected on low-side switch of half-bridge 8 1b = Open load detected on low-side switch of half-bridge 8
5	HB7_HS_OLD	R	0b	0b = No open load detected on high-side switch of half-bridge 7 1b = Open load detected on high-side switch of half-bridge 7
4	HB7_LS_OLD	R	0b	0b = No open load detected on low-side switch of half-bridge 7 1b = Open load detected on low-side switch of half-bridge 7
3	HB6_HS_OLD	R	0b	0b = No open load detected on high-side switch of half-bridge 6 1b = Open load detected on high-side switch of half-bridge 6
2	HB6_LS_OLD	R	0b	0b = No open load detected on low-side switch of half-bridge 6 1b = Open load detected on low-side switch of half-bridge 6
1	HB5_HS_OLD	R	0b	0b = No open load detected on high-side switch of half-bridge 5 1b = Open load detected on high-side switch of half-bridge 5
0	HB5_LS_OLD	R	0b	0b = No open load detected on low-side switch of half-bridge 5 1b = Open load detected on low-side switch of half-bridge 5

Table 23. Open-Load Detect (OLD) Status 2 Register Field Descriptions

OPEN-LOAD DETECT (OLD) STATUS 3 (OLD_STAT_3) REGISTER (ADDRESS = 0X06)

[RESET = 0X00]

The open-load detect (OLD) status 3 register is shown in Figure 54 and described in Table 24.

Register access type: Read only

7	6	5	4	3	2	1	0
Reserved							
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Figure 54. Open-Load Detect (OLD) Status 3 Register

Bit	Field	Type	Default	Description
7-0	Reserved	R	0b	Reserved.

Table 24. Open-Load Detect (OLD) Status 3 Register Field Descriptions

CONTROL REGISTERS

The control registers are used to configure the device. The control registers are read and write capable.

Table 25 lists the memory-mapped registers for the control registers. All register offset addresses not listed in Table 25 should be considered as reserved locations and the register contents should not be modified.

Address	Register Name	Section
0x07	Configuration Register	Go
0x08	Operation Control 1 Register	Go
0x09	Operation Control 2 Register	Go
0x0A	Operation Control 3 Register	Go
0x0B	PWM Control 1 Register	Go
0x0C	PWM Control 2 Register	Go
0x0D	Free-Wheeling Control 1 Register	Go
0x0E	Free-Wheeling Control 2 Register	Go
0x0F	PWM Map Control 1 Register	Go
0x10	PWM Map Control 2 Register	Go
0x11	PWM Map Control 3 Register	Go
0x12	PWM Map Control 4 Register	Go
0x13	PWM Frequency Control 1 Register	Go
0x14	PWM Frequency Control 2 Register	Go
0x15	PWM Duty Control Channel 1 Register	Go
0x16	PWM Duty Control Channel 2 Register	Go
0x17	PWM Duty Control Channel 3 Register	Go
0x18	PWM Duty Control Channel 4 Register	Go
0x19	PWM Duty Control Channel 5 Register	Go
0x1A	PWM Duty Control Channel 6 Register	Go
0x1B	PWM Duty Control Channel 7 Register	Go
0x1C	PWM Duty Control Channel 8 Register	Go
0x1D	Slew Rate Control 1 Register	Go
0x1E	Slew Rate Control 2 Register	Go
0x1F	Open-Load Detect (OLD) Control 1 Register	Go
0x20	Open-Load Detect (OLD) Control 2 Register	Go
0x21	Open-Load Detect (OLD) Control 3 Register	Go
0x22	Open-Load Detect (OLD) Control 4 Register	Go
0x23	Open-Load Detect (OLD) Control 5 Register	Go
0x24	Open-Load Detect (OLD) Control 6 Register	Go

Table 25. Control Registers Summary Table

CONFIGURATION (CONFIG_CTRL) REGISTER, (ADDRESS = 0X07) [RESET = 0X00]

The configuration register is shown in Figure 55 and described in Table 26.

Register access type: Read/Write

7	6	5	4	3	2	1	0
POLD_EN		IC_ID		OCP_REP	OTW_REP	EXT_OVP	CLR_FLT
R/W-0b	R-Xb	R-Xb	R-Xb	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Figure 55. Configuration Register

Bit	Field	Type	Default	Description
7	POLD_EN	RW	0b	0b = Passive OLD is disabled 1b = Passive OLD is enabled
6-4	IC_ID	R	XXXb	000b = Reserved 001b = Reserved 010b = Device connected is PT12493 (8 Channel Device) 011b = Reserved 100b = Reserved 101b = Reserved 110b = Reserved 111b = Reserved
3	OCP_REP	RW	0b	0b = Overcurrent condition is reported in FALTN pin 1b = Overcurrent condition warning is not reported on the FALTN pin
2	OTW_REP	RW	0b	0b = Overtemperature warning is not reported in FALTN pin 1b = Overtemperature warning is reported on the FALTN pin
1	EXT_OVP	RW	0b	0b = Overvoltage protection threshold is at 21 V 1b = Overvoltage protection threshold is at 33 V
0	CLR_FLT	RW	0b	0b = Faults not cleared 1b = Clear all faults

Table 26. Configuration Register Field Descriptions

NOTE

CLR_FLT bit is an auto-clear bit and will always read 0b.

OPERATION CONTROL 1 (OP_CTRL_1) REGISTER (ADDRESS = 0X08) [RESET = 0X00]

The operation control 1 register is shown in Figure 56 and described in Table 27.

Register access type: Read/Write

7	6	5	4	3	2	1	0
HB4_HS_EN	HB4_LS_EN	HB3_HS_EN	HB3_LS_EN	HB2_HS_EN	HB2_LS_EN	HB1_HS_EN	HB1_LS_EN
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Figure 56. Operation Control 1 Register

Bit	Field	Type	Default	Description
7	HB4_HS_EN	RW	0b	0b = Half-bridge 4 high-side switch is disabled 1b = Half-bridge 4 high-side switch is enabled
6	HB4_LS_EN	RW	0b	0b = Half-bridge 4 low-side switch is disabled 1b = Half-bridge 4 low-side switch is enabled
5	HB3_HS_EN	RW	0b	0b = Half-bridge 3 high-side switch is disabled 1b = Half-bridge 3 high-side switch is enabled
4	HB3_LS_EN	RW	0b	0b = Half-bridge 3 low-side switch is disabled 1b = Half-bridge 3 low-side switch is enabled

3	HB2_HS_EN	R/W	0b	0b = Half-bridge 2 high-side switch is disabled 1b = Half-bridge 2 high-side switch is enabled
2	HB2_LS_EN	R/W	0b	0b = Half-bridge 2 low-side switch is disabled 1b = Half-bridge 2 low-side switch is enabled
1	HB1_HS_EN	R/W	0b	0b = Half-bridge 1 high-side switch is disabled 1b = Half-bridge 1 high-side switch is enabled
0	HB1_LS_EN	R/W	0b	0b = Half-bridge 1 low-side switch is disabled 1b = Half-bridge 1 low-side switch is enabled

Table 27. Operation Control 1 Register Field Descriptions

OPERATION CONTROL 2 (OP_CTRL_2) REGISTER (ADDRESS = 0X09) [RESET = 0X00]

The operation control 2 register is shown in Figure 57 and described in Table 28.

Register access type: Read/Write

7	6	5	4	3	2	1	0
HB8_HS_EN	HB8_LS_EN	HB7_HS_EN	HB7_LS_EN	HB6_HS_EN	HB6_LS_EN	HB5_HS_EN	HB5_LS_EN
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Figure 57. Operation Control 2 Register

Bit	Field	Type	Default	Description
7	HB8_HS_EN	R/W	0b	0b = Half-bridge 8 high-side switch is disabled 1b = Half-bridge 8 high-side switch is enabled
6	HB8_LS_EN	R/W	0b	0b = Half-bridge 8 low-side switch is disabled 1b = Half-bridge 8 low-side switch is enabled
5	HB7_HS_EN	R/W	0b	0b = Half-bridge 7 high-side switch is disabled 1b = Half-bridge 7 high-side switch is enabled
4	HB7_LS_EN	R/W	0b	0b = Half-bridge 7 low-side switch is disabled 1b = Half-bridge 7 low-side switch is enabled
3	HB6_HS_EN	R/W	0b	0b = Half-bridge 6 high-side switch is disabled 1b = Half-bridge 6 high-side switch is enabled
2	HB6_LS_EN	R/W	0b	0b = Half-bridge 6 low-side switch is disabled 1b = Half-bridge 6 low-side switch is enabled
1	HB5_HS_EN	R/W	0b	0b = Half-bridge 5 high-side switch is disabled 1b = Half-bridge 5 high-side switch is enabled
0	HB5_LS_EN	R/W	0b	0b = Half-bridge 5 low-side switch is disabled 1b = Half-bridge 5 low-side switch is enabled

Table 28. Operation Control 2 Register Field Descriptions

OPERATION CONTROL 3 (OP_CTRL_3) REGISTER (ADDRESS = 0X0A) [RESET = 0X00]

The operation control 3 register is shown in Figure 58 and described in Table 29.

Register access type: Read

7	6	5	4	3	2	1	0
Reserved							
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

Figure 58. Operation Control 3 Register

Bit	Field	Type	Default	Description
7-0	Reserved	R	0b	Reserved.

Table 29. Operation Control 3 Register Field Descriptions

PWM CONTROL 1 (PWM_CTRL_1) REGISTER, (ADDRESS = 0X0B) [RESET = 0X00]

The PWM control 1 register is shown in Figure 59 and described in Table 30.

Register access type: Read/Write

7	6	5	4	3	2	1	0
HB8_PWM	HB7_PWM	HB6_PWM	HB5_PWM	HB4_PWM	HB3_PWM	HB2_PWM	HB1_PWM
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Figure 59. PWM Control 1 Register

Bit	Field	Type	Default	Description
7	HB8_PWM	RW	0b	0b = Half-bridge 8 is operating in continuous mode 1b = Half-bridge 8 is operating in PWM mode
6	HB7_PWM	RW	0b	0b = Half-bridge 7 is operating in continuous mode 1b = Half-bridge 7 is operating in PWM mode
5	HB6_PWM	RW	0b	0b = Half-bridge 6 is operating in continuous mode 1b = Half-bridge 6 is operating in PWM mode
4	HB5_PWM	RW	0b	0b = Half-bridge 5 is operating in continuous mode 1b = Half-bridge 5 is operating in PWM mode
3	HB4_PWM	RW	0b	0b = Half-bridge 4 is operating in continuous mode 1b = Half-bridge 4 is operating in PWM mode
2	HB3_PWM	RW	0b	0b = Half-bridge 3 is operating in continuous mode 1b = Half-bridge 3 is operating in PWM mode
1	HB2_PWM	RW	0b	0b = Half-bridge 2 is operating in continuous mode 1b = Half-bridge 2 is operating in PWM mode
0	HB1_PWM	RW	0b	0b = Half-bridge 1 is operating in continuous mode 1b = Half-bridge 1 is operating in PWM mode

Table 30. PWM Control 1 Register Field Descriptions

PWM CONTROL 2 (PWM_CTRL_2) REGISTER (ADDRESS = 0X0C) [RESET = 0X00]

The PWM control 2 register is shown in Figure 60 and described in Table 31.

Register access type: Read/Write

7	6	5	4	3	2	1	0
PWM_CH8_DIS	PWM_CH7_DIS	PWM_CH6_DIS	PWM_CH5_DIS	PWM_CH4_DIS	PWM_CH3_DIS	PWM_CH2_DIS	PWM_CH1_DIS
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Figure 60. PWM Control 2 Register

Bit	Field	Type	Default	Description
7	PWM_CH8_DIS	R/W	0b	0b = PWM Generator-8 is enabled 1b = PWM Generator-8 is disabled
6	PWM_CH7_DIS	R/W	0b	0b = PWM Generator-7 is enabled 1b = PWM Generator-7 is disabled
5	PWM_CH6_DIS	R/W	0b	0b = PWM Generator-6 is enabled 1b = PWM Generator-6 is disabled
4	PWM_CH5_DIS	R/W	0b	0b = PWM Generator-5 is enabled 1b = PWM Generator-5 is disabled
3	PWM_CH4_DIS	R/W	0b	0b = PWM Generator-4 is enabled 1b = PWM Generator-4 is disabled
2	PWM_CH3_DIS	R/W	0b	0b = PWM Generator-3 is enabled 1b = PWM Generator-3 is disabled
1	PWM_CH2_DIS	R/W	0b	0b = PWM Generator-2 is enabled 1b = PWM Generator-2 is disabled
0	PWM_CH1_DIS	R/W	0b	0b = PWM Generator-1 is enabled 1b = PWM Generator-1 is disabled

Table 31. PWM Control 2 Register Field Descriptions

FREE-WHEELING CONTROL 1 (FW_CTRL_1) REGISTER (ADDRESS = 0X0D) [RESET = 0X00]

The free-wheeling control 1 register is shown in Figure 61 and described in Table 32.

Register access type: Read/Write

7	6	5	4	3	2	1	0
HB8_FW	HB7_FW	HB6_FW	HB5_FW	HB4_FW	HB3_FW	HB2_FW	HB1_FW
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Figure 61. Free-Wheeling Control 1 Register

Bit	Field	Type	Default	Description
7	HB8_FW	R/W	0b	0b = Passive free-wheeling on half-bridge 8 is enabled 1b = Active free-wheeling on half-bridge 8 is enabled
6	HB7_FW	R/W	0b	0b = Passive free-wheeling on half-bridge 7 is enabled 1b = Active free-wheeling on half-bridge 7 is enabled
5	HB6_FW	R/W	0b	0b = Passive free-wheeling on half-bridge 6 is enabled 1b = Active free-wheeling on half-bridge 6 is enabled
4	HB5_FW	R/W	0b	0b = Passive free-wheeling on half-bridge 5 is enabled 1b = Active free-wheeling on half-bridge 5 is enabled
3	HB4_FW	R/W	0b	0b = Passive free-wheeling on half-bridge 4 is enabled 1b = Active free-wheeling on half-bridge 4 is enabled

2	HB3_FW	R/W	0b	0b = Passive free-wheeling on half-bridge 3 is enabled 1b = Active free-wheeling on half-bridge 3 is enabled
1	HB2_FW	R/W	0b	0b = Passive free-wheeling on half-bridge 2 is enabled 1b = Active free-wheeling on half-bridge 2 is enabled
0	HB1_FW	R/W	0b	0b = Passive free-wheeling on half-bridge 1 is enabled 1b = Active free-wheeling on half-bridge 1 is enabled

Table 32. Free-Wheeling Control 1 Register Field Descriptions

FREE-WHEELING CONTROL 2 (FW_CTRL_2) REGISTER (ADDRESS = 0X0E) [RESET = 0X00]

The free-wheeling control 2 register is shown in Figure 62 and described in Table 33.
Register access type: Read/Write

7	6	5	4	3	2	1	0
Reserved							
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Figure 62. Free-Wheeling Control 2 Register

Bit	Field	Type	Default	Description
7-0	Reserved	R/W	0000b	Reserved.

Table 33. Free-Wheeling Control 2 Register Field Descriptions

PWM MAP CONTROL 1 (PWM_MAP_CTRL_1) REGISTER (ADDRESS = 0X0F) [RESET = 0X00]

The PWM Map Control 1 register is shown in Figure 63 and described in Table 34.
Register access type: Read/Write

7	6	5	4	3	2	1	0
Reserved			HB2_PWM_MAP		HB1_PWM_MAP		
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Figure 63. PWM Map Control 1 Register

Bit	Field	Type	Default	Description
7-6	Reserved	R	00b	Reserved
5-3	HB2_PWM_MAP	R/W	000b	000b = HB2 mapped to PWM channel 1 001b = HB2 mapped to PWM channel 2 010b = HB2 mapped to PWM channel 3 011b = HB2 mapped to PWM channel 4 100b = HB2 mapped to PWM channel 5 101b = HB2 mapped to PWM channel 6 110b = HB2 mapped to PWM channel 7 111b = HB2 mapped to PWM channel 8

2-0	HB1_PWM_MAP	R/W	000b	000b = HB1 mapped to PWM channel 1 001b = HB1 mapped to PWM channel 2 010b = HB1 mapped to PWM channel 3 011b = HB1 mapped to PWM channel 4 100b = HB1 mapped to PWM channel 5 101b = HB1 mapped to PWM channel 6 110b = HB1 mapped to PWM channel 7 111b = HB1 mapped to PWM channel 8
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Table 34. PWM Map Control 1 Register Field Descriptions

PWM MAP CONTROL 2 (PWM_MAP_CTRL_2) REGISTER (ADDRESS = 0X10) [RESET = 0X00]

The PWM frequency map control 2 register is shown in Figure 64 and described in Table 35. Register access type: Read/Write

7	6	5	4	3	2	1	0
Reserved		HB4_PWM_MAP			HB3_PWM_MAP		
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Figure 64. PWM Map Control 2 Register

Bit	Field	Type	Default	Description
7-6	Reserved	R	00b	Reserved
5-3	HB4_PWM_MAP	R/W	000b	000b = HB4 mapped to PWM channel 1 001b = HB4 mapped to PWM channel 2 010b = HB4 mapped to PWM channel 3 011b = HB4 mapped to PWM channel 4 100b = HB4 mapped to PWM channel 5 101b = HB4 mapped to PWM channel 6 110b = HB4 mapped to PWM channel 7 111b = HB4 mapped to PWM channel 8
2-0	HB3_PWM_MAP	R/W	000b	000b = HB3 mapped to PWM channel 1 001b = HB3 mapped to PWM channel 2 010b = HB3 mapped to PWM channel 3 011b = HB3 mapped to PWM channel 4 100b = HB3 mapped to PWM channel 5 101b = HB3 mapped to PWM channel 6 110b = HB3 mapped to PWM channel 7 111b = HB3 mapped to PWM channel 8

Table 35. PWM Map Control 2 Register Field Descriptions

PWM MAP CONTROL 3 (PWM_MAP_CTRL_3) REGISTER (ADDRESS = 0X11) [RESET = 0X00]

The PWM frequency map control 3 register is shown in Figure 65 and described in Table 36. Register access type: Read/Write

7	6	5	4	3	2	1	0
Reserved		HB6_PWM_MAP			HB5_PWM_MAP		
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Figure 65. PWM Map Control 3 Register

Bit	Field	Type	Default	Description
7-6	Reserved	R	00b	Reserved
5-3	HB6_PWM_MAP	R/W	000b	000b = HB6 mapped to PWM channel 1 001b = HB6 mapped to PWM channel 2 010b = HB6 mapped to PWM channel 3 011b = HB6 mapped to PWM channel 4 100b = HB6 mapped to PWM channel 5 101b = HB6 mapped to PWM channel 6 110b = HB6 mapped to PWM channel 7 111b = HB6 mapped to PWM channel 8
2-0	HB5_PWM_MAP	R/W	000b	000b = HB5 mapped to PWM channel 1 001b = HB5 mapped to PWM channel 2 010b = HB5 mapped to PWM channel 3 011b = HB5 mapped to PWM channel 4 100b = HB5 mapped to PWM channel 5 101b = HB5 mapped to PWM channel 6 110b = HB5 mapped to PWM channel 7 111b = HB5 mapped to PWM channel 8

Table 36. PWM Map Control 3 Register Field Descriptions

PWM MAP CONTROL 4 (PWM_MAP_CTRL_4) REGISTER (ADDRESS = 0X12) [RESET = 0X00]

The PWM frequency map control 4 register is shown in Figure 66 and described in Table 37.
Register access type: Read/Write

7	6	5	4	3	2	1	0
Reserved		HB8_PWM_MAP			HB7_PWM_MAP		
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Figure 66. PWM Map Control 4 Register

Bit	Field	Type	Default	Description
7-6	Reserved	R	00b	Reserved
5-3	HB8_PWM_MAP	R/W	000b	000b = HB8 mapped to PWM channel 1 001b = HB8 mapped to PWM channel 2 010b = HB8 mapped to PWM channel 3 011b = HB8 mapped to PWM channel 4 100b = HB8 mapped to PWM channel 5 101b = HB8 mapped to PWM channel 6 110b = HB8 mapped to PWM channel 7 111b = HB8 mapped to PWM channel 8
2-0	HB7_PWM_MAP	R/W	000b	000b = HB7 mapped to PWM channel 1 001b = HB7 mapped to PWM channel 2 010b = HB7 mapped to PWM channel 3 011b = HB7 mapped to PWM channel 4 100b = HB7 mapped to PWM channel 5 101b = HB7 mapped to PWM channel 6 110b = HB7 mapped to PWM channel 7 111b = HB7 mapped to PWM channel 8

Table 37. PWM Map Control 4 Register Field Descriptions

PWM FREQUENCY CONTROL 1 (PWM_FREQ_CTRL_1) REGISTER (ADDRESS = 0X13)

[RESET = 0X00]

The PWM frequency control register 1 is shown in Figure 67 and described in Table 38.
Register access type: Read/Write

7	6	5	4	3	2	1	0
PWM_CH4_FREQ		PWM_CH3_FREQ		PWM_CH2_FREQ		PWM_CH1_FREQ	
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Figure 67. PWM Frequency Control 1 Register

Bit	Field	Type	Default	Description
7-6	PWM_CH4_FREQ	R/W	00b	00b = PWM frequency is 80 Hz 01b = PWM frequency is 100 Hz 10b = PWM frequency is 200 Hz 11b = PWM frequency is 2000 Hz
5-4	PWM_CH3_FREQ	R/W	00b	00b = PWM frequency is 80 Hz 01b = PWM frequency is 100 Hz 10b = PWM frequency is 200 Hz 11b = PWM frequency is 2000 Hz
3-2	PWM_CH2_FREQ	R/W	00b	00b = PWM frequency is 80 Hz 01b = PWM frequency is 100 Hz 10b = PWM frequency is 200 Hz 11b = PWM frequency is 2000 Hz
1-0	PWM_CH1_FREQ	R/W	00b	00b = PWM frequency is 80 Hz 01b = PWM frequency is 100 Hz 10b = PWM frequency is 200 Hz 11b = PWM frequency is 2000 Hz

Table 38. PWM Frequency Control 1 Register Field Descriptions

PWM FREQUENCY CONTROL 2 (PWM_FREQ_CTRL_2) REGISTER (ADDRESS = 0X14)

[RESET = 0X00]

The PWM frequency control register 2 is shown in Figure 68 and described in Table 39.
Register access type: Read/Write

7	6	5	4	3	2	1	0
PWM_CH8_FREQ		PWM_CH7_FREQ		PWM_CH6_FREQ		PWM_CH5_FREQ	
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Figure 68. PWM Frequency Control 2 Register

Bit	Field	Type	Default	Description
7-6	PWM_CH8_FREQ	R/W	00b	00b = PWM frequency is 80 Hz 01b = PWM frequency is 100 Hz 10b = PWM frequency is 200 Hz 11b = PWM frequency is 2000 Hz
5-4	PWM_CH7_FREQ	R/W	00b	00b = PWM frequency is 80 Hz 01b = PWM frequency is 100 Hz 10b = PWM frequency is 200 Hz 11b = PWM frequency is 2000 Hz

3-2	PWM_CH6_FREQ	R/W	00b	00b = PWM frequency is 80 Hz 01b = PWM frequency is 100 Hz 10b = PWM frequency is 200 Hz 11b = PWM frequency is 2000 Hz
1-0	PWM_CH5_FREQ	R/W	00b	00b = PWM frequency is 80 Hz 01b = PWM frequency is 100 Hz 10b = PWM frequency is 200 Hz 11b = PWM frequency is 2000 Hz

Table 39. PWM Frequency Control 2 Register Field Descriptions

PWM DUTY CONTROL CHANNEL 1 (PWM_DUTY_CH1) REGISTER (ADDRESS = 0X15)

[RESET = 0X00]

The channel 1 PWM duty cycle control register is shown in Figure 69 and described in Table 40.
Register access type: Read/Write

7	6	5	4	3	2	1	0
PWM_DUTY_CH1							
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Figure 69. PWM Duty Control Channel 1 Register

Bit	Field	Type	Default	Description
7-0	PWM_DUTY_CH1	R/W	00000000b	00000000b = 0 % PWM Duty 11111111b = 100 % PWM Duty Calculate duty as decimal (xxxxxxx) × 1/255

Table 40. PWM Duty Control Channel 1 Register Field Descriptions

PWM DUTY CONTROL CHANNEL 2 (PWM_DUTY_CH2) REGISTER (ADDRESS = 0X16)

[RESET = 0X00]

The channel 2 PWM duty cycle control register is shown in Figure 70 and described in Table 41.
Register access type: Read/Write

7	6	5	4	3	2	1	0
PWM_DUTY_CH2							
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Figure 70. PWM Duty Control Channel 2 Register

Bit	Field	Type	Default	Description
7-0	PWM_DUTY_CH2	R/W	00000000b	00000000b = 0 % PWM Duty 11111111b = 100 % PWM Duty Calculate duty as decimal (xxxxxxx) × 1/255

Table 41. PWM Duty Control Channel 2 Register Field Descriptions

PWM DUTY CONTROL CHANNEL 3 (PWM_DUTY_CH3) REGISTER (ADDRESS = 0X17)

[RESET = 0X00]

The channel 3 PWM duty cycle control register is shown in Figure 71 and described in Table 42.
Register access type: Read/Write

7	6	5	4	3	2	1	0
PWM_DUTY_CH3							
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Figure 71. PWM Duty Control Channel 3 Register

Bit	Field	Type	Default	Description
7-0	PWM_DUTY_CH3	R/W	00000000b	00000000b = 0 % PWM Duty 11111111b = 100 % PWM Duty Calculate duty as decimal (xxxxxxxxb) × 1/255

Table 42. PWM Duty Control Channel 3 Register Field Descriptions

PWM DUTY CONTROL CHANNEL 4 (PWM_DUTY_CH4) REGISTER (ADDRESS = 0X18)

[RESET = 0X00]

The channel 4 PWM duty cycle control register is shown in Figure 72 and described in Table 43.
Register access type: Read/Write

7	6	5	4	3	2	1	0
PWM_DUTY_CH4							
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Figure 72. PWM Duty Control Channel 4 Register

Bit	Field	Type	Default	Description
7-0	PWM_DUTY_CH4	R/W	00000000b	00000000b = 0 % PWM Duty 11111111b = 100 % PWM Duty Calculate duty as decimal (xxxxxxxxb) × 1/255

Table 43. PWM Duty Control Channel 4 Register Field Descriptions

PWM DUTY CONTROL CHANNEL 5 (PWM_DUTY_CH5) REGISTER (ADDRESS = 0X19)

[RESET = 0X00]

The channel 5 PWM duty cycle control register is shown in Figure 73 and described in Table 44.
Register access type: Read/Write

7	6	5	4	3	2	1	0
PWM_DUTY_CH5							
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Figure 73. PWM Duty Control Channel 5 Register

Bit	Field	Type	Default	Description
7-0	PWM_DUTY_CH5	R/W	00000000b	00000000b = 0 % PWM Duty 11111111b = 100 % PWM Duty Calculate duty as decimal (xxxxxxxxb) × 1/255

Table 44. PWM Duty Control Channel 5 Register Field Descriptions

PWM DUTY CONTROL CHANNEL 6 (PWM_DUTY_CH6) REGISTER (ADDRESS = 0X1A)

[RESET = 0X00]

The channel 6 PWM duty cycle control register is shown in Figure 74 and described in Table 45.
Register access type: Read/Write

7	6	5	4	3	2	1	0
PWM_DUTY_CH6							
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Figure 74. PWM Duty Control Channel 6 Register

Bit	Field	Type	Default	Description
7-0	PWM_DUTY_CH6	R/W	00000000b	00000000b = 0 % PWM Duty 11111111b = 100 % PWM Duty Calculate duty as decimal (xxxxxxxxb) × 1/255

Table 45. PWM Duty Control Channel 6 Register Field Descriptions

PWM DUTY CONTROL CHANNEL 7 (PWM_DUTY_CH7) REGISTER (ADDRESS = 0X1B)

[RESET = 0X00]

The channel 7 PWM duty cycle control register is shown in Figure 75 and described in Table 46.
Register access type: Read/Write

7	6	5	4	3	2	1	0
PWM_DUTY_CH7							
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Figure 75. PWM Duty Control Channel 7 Register

Bit	Field	Type	Default	Description
7-0	PWM_DUTY_CH7	R/W	00000000b	00000000b = 0 % PWM Duty 11111111b = 100 % PWM Duty Calculate duty as decimal (xxxxxxxxb) × 1/255

Table 46. PWM Duty Control Channel 7 Register Field Descriptions

PWM DUTY CONTROL CHANNEL 8 (PWM_DUTY_CH8) REGISTER (ADDRESS = 0X1C)

[RESET = 0X00]

The channel 8 PWM duty cycle control register is shown in Figure 76 and described in Table 47.
Register access type: Read/Write

7	6	5	4	3	2	1	0
PWM_DUTY_CH8							
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Figure 76. PWM Duty Control Channel 8 Register

Bit	Field	Type	Default	Description
7-0	PWM_DUTY_CH8	R/W	00000000b	00000000b = 0 % PWM Duty 11111111b = 100 % PWM Duty Calculate duty as decimal (xxxxxxxxb) × 1/255

Table 47. PWM Duty Control Channel 8 Register Field Descriptions

SLEW RATE CONTROL 1 (SR_CTRL_1) REGISTER (ADDRESS = 0X1D [RESET = 0X00])

The slew rate control 1 register is shown in Figure 77 and described in Table 48.

Register access type: Read/Write

7	6	5	4	3	2	1	0
HB8_SR	HB7_SR	HB6_SR	HB5_SR	HB4_SR	HB3_SR	HB2_SR	HB1_SR
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Figure 77. Slew Rate Control 1 Register

Bit	Field	Type	Default	Description
7	HB8_SR	R/W	0b	0b = 0.6 V/μs 1b = 2.5 V/μs
6	HB7_SR	R/W	0b	0b = 0.6 V/μs 1b = 2.5 V/μs
5	HB6_SR	R/W	0b	0b = 0.6 V/μs 1b = 2.5 V/μs
4	HB5_SR	R/W	0b	0b = 0.6 V/μs 1b = 2.5 V/μs
3	HB4_SR	R/W	0b	0b = 0.6 V/μs 1b = 2.5 V/μs
2	HB3_SR	R/W	0b	0b = 0.6 V/μs 1b = 2.5 V/μs
1	HB2_SR	R/W	0b	0b = 0.6 V/μs 1b = 2.5 V/μs
0	HB1_SR	R/W	0b	0b = 0.6 V/μs 1b = 2.5 V/μs

Table 48. Slew Rate Control 1 Register Field Descriptions

SLEW RATE CONTROL 2 (SR_CTRL_2) REGISTER (ADDRESS = 0X1E) [RESET = 0X00]

The slew rate control 2 register is shown in Figure 78 and described in Table 49.

Register access type: Read/Write

7	6	5	4				
Reserved							
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Figure 78. Slew Rate Control 2 Register

Bit	Field	Type	Default	Description
7-4	Reserved	R/W	0000b	Reserved

Table 49. Slew Rate Control 2 Register Field Descriptions

OPEN-LOAD DETECT (OLD) CONTROL 1 (OLD_CTRL_1) REGISTER (ADDRESS = 0X1F)

[RESET = 0X00]

The open-load detect (OLD) control (OLD_CTRL_1) register-1 is shown in Figure 79 and described in Table 50. Register access type: Read/Write

7	6	5	4	3	2	1	0
HB8_OLD_DIS	HB7_OLD_DIS	HB6_OLD_DIS	HB5_OLD_DIS	HB4_OLD_DIS	HB3_OLD_DIS	HB2_OLD_DIS	HB1_OLD_DIS
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Figure 79. Open-Load Detect (OLD) Control (OLD_CTRL_1) Register

Bit	Field	Type	Default	Description
7	HB8_OLD_DIS	R/W	0b	0b = Open-load detection on half-bridge 8 is enabled 1b = Open-load on half-bridge 8 is disabled
6	HB7_OLD_DIS	R/W	0b	0b = Open-load detection on half-bridge 7 is enabled 1b = Open-load on half-bridge 7 is disabled
5	HB6_OLD_DIS	R/W	0b	0b = Open-load detection on half-bridge 6 is enabled 1b = Open-load on half-bridge 6 is disabled
4	HB5_OLD_DIS	R/W	0b	0b = Open-load detection on half-bridge 5 is enabled 1b = Open-load on half-bridge 5 is disabled
3	HB4_OLD_DIS	R/W	0b	0b = Open-load detection on half-bridge 4 is enabled 1b = Open-load on half-bridge 4 is disabled
2	HB3_OLD_DIS	R/W	0b	0b = Open-load detection on half-bridge 3 is enabled 1b = Open-load on half-bridge 3 is disabled
1	HB2_OLD_DIS	R/W	0b	0b = Open-load detection on half-bridge 2 is enabled 1b = Open-load on half-bridge 2 is disabled
0	HB1_OLD_DIS	R/W	0b	0b = Open-load detection on half-bridge 1 is enabled 1b = Open-load on half-bridge 1 is disabled

Table 50. Open-Load Detect (OLD) Control (OLD_CTRL_1) Register Field Descriptions

OPEN-LOAD DETECT (OLD) CONTROL 2 (OLD_CTRL_2) REGISTER (ADDRESS = 0X20)

[RESET = 0X00]

The open-load detect (OLD) control (OLD_CTRL_2) register-2 is shown in Figure 80 and described in Table 51. Register access type: Read/Write

7	6	5	4	3	2	1	0
OLD_REP	OLD_OP	PL_MODE_EN				Reserved	
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Figure 80. Open-Load Detect (OLD) Control (OLD_CTRL_2) Register

Bit	Field	Type	Default	Description
7	OLD_REP	R/W	0b	0b = Report on FALTN pin during OLD condition 1b = No report on FALTN pin during OLD condition
6	OLD_OP	R/W	0b	0b = Half bridges are not active after OLD condition detect 1b = Half bridges are active after OLD condition detect
5-4	PL_MODE_EN	R/W	00b	00b = Parallel mode OCP fast turn-off slew is enabled 01b = Parallel mode OCP slow turn-off slew is enabled 10b = Invalid Setting 11b = Invalid Setting
3-0	Reserved	R	0b	Reserved

Table 51. Open-Load Detect (OLD) Control (OLD_CTRL_2) Register Field Descriptions

OPEN-LOAD DETECT (OLD) CONTROL 3 (OLD_CTRL_3) REGISTER (ADDRESS = 0X21)

[RESET = 0X00]

The open-load detect (OLD) control (OLD_CTRL_3) register-3 is shown in Figure 81 and described in Table 52. This register also contains the bits to set the OCP deglitch time (OCP_DEG).

Register access type: Read/Write

7	6	5	4	3	2	1	0
OCP_DEG		OLD_NEG_EN		Reserved			
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Figure 81. Open-Load Detect (OLD) Control (OLD_CTRL_3) Register

Bit	Field	Type	Default	Description
7-5	OCP_DEG	R/W	000b	000b = OCP deglitch time is 10 μs 001b = OCP deglitch time is 5 μs 010b = OCP deglitch time is 2.5μs 011b = OCP deglitch time is 1 μs 100b = OCP deglitch time is 60 μs 101b = OCP deglitch time is 40 μs 110b = OCP deglitch time is 30 μs 111b = OCP deglitch time is 20 μs
4	OLD_NEG_EN	R/W	0b	0b = Negative-current OLD mode is disabled 1b = Negative-current OLD mode is enabled
3-0	Reserved	R/W	0b	Reserved

Table 52. Open-Load Detect (OLD) Control (OLD_CTRL_3) Register Field Descriptions

OPEN LOAD DETECT (OLD) CONTROL 4 (OLD_CTRL_4) REGISTER (ADDRESS = 0X22)

[RESET = 0X00]

The open load detect (OLD) control (OLD_CTRL_4) register-4 is shown in Figure 82 and described in Table 53. Register access type: Read/Write

7	6	5	4	3	2	1	0
HB8_LCOLD_EN	HB7_LOLD_EN	HB6_LOLD_EN	HB5_LOLD_EN	HB4_LOLD_EN	HB3_LOLD_EN	HB2_LOLD_EN	HB1_LOLD_EN
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Figure 82. Open Load Detect (OLD) Control (OLD_CTRL_4) Register

Bit	Field	Type	Default	Description
7	HB8_LOLD_EN	R/W	0b	0b = Low-current OLD on half-bridge 8 is disabled 1b = Low-current OLD on half-bridge 8 is enabled
6	HB7_LOLD_EN	R/W	0b	0b = Low-current OLD on half-bridge 7 is disabled 1b = Low-current OLD on half-bridge 7 is enabled
5	HB6_LOLD_EN	R/W	0b	0b = Low-current OLD on half-bridge 6 is disabled 1b = Low-current OLD on half-bridge 6 is enabled
4	HB5_LOLD_EN	R/W	0b	0b = Low-current OLD on half-bridge 5 is disabled 1b = Low-current OLD on half-bridge 5 is enabled
3	HB4_LOLD_EN	R/W	0b	0b = Low-current OLD on half-bridge 4 is disabled 1b = Low-current OLD on half-bridge 4 is enabled
2	HB3_LOLD_EN	R/W	0b	0b = Low-current OLD on half-bridge 3 is disabled 1b = Low-current OLD on half-bridge 3 is enabled
1	HB2_LOLD_EN	R/W	0b	0b = Low-current OLD on half-bridge 2 is disabled 1b = Low-current OLD on half-bridge 2 is enabled
0	HB1_LOLD_EN	R/W	0b	0b = Low-current OLD on half-bridge 1 is disabled 1b = Low-current OLD on half-bridge 1 is enabled

Table 53. Open Load Detect (OLD) Control (OLD_CTRL_4) Register Field Descriptions

OPEN LOAD DETECT (OLD) CONTROL 5 (OLD_CTRL_5) REGISTER (ADDRESS = 0X23)

[RESET = 0X00]

The open load detect (OLD) (OLD_CTRL_5) register-5 is shown in Figure 83 and described in Table 54.

7	6	5	4	3	2	1	0
HB8_POLD_EN	HB7_POLD_EN	HB6_POLD_EN	HB5_POLD_EN	HB4_POLD_EN	HB3_POLD_EN	HB2_POLD_EN	HB1_POLD_EN
N	N	N	N	N	N	N	N
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Figure 83. Open Load Detect (OLD) Control (OLD_CTRL_5) Register

Bit	Field	Type	Default	Description
7	HB8_POLD_EN	R/W	0b	0b = Passive OLD operation of half-bridge 8 is disabled 1b = Passive OLD operation of half-bridge 8 is enabled
6	HB7_POLD_EN	R/W	0b	0b = Passive OLD operation of half-bridge 7 is disabled 1b = Passive OLD operation of half-bridge 7 is enabled
5	HB6_POLD_EN	R/W	0b	0b = Passive OLD operation of half-bridge 6 is disabled 1b = Passive OLD operation of half-bridge 6 is enabled
4	HB5_POLD_EN	R/W	0b	0b = Passive OLD operation of half-bridge 5 is disabled 1b = Passive OLD operation of half-bridge 5 is enabled
3	HB4_POLD_EN	R/W	0b	0b = Passive OLD operation of half-bridge 4 is disabled 1b = Passive OLD operation of half-bridge 4 is enabled
2	HB3_POLD_EN	R/W	0b	0b = Passive OLD operation of half-bridge 3 is disabled 1b = Passive OLD operation of half-bridge 3 is enabled
1	HB2_POLD_EN	R/W	0b	0b = Passive OLD operation of half-bridge 2 is disabled 1b = Passive OLD operation of half-bridge 2 is enabled
0	HB1_POLD_EN	R/W	0b	0b = Passive OLD operation of half-bridge 1 is disabled 1b = Passive OLD operation of half-bridge 1 is enabled

Table 54. Open Load Detect (OLD) Control (OLD_CTRL_5) Register Field Descriptions

OPEN LOAD DETECT (OLD) CONTROL 6 (OLD_CTRL_6) REGISTER (ADDRESS = 0X24)

[RESET = 0X00]

The open load detect (OLD) (OLD_CTRL_6) register-6 register is shown in Figure 84 and described in Table 55.

7	6	5	4	3	2	1	0
HB8_VM_POL D	HB7_VM_POL D	HB6_VM_POL D	HB5_VM_POL D	HB4_VM_POL D	HB3_VM_POL D	HB2_VM_POL D	HB1_VM_POL D
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

Figure 84. Open Load Detect (OLD) Control (OLD_CTRL_6) Register

Bit	Field	Type	Default	Description
7	HB8_VM_POLD	R/W	0b	0b = Passive OLD operation for VM connected load of half- bridge 8 is disabled 1b = Passive OLD operation for VM connected load of half- bridge 8 is enabled
6	HB7_VM_POLD	R/W	0b	0b = Passive OLD operation for VM connected load of half- bridge 7 is disabled 1b = Passive OLD operation for VM connected load of half- bridge 7 is enabled
5	HB6_VM_POLD	R/W	0b	0b = Passive OLD operation for VM connected load of half- bridge 6 is disabled 1b = Passive OLD operation for VM connected load of half- bridge 6 is enabled
4	HB5_VM_POLD	R/W	0b	0b = Passive OLD operation for VM connected load of half- bridge 5 is disabled 1b = Passive OLD operation for VM connected load of half- bridge 5 is enabled
3	HB4_VM_POLD	R/W	0b	0b = Passive OLD operation for VM connected load of half- bridge 4 is disabled 1b = Passive OLD operation for VM connected load of half- bridge 4 is enabled
2	HB3_VM_POLD	R/W	0b	0b = Passive OLD operation for VM connected load of half- bridge 3 is disabled 1b = Passive OLD operation for VM connected load of half- bridge 3 is enabled
1	HB2__VM_POLD	R/W	0b	0b = Passive OLD operation for VM connected load of half- bridge 2 is disabled 1b = Passive OLD operation for VM connected load of half- bridge 2 is enabled
0	HB1_VM_POLD	R/W	0b	0b = Passive OLD operation for VM connected load of half- bridge 1 is disabled 1b = Passive OLD operation for VM connected load of half- bridge 1 is enabled

Table 55. Open Load Detect (OLD) Control (OLD_CTRL_6) Register Field Descriptions

APPLICATION AND IMPLEMENTATION

APPLICATION INFORMATION

The PT12493 is primarily used in control of multiple brushed DC motors in HVAC applications. The design procedures in the Typical Application section highlight how to use and configure the device. It also possible utilizes to drive side-mirrors fold (by paralleling the half-bridges to meet the high current requirement), or drives stepping motor for mirror x-y axis direction control and side indicator LED's, or controls air solenoid valve for massage seat.

TYPICAL APPLICATION

DC MOTOR APPLICATION

The PT12493 is primarily used for the control of multiple brushed DC motors which can be connected in independent-type, sequential-type or the parallel-type motor connection as shown in Figure 85.

An automotive battery powers the device to power supply pin (VM). A 3.3-V regulated power supply is generated for the supplying power to the digital core (VDD) of the device. A micro-controller is connected to the PT12493 with the SPI interface (4-lines) for control, configuration and diagnostics. The device operating or sleep state is controlled by the SLEPN pin and FALTN pins is used as an additional hardware diagnostic.

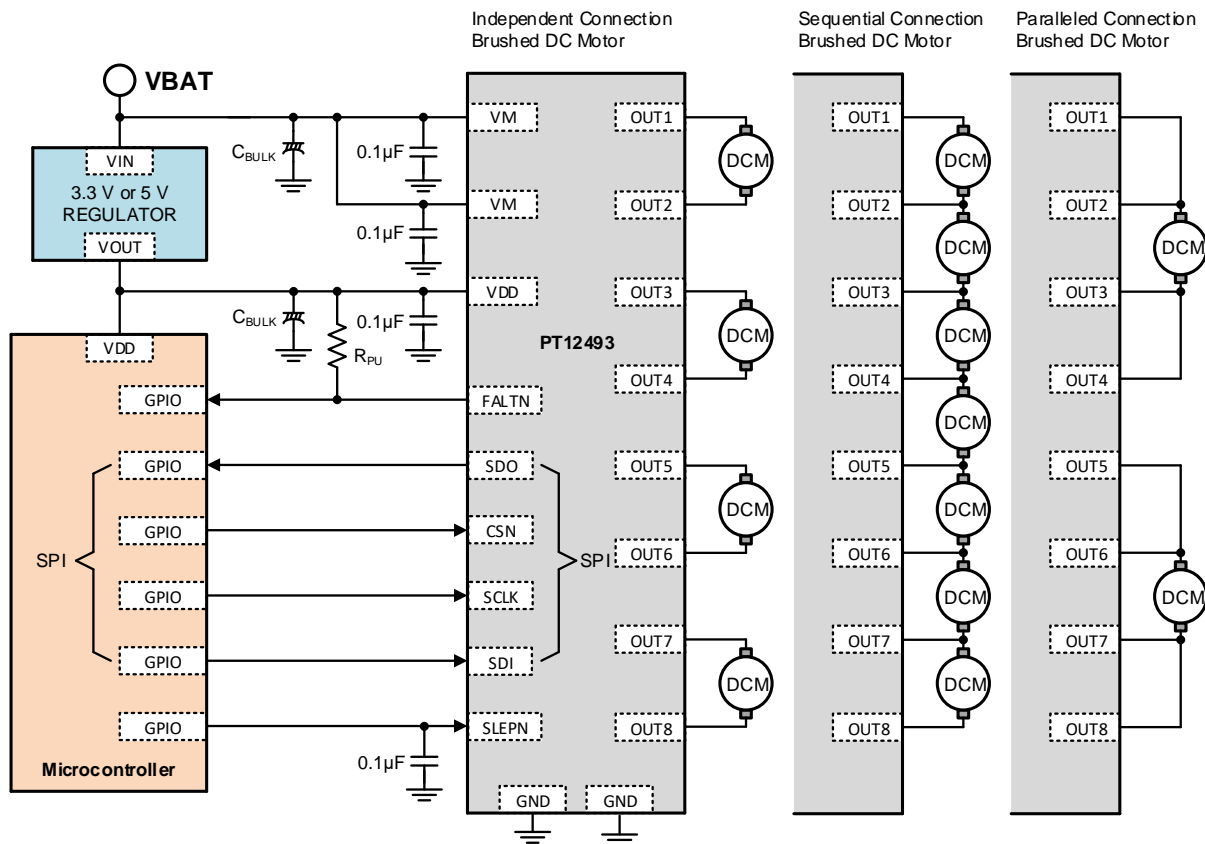


Figure 85. Primary Application Schematic (Automotive HVAC Application)

DESIGN REQUIREMENTS

Table 56 lists example input parameters for the system design.

DESIGN PARAMETERS	REFERENCE	EXAMPLE VALUE
Supply voltage	V _V M	13.5-V
Supply digital voltage	V _V DD	3.3-V
Number of motor connected	N	6 motors
Number of motor operating in normal operation	N _F	4 motors
Number of motor operating in stall condition	N _S	2 motors
Motor RMS current	I _{RMS}	200-mA
Motor peak current	I _{PEAK}	800-mA
Motor resistance	R _{MOTOR}	16.9-Ω
Motor inductance	L _{MOTOR}	10-mH
PWM Frequency	f _{PWM}	2-kHz (Internal)
Rise and fall time for continuous mode (SR = 0)	t _{RISE_CONT} , t _{FALL_CONT}	22.5-μs
Rise and fall time for PWM mode (SR = 1)	t _{RISE_PWM} , t _{FALL_PWM}	5.4-μs

Table 56. Design Parameters

DETAILED DESIGN PROCEDURE

The design procedure includes the selection of motor current rating the power dissipation to meet the desired thermal performance.

MOTOR CURRENT RATING

Motor specification selection is the most importance criteria for the design. Each half-bridge (OUT_x) of the PT12493 device is designed to handle RMS current of 1 A and the peak current is limited by the minimum over-current (OCP) limit of 1.3-A. Therefore, a motor with peak starting current higher than 1.3-A is expected to hit OCP limit. For higher peak current motors (starting current higher than 1.3-A), following methods can be implemented:

Current Chopping: During starting, if supply voltage is connected directly to the motor, then due to low back-emf (when speed is zero or low), a huge peak current is demanded by the motor. This peak current is only limited by the motor's winding resistance (R_{MOTOR}). This peak current of motor can be limited by starting the motor with low-duty PWM switching operation and then gradually increasing (duty-ramping) the duty with speed to 100% PWM operation (equivalent to motor operating in continuous mode). This duty-ramping provides enough time to ramp motor speed and build sufficient back-emf which limits the peak current. The PT12493 device implements a 2-kHz PWM switching operation which is suitable for the HVAC damper motors.

OCP Deglitch Time Adjustments: This method is applicable if the motor inertia is low and the motor can quickly pick up the speed. For this method, the motor starting current should settle to lower than minimum over-current limit (I_{OCP}) before OCP deglitch time (t_{OCP}) is over. The device provides multiple (8 settings) OCP deglitch time settings with a default deglitch time of 10-μs and can be increased to a maximum value of 60-μs.

POWER DISSIPATION

A detailed explanation of the power dissipation of the device is presented in Power Dissipation section.

NOTE

For multiple motor connection, it has to be ensured that the total device current should be lower than the maximum current-carrying capability of the power-supply (VM/GND) pins, i.e. 6-A (maximum).

Information in the following applications sections is not part of the PTC component specification, and PTC does not warrant its accuracy or completeness. Customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

DC MOTOR WITH HALF BRIDGE APPLICATION

The PT12493 can alternatively be used for the mirrors targeting the mirror-fold, mirror x-y direction control and side indicator LED's as shown in Figure 86.

The half-bridges are connected in parallel to support the higher current requirement of the mirror fold application. Whereas, single half-bridges can be used for driving the low-current motors used for the mirror X and Y positioning. Moreover, the LED's used in side indicators, puddle lamp is lower current which can be easily driven by single half-bridges.

The driver is powered by the automotive battery with a 3.3-V regulated power supply generated for the supplying power to the digital pin (VDD). A micro-controller is connected to the PT12493 device with the SPI interface (4-lines) for control, configuration and diagnostics. The device operating or sleep state is controlled by the SLEPN pin and FALTN pins is used as an additional hardware diagnostic.

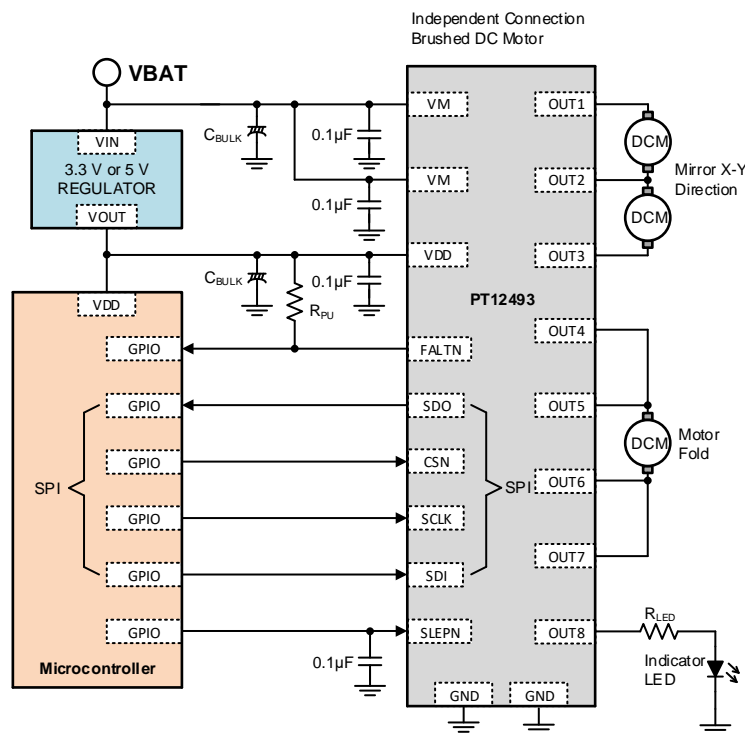


Figure 86. Alternative Application Schematic (Automotive Side-Mirror Application)

DESIGN REQUIREMENTS

Table 57 lists example input parameters for the system design.

DESIGN PARAMETERS	REFERENCE	EXAMPLE VALUE
Supply voltage	V _{VM}	13.5-V
Supply digital voltage	V _{VDD}	3.3-V
Motor RMS current (Mirror Fold Motor)	I _{RMS_FOLD}	1.8-A
Motor peak current (Mirror Fold Motor)	I _{PEAK_FOLD}	3-A
Motor RMS current (X/Y Direction Motor)	I _{RMS_XY}	200-mA
Motor peak current (X/Y Direction Motor)	I _{PEAK_XY}	800-mA
LED Current	I _{LED}	150-mA
PWM Frequency (Motor)	f _{PWM_MOTOR}	2-kHz (Internal)
PWM Frequency (LED)	f _{PWM_LED}	100-Hz (Internal)
Rise and fall time for continuous mode (SR = 0)	t _{RISE_CONT} , t _{FALL_CONT}	22.5-μs
Rise and fall time for PWM mode (SR = 1)	t _{RISE_PWM} , t _{FALL_PWM}	5.4-μs

Table 57. Design Parameters

DETAILED DESIGN PROCEDURE

The key-requirement for this application is the selection of number of half-bridges to operate in parallel for the high current motor (mirror-fold) application. Parallel Mode (Continuous Operation) describes the configuration for half-bridges for enabling the parallel mode operation.

H-BRIDGE REQUIREMENTS FOR PARALLEL OPERATION

The selection of number of half-bridges for connecting in parallel operation to support higher current depends on two parameters as:

1. **Peak / Stall Current:** The mirror-fold motor peak current decides the amount of current flowing through a single half-bridge which has to be lower than the minimum OCP (I_{OCP}) threshold limit. A current limiting approach for limiting the peak current of motor can also be implemented as shown in Motor Current Rating section. This section also explains the application of adjusting the OCP deglitch timing for meeting the desired peak currents.
2. **Thermal:** For meeting the desired thermal performance during the peak current / stall condition, the number of half-bridges is increased to reduce the effective $R_{DS(ON)}$.

For example, as shown in Table 57, six half-bridges can be connected in parallel combination (3 half-bridges for high-side and 3 half-bridges for low-side) to support the 3-A peak current requirement. The power dissipation for this can be calculated in similar way as explained in Thermal Application section.

STEPPING MOTOR APPLICATION

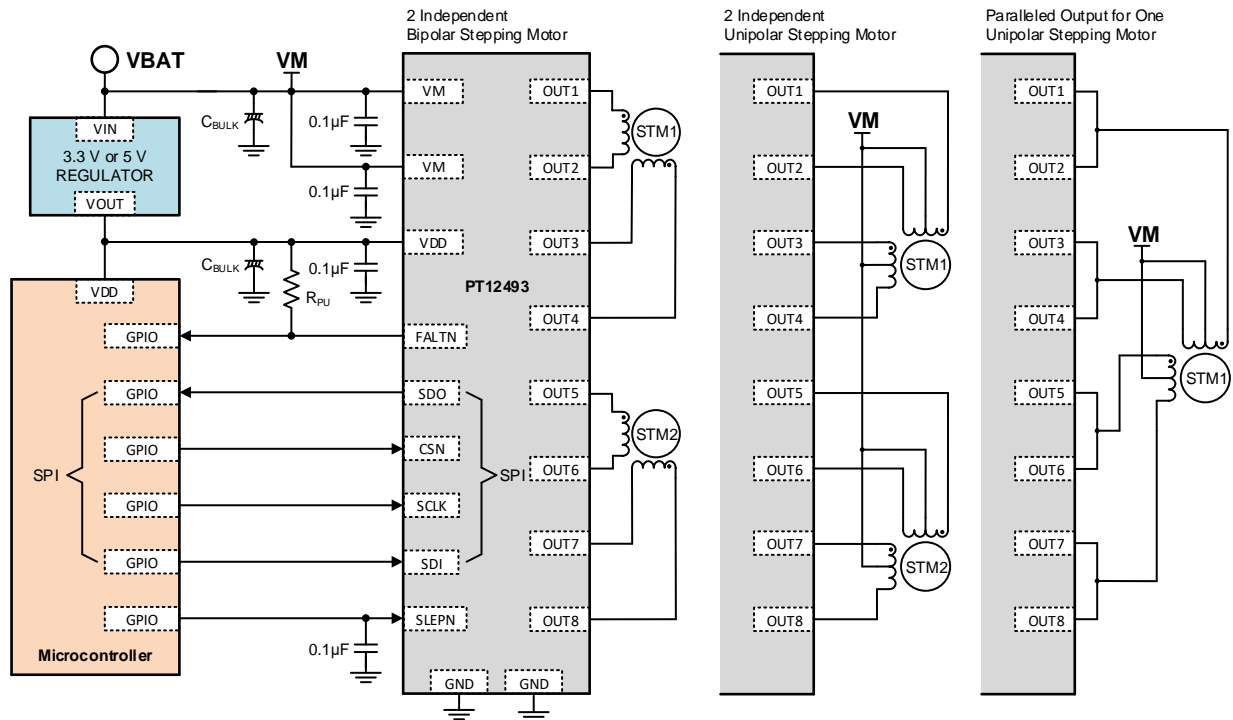


Figure 87. Stepping Motor Application Schematic

SOLENOID APPLICATION

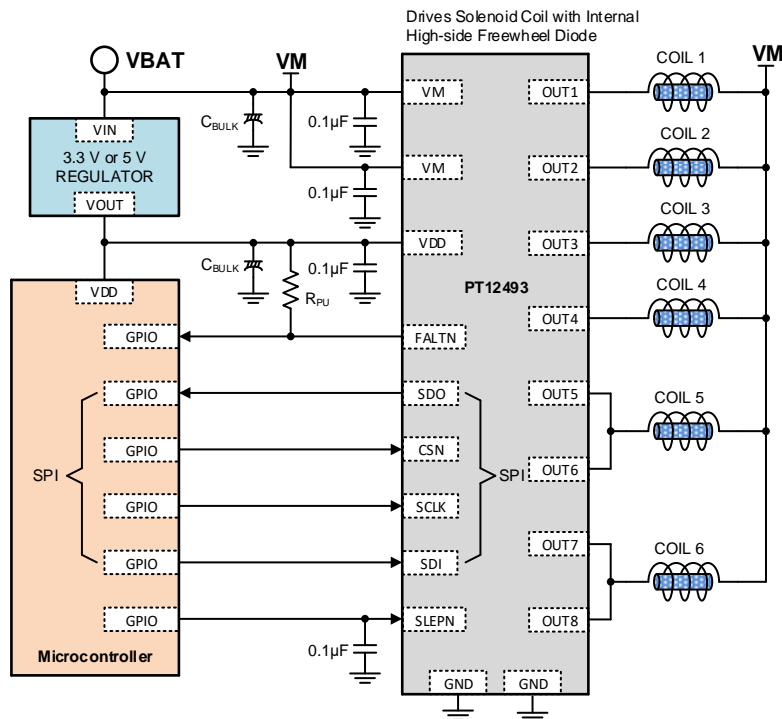


Figure 88. Solenoid Application Schematic

POWER SUPPLY RECOMMENDATIONS

The PT12493 device is designed to operate from an input voltage supply (VM) range from 4.5-V to 32-V. A 0.1- μ F ceramic capacitor rated for VM must be placed as close to the device as possible. In addition, a bulk capacitor must be included on the VM pin but can be shared with the bulk bypass capacitance for the external power MOSFETs.

BULK CAPACITANCE SIZING

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size. The amount of local capacitance depends on a variety of factors including:

- The highest current required by the motor system
- The power supply's type, capacitance, and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable supply voltage ripple
- Type of motor (brushed DC, brushless DC, stepper)
- The motor startup and braking methods

The inductance between the power supply and motor drive system will limit the rate of change of current from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet provides a recommended minimum value, but system level testing is required to determine the appropriate sized bulk capacitor.

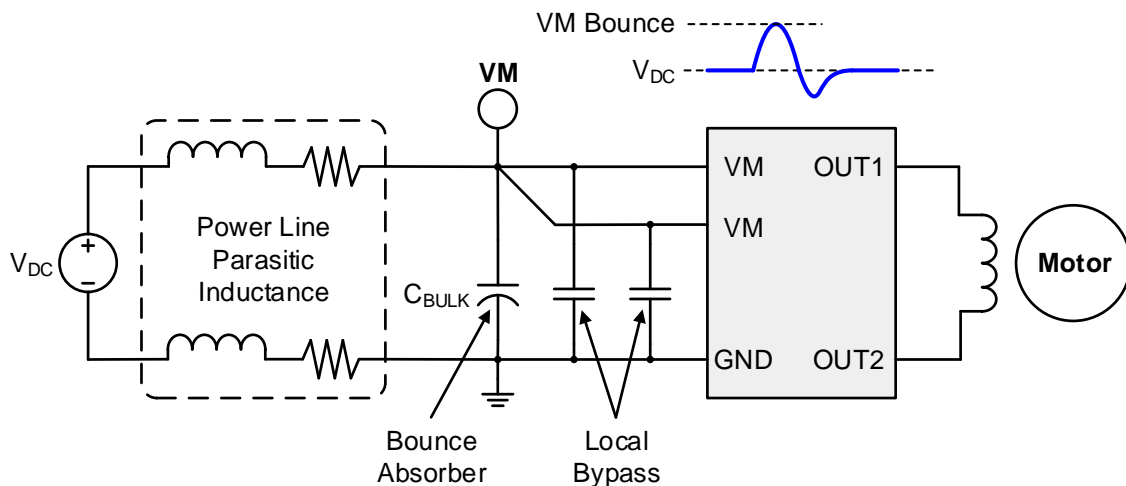


Figure 89. Motor Drive Power Supply Parasitic Example

PCB LAYOUT

LAYOUT GUIDELINES

Bypass the VM pin to the GND pin using a low-ESR ceramic bypass capacitor with a recommended value of 0.1 μ F. Place this capacitor as close to the VM pin as possible with a thick trace or ground plane connected to the PGND pin. Additionally, bypass the VM pin using a bulk capacitor rated for VM. This component can be electrolytic. This capacitance must be at least 10 μ F.

Bypass the VDD pin to the GND pin with a 0.1- μ F low-ESR ceramic capacitor rated for 6.3 V (X5R or

X7R). Place this capacitor as close to the pin as possible and minimize the path from the capacitor to the AGND pin.

LAYOUT EXAMPLE

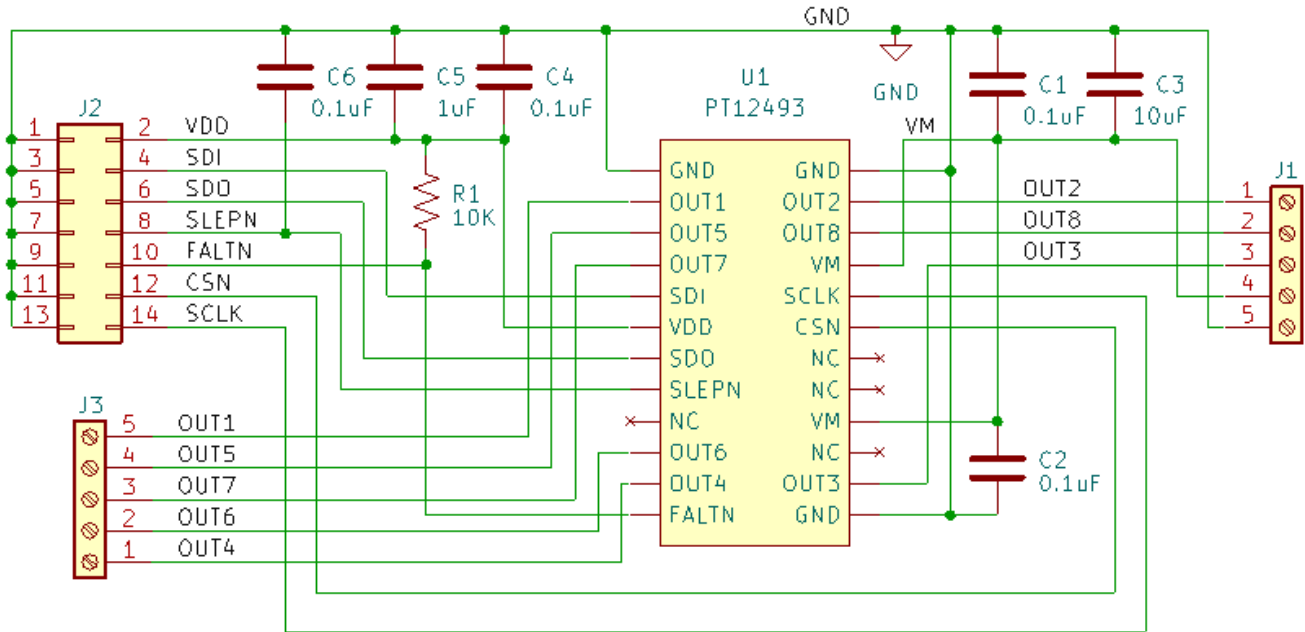


Figure 90. Simplified Schematic for Layout Example

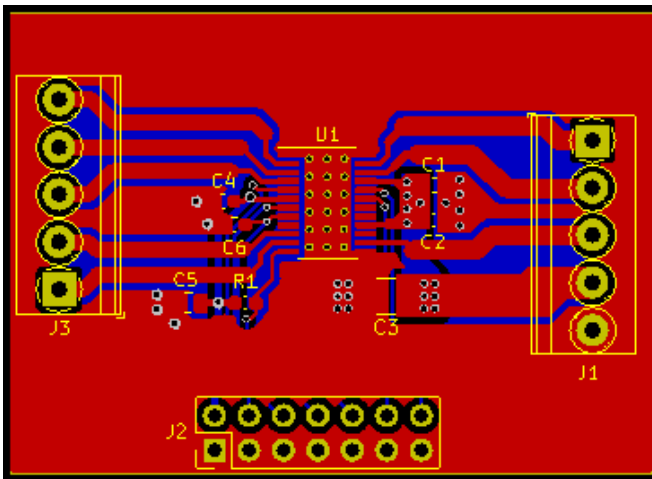


Figure 91. Layout Example, top side

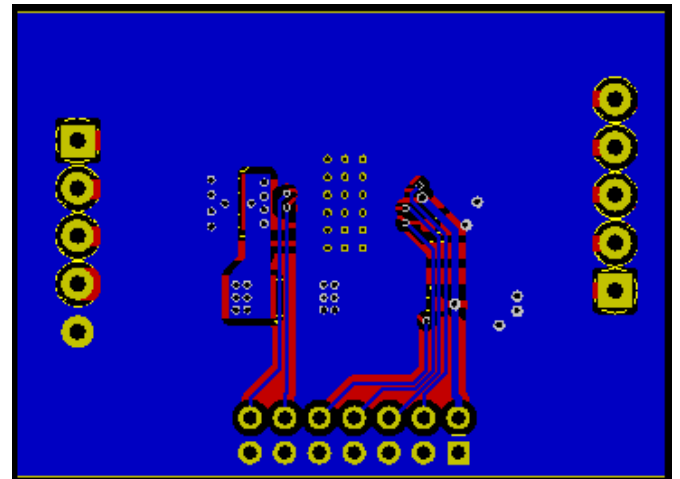


Figure 92. Layout Example, top side

- (1) This example is a two-layer board, both sides should reserve a large area copper plane to enhance power dissipation, the exposed thermal pad of the device must be soldered to the board. The copper plane should connect to ground and not be fragmented for low thermal conductivity.
- (2) The VM power and half bridge outputs path could utilize wide polygon pattern and multiple vias for higher current carrying capability.
- (3) Keeps the SPI routing and half bridge output separate, or minimize their cross area. To prevent the BCI noise from output terminal interference the control signal, add a 0.1µF on the SLEPN near the device is recommended.

THERMAL APPLICATION

This section presents the power dissipation and thermal analysis of PT12493 device applicable for different types of PCB's.

POWER DISSIPATION

The total power dissipation in the PT12493 device constitutes three main components as the power dissipation in full-bridges (P_{DRV}) due to on-state resistance ($R_{DS(ON)}$), power dissipation due to switching losses in FETs (P_{SW}) and power losses due to quiescent current consumption (P_Q).

POWER DISSIPATION DUE TO DEVICE ON-STATE RESISTANCE ($R_{DS(ON)}$)

The current path for a motor connected in full-bridge is through the high-side FET of one half-bridge and low-side FET of other half-bridge. The power dissipation of PT12493 depends on the amount of current flowing through the full-bridge and the number of such full-bridges which are operating together. The power dissipation (P_{FB_CONT}) in a single full-bridge configuration for continuous mode depends on the motor rms current (I_{RMS}) and high-side ($R_{DS(ON)_HS}$) and low-side ($R_{DS(ON)_LS}$) on-state resistance as shown in Equation 1.

$$P_{FB_CONT} = (I_{RMS})^2 \times (R_{DS(ON)_HS} + R_{DS(ON)_LS}) \quad (1)$$

The power dissipation (P_{FB_STALL}) in a single full-bridge configuration for motor is a stall condition depends on the motor peak current (I_{PEAK}) and high-side ($R_{DS(ON)_HS}$) and low-side ($R_{DS(ON)_LS}$) on-state resistance as shown in Equation 2.

$$P_{FB_STALL} = (I_{PEAK})^2 \times (R_{DS(ON)_HS} + R_{DS(ON)_LS}) \quad (2)$$

Now, the power dissipation for operating mode and stall mode in single full-bridge for the typical application as shown in Table 56 is calculated in Equation 3 and Equation 4 respectively.

$$P_{FB_CONT} = (I_{RMS})^2 \times (R_{DS(ON)_HS} + R_{DS(ON)_LS}) = (200\text{-mA})^2 \times (0.75\text{-}\Omega + 0.75\text{-}\Omega) = 60\text{-mW} \quad (3)$$

$$P_{FB_STALL} = (I_{PEAK})^2 \times (R_{DS(ON)_HS} + R_{DS(ON)_LS}) = (800\text{-mA})^2 \times (0.75\text{-}\Omega + 0.75\text{-}\Omega) = 960\text{-mW} \quad (4)$$

For N_F -full bridges in operating condition and N_S -full bridges in stall condition, the total driver power (P_{DRV}) is expressed and calculated as shown in Equation 5.

$$P_{DRV} = N_F \times P_{FB_CONT} + N_S \times P_{FB_STALL} = 4 \times 60\text{-mW} + 2 \times 960\text{-mW} = 2.16\text{-W} \quad (5)$$

NOTE

This power calculation is highly dependent on the device temperature which significantly effects the high-side and low-side $R_{DS(ON)}$ of the FETs. For more accurate calculation, consider the dependency of $R_{DS(ON)}$ of FETs with device temperature.

POWER DISSIPATION DUE TO SWITCHING LOSSES

The power loss due to the PWM switching frequency depends on the slew rates (rise-time, t_{RISE_PWM} , and fall-time, t_{FALL_PWM}), supply voltage (V_{VM}), motor RMS current (I_{RMS}) and the PWM switching frequency (f_{PWM}). Considering a case, where the PWM switching is only applicable for single half-bridge in a full-bridge configuration (see Free-Wheeling Mode (Synchronous Rectification) Disable / Enable), therefore only half of the half-bridges are operating in PWM switching. Hence, the switching losses during rise-time and fall-time is calculated as shown in Equation 6 and Equation 7.

$$P_{SW_RISE} = (N_F/2) \times 0.5 \times V_{VM} \times I_{RMS} \times t_{RISE_PWM} \times f_{PWM} \quad (6)$$

$$P_{SW_FALL} = (N_F/2) \times 0.5 \times V_{VM} \times I_{RMS} \times t_{FALL_PWM} \times f_{PWM} \quad (7)$$

Putting various parameters from Table 56 in Equation 6 and Equation 7, the rise-time (P_{SW_RISE}) and fall-time (P_{SW_FALL}) switching losses are calculated as shown in Equation 8 and Equation 9 as,

$$P_{SW_RISE} = (N_f/2) \times 0.5 \times V_{VM} \times I_{RMS} \times t_{RISE_PWM} \times f_{PWM} = (4/2) \times 0.5 \times 13.5\text{-V} \times 200\text{-mA} \times 9\text{-}\mu\text{s} \times 2\text{-kHz} = 48.6\text{-mW} \quad (8)$$

$$P_{SW_FALL} = (N_f/2) \times 0.5 \times V_{VM} \times I_{RMS} \times t_{FALL_PWM} \times f_{PWM} = (4/2) \times 0.5 \times 13.5\text{-V} \times 200\text{-mA} \times 9\text{-}\mu\text{s} \times 2\text{-kHz} = 48.6\text{-mW} \quad (9)$$

Hence, the total switching power (P_{SW}) is calculated as the sum of rise-time (P_{SW_RISE}) switching losses and fall-time (P_{SW_FALL}) switching losses as shown in Equation 10

$$P_{SW} = P_{SW_RISE} + P_{SW_FALL} = 48.6\text{-mW} + 48.6\text{-mW} = 97.2\text{-mW} \quad (10)$$

NOTE

The rise-time (t_{RISE}) and the fall-time (t_{FALL}) are calculated based on typical values of the slew rate (SR) from Specifications. This parameter is intended to change based on the supply-voltage, temperature and device to device variation.

POWER DISSIPATION DUE TO QUIESCENT CURRENT

The power dissipation due to the quiescent current taken by the power supply (P_{VM}) and the digital supply (P_{VDD}) depends on the applied voltage (V_{VM} and V_{VDD}) and operating mode currents (I_{VM} and I_{VDD}) and are calculated as shown in Equation 11 and Equation 12 respectively.

$$P_{VM} = V_{VM} \times I_{VM} \quad (11)$$

$$P_{VDD} = V_{VDD} \times I_{VDD} \quad (12)$$

Putting various parameters from Table 56 in Equation 11 and Equation 12, the power-supply (P_{VM}) and digital-supply (P_{SW_FALL}) quiescent power losses are calculated as shown in Equation 13 and Equation 14 as,

$$P_{VM} = V_{VM} \times I_{VM} = 13.5\text{-V} \times 3\text{-mA} = 40.5\text{-mW} \quad (13)$$

$$P_{VDD} = V_{VDD} \times I_{VDD} = 3.3\text{-V} \times 3\text{-mA} = 9\text{-mW} \quad (14)$$

The total quiescent power loss (P_Q) is calculated as the sum of quiescent power loss due to VM and VDD as shown in Equation 15 as,

$$P_Q = P_{VM} + P_{VDD} = 40.5\text{-mW} + 9.9\text{-mW} = 50.4\text{-mW} \quad (15)$$

NOTE

The quiescent power is calculated using the typical operating current (I_{VM} and I_{VDD}) which is dependent on supply-voltage, temperature and device to device variation.

TOTAL POWER DISSIPATION

The total power dissipation (P_{TOT}) is calculated as the sum of the power dissipation in full-bridges (P_{DRV}), power dissipation due to switching losses in FET's (P_{SW}) and power losses due to quiescent current consumption (P_Q) as shown in Equation 16.

$$P_{TOT} = P_{DRV} + P_{SW} + P_Q \quad (16)$$

Now, by putting values of P_{DRV} , P_{SW} and P_Q from Equation 5, Equation 10 and Equation 15 in Equation 16, the total power dissipation (P_{TOT}) is calculated as shown in Equation 17.

$$P_{TOT} = P_{DRV} + P_{SW} + P_Q = 2.16\text{-W} + 97.2\text{-mW} + 50.4\text{-mW} = 2.3076\text{-W} \quad (17)$$

THERMAL PARAMETERS

The variation of thermal parameters such as the $R_{\theta JA}$ (Junction-to-Ambient Thermal Resistance) and Ψ_{JB} (Junction-to-Board Characterization Parameter) is highly dependent on the PCB type, copper thickness and the copper pad area.

NOTE

The thermal parameters ($R_{\theta JA}$ (Junction-to-Ambient Thermal Resistance) and Ψ_{JB} (Junction-to-Board Characterization Parameter)) are calculated considering the ambient temperature of 25°C and with 1.5-W power evenly dissipated between high-side and low-side FET's. The thermal parameters calculated considering the power dissipation at the actual location of the power-FETs rather than an averaged estimation. The thermal parameters are highly dependent on the external conditions such as altitude, package geometry etc.

DEVICE JUNCTION TEMPERATURE ESTIMATION

The device junction temperature (T_J) is calculated by the power dissipation and the thermal parameters (Junction-to-Ambient Thermal Resistance ($R_{\theta JA}$)) for the particular PCB. For an ambient temperature of T_A and total power dissipation (P_{TOT}), the junction temperature (T_J) is calculated as shown in Equation 18.

$$T_J = T_A + (P_{TOT} \times R_{\theta JA}) \quad (18)$$

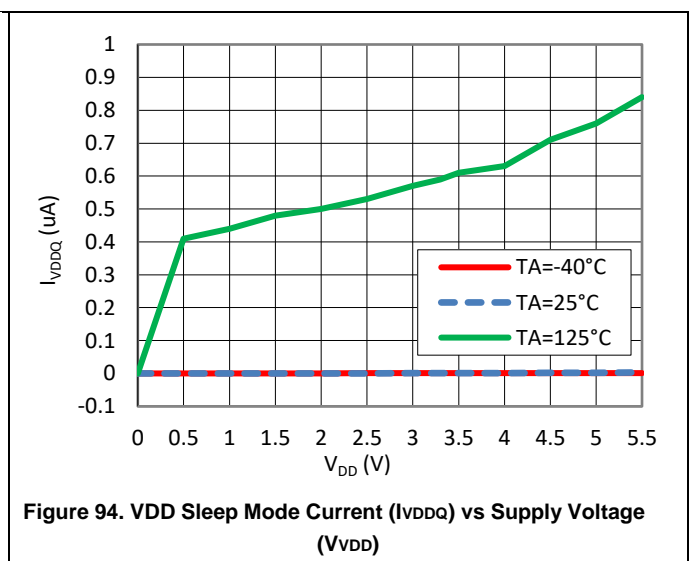
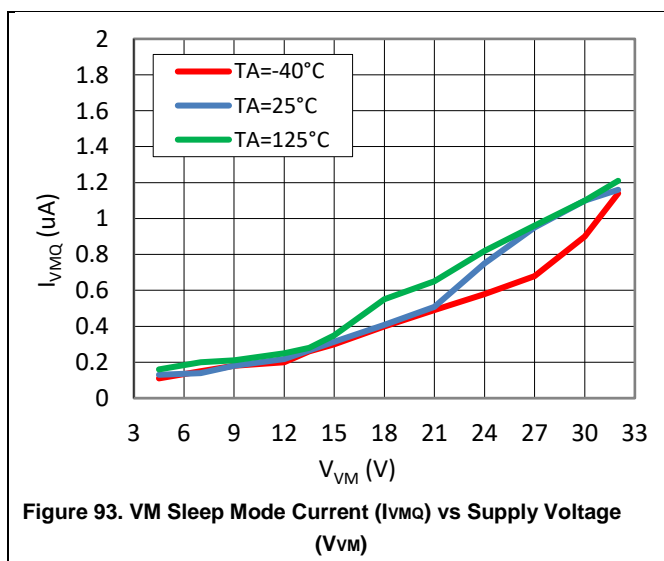
Considering a 4-layer PCB, with copper thickness as 2-oz and copper-pad area as 16-cm², the junction-to-ambient thermal resistance ($R_{\theta JA}$) can be estimate as 22°C/W.

By putting the value of total power dissipation (P_{TOT}) from Equation 17 in Equation 18 and taking ambient temperature (T_A) as 25°C, the junction temperature is calculated as shown in Equation 19.

$$T_J = T_A + (P_{TOT} \times R_{\theta JA}) = 25^\circ\text{C} + (2.3076\text{-W} \times 22^\circ\text{C/W}) = 75.77^\circ\text{C} \quad (19)$$

Hence, the power dissipation of 2.3076-W in the PT12493 device causes the junction temperature (T_J) to increase to 75.77°C. This junction temperature has a margin of 74.23°C before hitting the thermal shutdown limit.

PERFORMANCE CHARTS



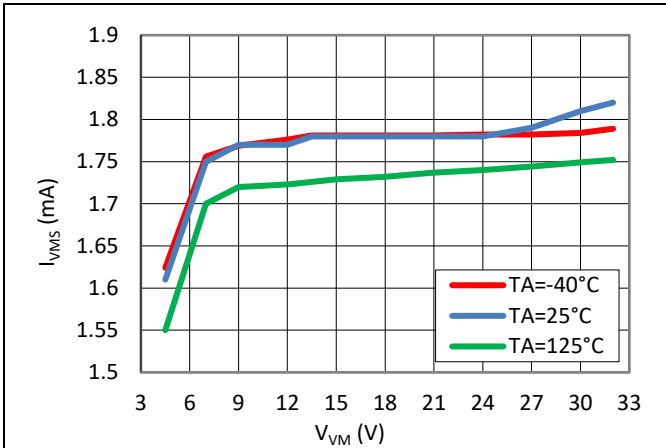


Figure 95. VM Standby Mode Current (I_{VMS}) vs Supply Voltage (V_{VM})

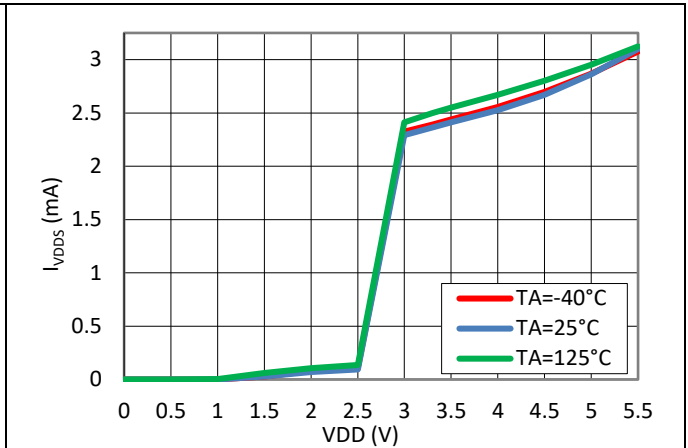


Figure 96. VDD Standby Mode Current (I_{VDDS}) vs Supply Voltage (V_{VDD})

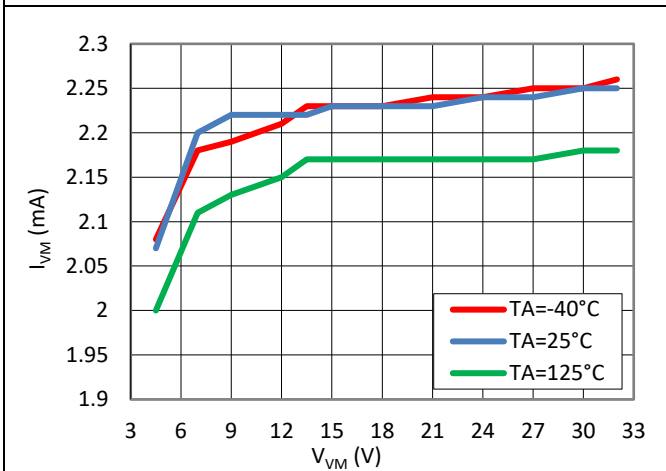


Figure 97. VM Operating Mode Current (I_{VM}) vs Supply Voltage (V_{VM})

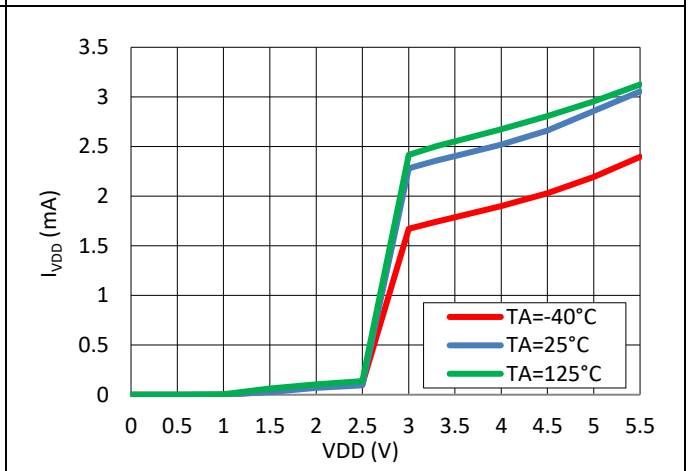


Figure 98. VDD Operating Mode Current (I_{VDD}) vs Supply Voltage (V_{VDD})

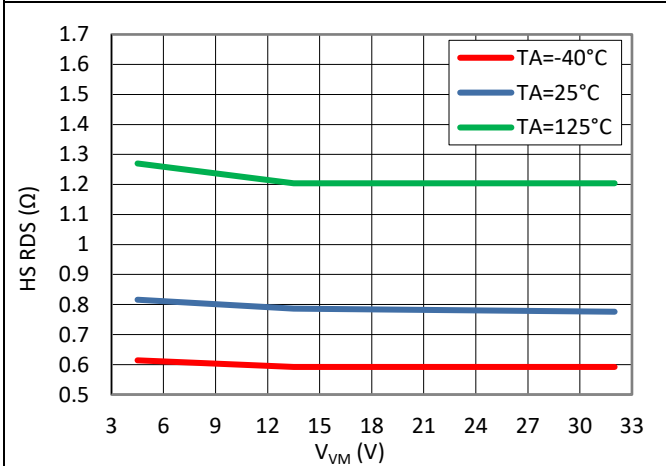


Figure 99. High Side On-State Resistance (R_{DS(ON)}) vs Supply Voltage (V_{VM})

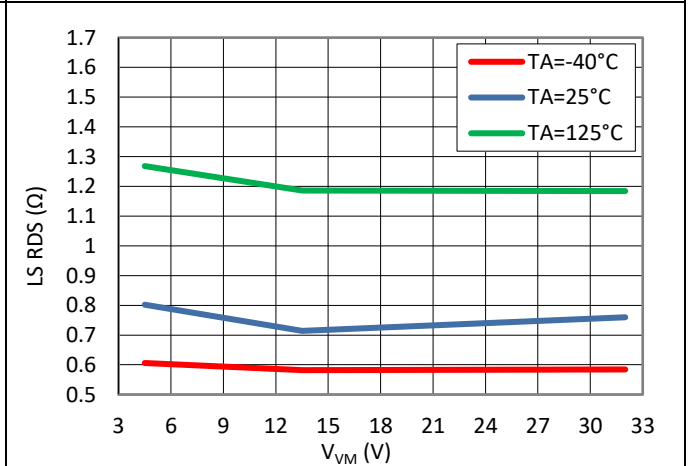


Figure 100. Low-Side On-State Resistance (R_{DS(ON)}) vs Supply Voltage (V_{VM})

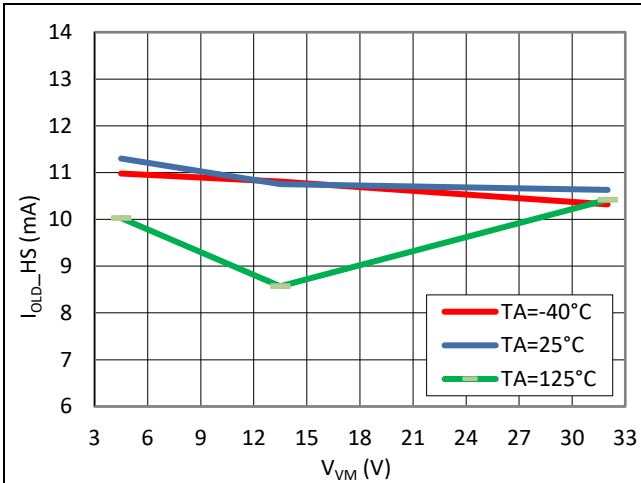


Figure 101. High-Side Open-Load Detection Current (I_{OL_D}) vs Supply Voltage (V_{VM})

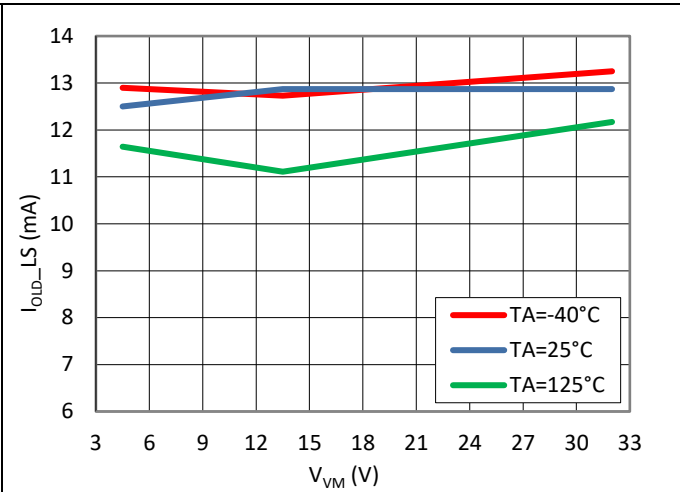


Figure 102. Low-Side Open-Load Detection Current (I_{OL_D}) vs Supply Voltage (V_{VM})

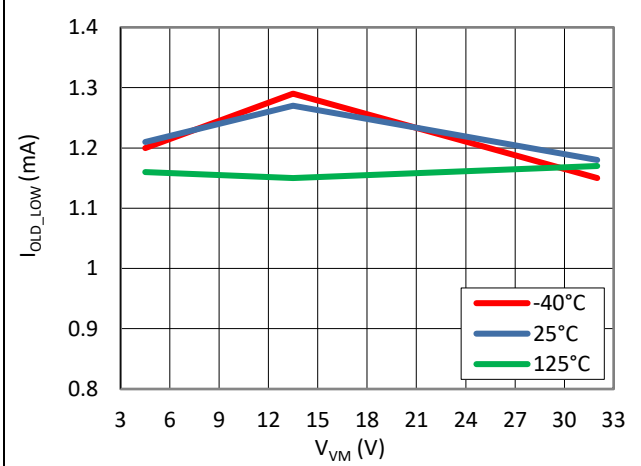


Figure 103. Low open-load detection current (I_{OL_D_LOW}) vs supply voltage (V_{VM})

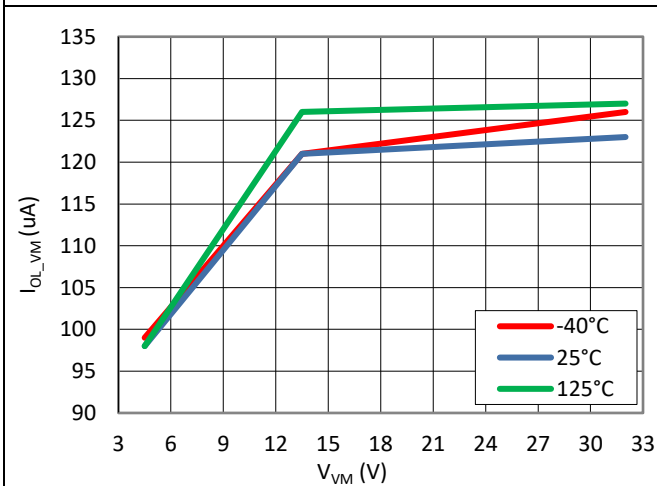


Figure 104. Open-load pull-down current (I_{OL_VM}) when HBX_VM_POLD = 0b vs supply voltage (V_{VM})

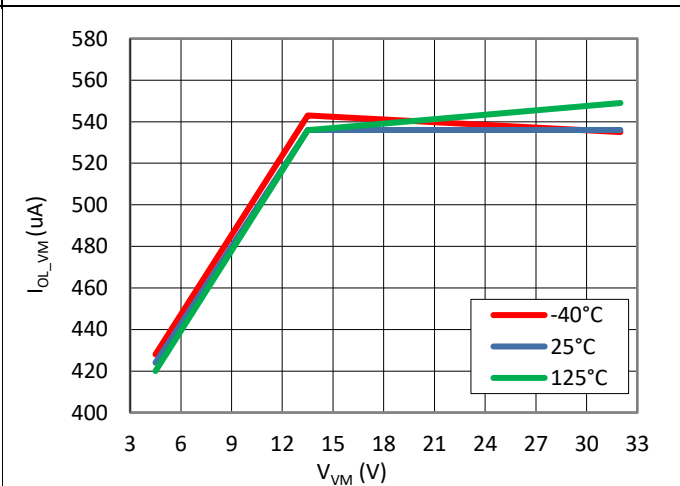


Figure 105. Open-load pull-down current (I_{OL_VM}) when HBX_VM_POLD = 1b vs supply voltage (V_{VM})

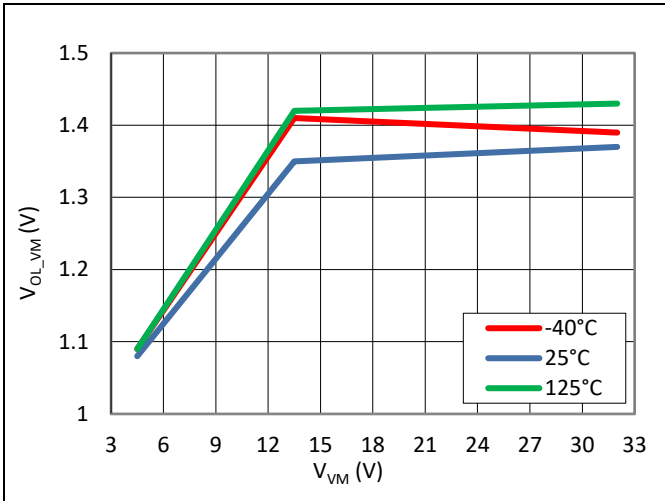


Figure 106. Open-load low-side threshold voltage (V_{OL_VM}) when $HBX_VM_POLD = 0b$ vs supply voltage (V_{VM})

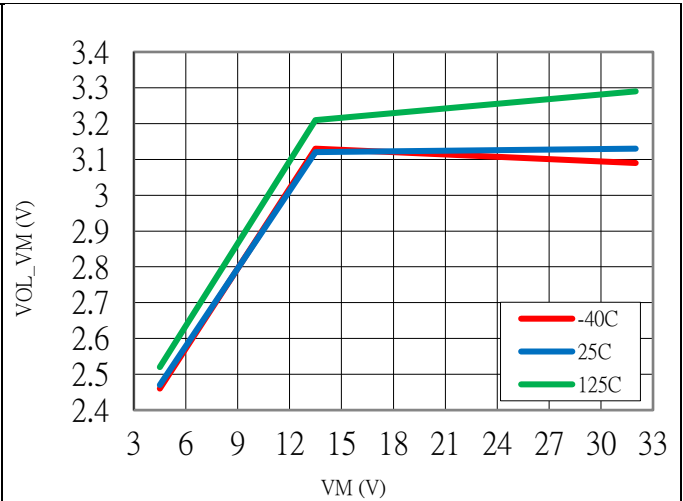


Figure 107. Open-load low-side threshold voltage (V_{OL_VM}) when $HBX_VM_POLD = 1b$ vs supply voltage (V_{VM})

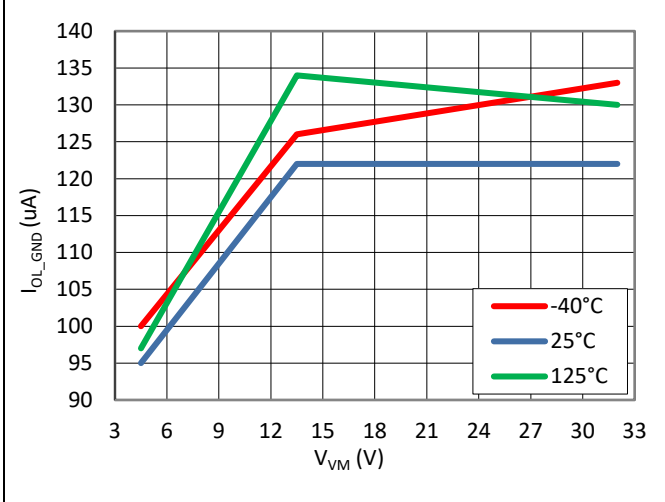


Figure 108. Open-load pull-up current (I_{OL_GND}) vs supply voltage (V_{VM})

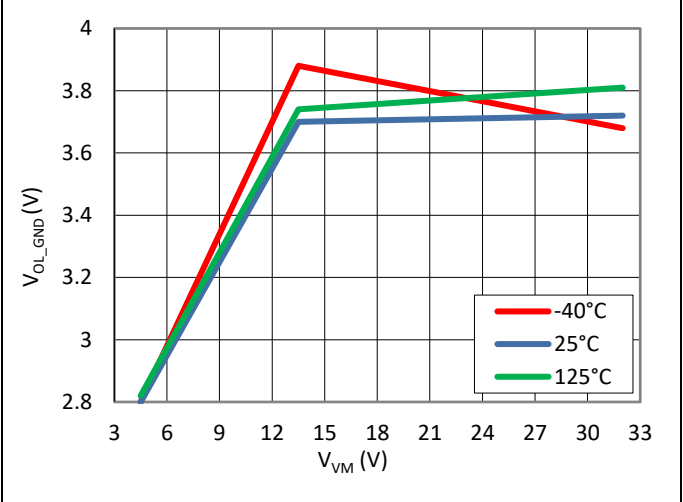


Figure 109. Open-load low-side threshold voltage (V_{OL_GND}) vs supply voltage (V_{VM})

ABSOLUTE MAXIMUM RATINGS

over operating ambient temperature range (unless otherwise noted) ⁽¹⁾

Parameters	Symbol	Min.	Max.	Unit
Power supply pin voltage (VM)	V _M	-0.3	40	V
Logic supply pin voltage (VDD)	V _{DD}	-0.3	6	V
Output pin voltage (OUTx)	V _{OUTx}	-0.7	V _{IN} +0.7	V
Logic pin input voltage (CSN, SLEPN, SCLK, SDI)	V _{DI}	-0.3	V _{DD} +0.3	V
Logic pin output voltage (FALTN, SDO)	V _{DO}	-0.3	V _{DD} +0.3	V
Continuous supply current (VM pins combined)	I _{VM}	0	6	A
Continuous sink current (GND pins combined)	I _{GND}	0	6	A
Peak output current drive (OUTx)	I _{OUT_PK}	Internal Limited	Internal Limited	A
Junction temperature	T _J	-40	150	°C
Storage temperature	T _{STG}	-40	150	°C

Operating a device beyond its Absolute Maximum Ratings may cause permanent damage. These limits do not guarantee proper function or performance. Even short-term operation within Absolute Maximum Ratings but outside the Recommended Operating Conditions may lead to malfunction, reduced reliability, or shortened lifespan.

(1) Stresses beyond those listed under Absolute Maximum Rating may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Condition. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ESD RATINGS

Parameters	Symbol	Target Pins	VALUE	Unit
Human body model (HBM)	V_{HBM}	All pins	±2000	V
Charge device model (CDM)	V_{CDM}	Corner pins	±750	
		Other pins	±500	

RECOMMENDED OPERATION CONDITIONS

Parameters	Symbol	Min.	Max.	Unit
Power supply voltage (VM)	V_M	4.5	32	V
Logic supply voltage (VDD)	V_{DD}	3	5.5	V
Logic input voltage (CSN, SLEPN, SCLK, SDI)	V_{IN}	0	5.5	V
Open drain pull-up voltage (FALTN)	V_{OD}	0	5.5	V
Open drain output current (FALTN)	I_{OD}	0	5	mA
Push-pull pull-up voltage (SDO)	V_{OP}	0	5.5	V
Push-pull output current (SDO)	I_{OP}	0	5	mA
Operating ambient temperature	T_A	-40	125	°C
Operating junction temperature	T_J	-40	150	°C

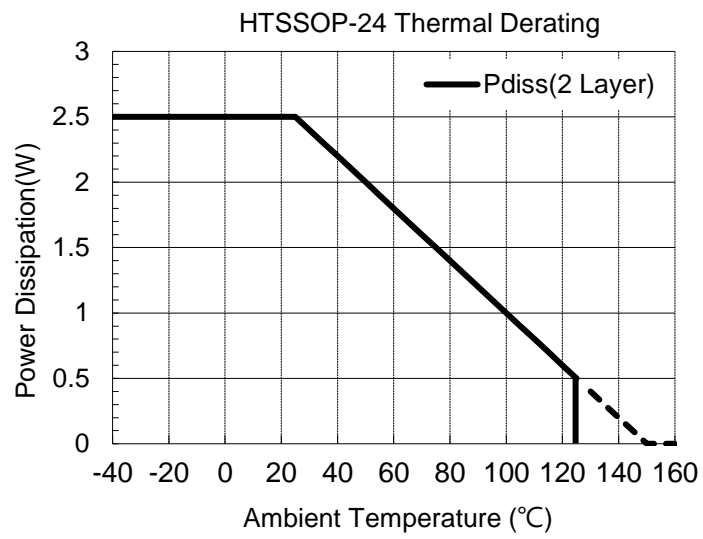
Operation between Recommended Operating Conditions and Absolute Maximum Ratings for extended periods cannot guarantee long-term reliability or normal functionality.

PACKAGE THERMAL CHARACTERISTIC

Parameters	Symbol	Condition	Typ	Unit
Junction-to-ambient thermal resistance	Rja	(Note 1)	50	°C/W
Junction-to-board thermal resistance	Rjb		12	°C/W
Package thermal resistance, from junction to thermal pad	Rjtp	(Note 2)*	3.1	°C/W

Note 1: The thermal resistance of HTSSOP-24 pin package measured on specified PCB: dimension=70mm x 80mm, FR-4, 2 layers board, thickness=1.6mm, copper thickness=1oz (35μm), GND plane metal coverage=50%, still airflow.

Note 2: The thermal via under the thermal pad: 12 holes, drill diameter=0.3mm, all connect to the GND plane on the bottom side.



ELECTRICAL CHARACTERISTICS

 Typical value at $T_A=25^{\circ}\text{C}$, $V_M=13.5\text{V}$, $V_{DD}=3.3\text{V}$.

 All other values at $T_J=-40^{\circ}\text{C}$ to 150°C , $V_M=4.5$ to 32V , $V_{DD}=3$ to 5.5V (unless otherwise noted)

Parameters	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Supply (V_M, V_{DD})						
VM sleep mode current	I_{VMQ}	$V_M = 13.5\text{V}$, SLEPN = 0, $T_A = 25^{\circ}\text{C}$		0.3	1.5	μA
		$V_M = 13.5\text{V}$, SLEPN = 0, $T_A = 125^{\circ}\text{C}$			2	μA
VDD sleep mode current	I_{VDDQ}	$V_M = 13.5\text{V}$, $V_{DD} = 3.3\text{V}$, SLEPN = 0, $T_A = 25^{\circ}\text{C}$		0.01	0.5	μA
		$V_M = 13.5\text{V}$, $V_{DD} = 3.3\text{V}$, SLEPN = 0, $T_A = 125^{\circ}\text{C}$			2	μA
VM standby mode current	I_{VMS}	$V_M = 13.5\text{V}$, SLEPN = 1, Driver = 'OFF', $T_A = 25^{\circ}\text{C}$		1.8	2	mA
		$V_M = 13.5\text{V}$, SLEPN = 1, Driver = 'OFF', $T_A = 125^{\circ}\text{C}$			2	mA
VDD standby mode current	I_{VDDS}	$V_M = 13.5\text{V}$, $V_{DD} = 3.3\text{V}$, SLEPN = 1, SPI = 'OFF', $T_A = 25^{\circ}\text{C}$		2.4	3	mA
		$V_M = 13.5\text{V}$, $V_{DD} = 3.3\text{V}$, SLEPN = 1, SPI = 'OFF', $T_A = 125^{\circ}\text{C}$			3	mA
VM operating mode current	I_{VM}	$V_M = 13.5\text{V}$, SLEPN = 1, All High-Side FETs = 'ON', $T_A = 25^{\circ}\text{C}$		2.2	5	mA
		$V_M = 13.5\text{V}$, SLEPN = 1, All High-Side FETs = 'ON', $T_A = 125^{\circ}\text{C}$			5	mA
VDD operating mode current	I_{VDD}	$V_M = 13.5\text{V}$, $V_{DD} = 3.3\text{V}$, SLEPN = 1, All High-Side FETs = 'ON', SPI = 'ON' (5 MHz), $T_A = 25^{\circ}\text{C}$		2.5	5	mA
		$V_M = 13.5\text{V}$, $V_{DD} = 3.3\text{V}$, SLEPN = 1, All High-Side FETs = 'ON', SPI = 'ON' (5 MHz), $T_A = 125^{\circ}\text{C}$			5	mA
Wake-up time	t_{WAKE}	SLEPN high to SPI ready			200	μs
Turnoff time	t_{SLEEP}	SLEPN low to device sleep			20	μs
LOGIC-LEVEL INPUTS (SLEPN, SCLK, SDI)						
Input logic low voltage	V_{IL}		0		0.3x	V_{DD}
Input logic high voltage	V_{IH}		0.7x		1x	V_{DD}
Input logic hysteresis	V_{HYS}		200			mV
Input logic low current	I_{IL}	$V_{IN} = 0\text{V}$	-1		1	μA
Input logic high current	I_{IH}	$V_{IN} = V_{DD}$		30	75	μA
Input capacitance	C_{ID}				15	pF
LOGIC-LEVEL INPUTS (CSN)						
Input logic low voltage	V_{IL}		0		0.3x	V_{DD}
Input logic high voltage	V_{IH}		0.7x		1x	V_{DD}
Input logic hysteresis	V_{HYS}		200			mV
Input logic low current	I_{IL}	$V_{IN} = 0\text{V}$		30	75	μA
Input logic high current	I_{IH}	$V_{IN} = V_{DD}$	-1		1	μA
Input capacitance	C_{ID}				15	pF
OPEN-DRAIN OUTPUTS (FALTN)						
Output logic low voltage	V_{OL}	$I_{OD} = 5\text{mA}$	0		0.4	V
Output logic high current	I_{OH}	$V_{OD} = 5\text{V}$	-1		1	μA
Output capacitance	C_{OD}				15	pF

Parameters	Symbol	Test Conditions	Min	Typ	Max	Unit
PUSH-PULL OUTPUTS (SDO)						
Output logic low voltage	V_{OL}	$I_{OP} = 5 \text{ mA}$	0		0.4	V
Output logic high voltage	V_{OH}	$I_{OP} = 5 \text{ mA}$	$V_{DD} - 0.6$		V_{DD}	V
Output logic low current	I_{OL}	$V_{OP} = 0 \text{ V}$	-1		1	μA
Output logic high current	I_{OH}	$V_{OP} = V_{DD}$	-1		1	μA
Output capacitance	C_{OD}				30	pF
DRIVER OUTPUTS (OUTx)						
High-side MOSFET on resistance	$R_{DS(ON)}$	$V_M = 13.5 \text{ V}, I_{OUT} = 0.5 \text{ A}, T_A = 25^\circ\text{C}$		0.75	1.1	Ω
		$V_M = 13.5 \text{ V}, I_{OUT} = 0.5 \text{ A}, T_A = 125^\circ\text{C}$			1.5	Ω
Low-side MOSFET on resistance		$V_M = 13.5 \text{ V}, I_{OUT} = 0.5 \text{ A}, T_A = 25^\circ\text{C}$	0.75	1.1	Ω	
		$V_M = 13.5 \text{ V}, I_{OUT} = 0.5 \text{ A}, T_A = 125^\circ\text{C}$			1.5	Ω
Output rise and fall time (high-side and low-side)	SR	$V_M = 13.5 \text{ V}, 10\text{-}90\%, R_{LOAD} = 47 \Omega, \text{HBx_SR} = 0\text{b}$		0.6		V/ μs
		$V_M = 13.5 \text{ V}, 10\text{-}90\%, R_{LOAD} = 47 \Omega, \text{HBx_SR} = 1\text{b}$		2.5		V/ μs
Output dead time (high to low / low to high)	t_{DEAD}	$V_M = 13.5 \text{ V}, \text{SR} = 0, \text{HS/LS driver OFF to LS/HS driver ON}$	8	20	32	μs
		$V_M = 13.5 \text{ V}, \text{SR} = 1, \text{HS/LS driver OFF to LS/HS driver ON}$	2	7.5	15	μs
Propagation delay (high-side / low-side ON/OFF)	t_{PD}	High-side ON or low-side ON command (SPI last transition) to OUTx transition from Hi-Z state, SR = 0	5	10	25	μs
		High-side ON or low-side ON command (SPI last transition) to OUTx transition from Hi-Z state, SR = 1	2	3	10	μs
Leakage current low-side	I_{LEAK}	$V_{OUTx} = 13.5 \text{ V}, \text{SLEPN} = 1, \text{SR} = 0\text{b}$		7	10	μA
		$V_{OUTx} = 13.5 \text{ V}, \text{SLEPN} = 1, \text{SR} = 1\text{b}$		22	35	μA
		$V_{OUTx} = 13.5 \text{ V}, \text{SLEPN} = 0$		4	15	μA
Leakage current high-side		$V_{OUTx} = 0 \text{ V}, \text{SLEPN} = 1$			2	μA
		$V_{OUTx} = 0 \text{ V}, \text{SLEPN} = 0$			2	μA
PWM MODE						
PWM switching frequency	f_{PWM}	PWM_CHx_FREQ = 00b	56	80	104	Hz
		PWM_CHx_FREQ = 01b	70	100	130	Hz
		PWM_CHx_FREQ = 10b	140	200	260	Hz
		PWM_CHx_FREQ = 11b	1400	2000	2600	Hz
PROTECTION CIRCUITS						
Supply under voltage lockout (UVLO)	V_{UVLO}	Supply rising	4.0		4.5	V
		Supply falling	3.8		4.3	V
Supply under voltage lockout hysteresis	V_{UVLO_HYS}	Rising to falling threshold		200		mV
Supply under voltage deglitch time	t_{UVLO}			10		μs
Supply overvoltage protection (OVP)	V_{OVP}	Supply rising, EXT_OVP = 0b	22		25	V
		Supply falling, EXT_OVP = 0b	20		24	V
		Supply rising, EXT_OVP = 1b	35		37	V
		Supply falling, EXT_OVP = 1b	32		34.3	V
Supply overvoltage protection hysteresis	V_{OVP_HYS}	Rising to falling threshold, EXT_OVP = 0b		1		V
		Rising to falling threshold, EXT_OVP = 1b		0.7		V
Supply overvoltage deglitch time	t_{OVP}			10		μs

Parameters	Symbol	Test Conditions	Min	Typ	Max	Unit
Logic under voltage (POR)	V_{POR}	Supply rising	2.45		3	V
		Supply falling	2.4		2.95	V
Logic under voltage hysteresis	V_{POR_HYS}	Rising to falling threshold		75		mV
Overcurrent protection trip point (1)(2)	I_{OCP}		1.3	1.8	2.3	A
(1) For $20\text{-V} < V_{VM} < 28\text{-V}$, the OCP deglitch time must be limited to 10- μs (Default Deglitch Value, OCP_DEG = 000b). (2) For $V_{VM} > 28\text{ V}$, the OCP deglitch time must be limited to 1- μs (Lowest Deglitch Value, OCP_DEG = 011b).						
Overcurrent protection deglitch time	t_{OCP}	OCP_DEG = 000b	6	10	14	μs
		OCP_DEG = 001b	2.6	5	7.9	μs
		OCP_DEG = 010b	0.4	2.5	5.9	μs
		OCP_DEG = 011b	0.1	1	3.4	μs
		OCP_DEG = 100b	38.2	60	76.6	μs
		OCP_DEG = 101b	23.1	40	51.9	μs
		OCP_DEG = 110b	18.5	30	41.5	μs
		OCP_DEG = 111b	8.4	20	31.6	μs
Open load detection current	I_{OLD}	Current flowing from VM to OUTx (High-Side = ON) or OUTx to GND (Low-Side = ON)	2	10	18	mA
Negative open load detection current	I_{OLD_NEG}	Current flowing from OUTx to VM (High-Side = ON) or GND to OUTx (Low-Side = ON)	2	15	30	mA
Open load detection current in low current OLD mode	I_{OLD_LOW}	Current flowing from VM to OUTx (High-Side = ON) or OUTx to GND (Low-Side = ON)	0.2	1.2	2	mA
Passive OLD current	I_{OL_GND}	MOSFETs in Hi-Z state, current from OUTx to GND during OLD trip		113		μA
Passive OLD voltage threshold	V_{OL_GND}	MOSFETs in Hi-Z state, voltage at OUTx during OLD trip for GND-connected load		3.3		V
Passive OLD current	I_{OL_VM}	MOSFETs in Hi-Z state, current from VM to OUTx for OLD trip, HBX_VM_POLD = 0b		118		μA
Passive OLD voltage threshold	V_{OL_VM}	MOSFETs in Hi-Z state, voltage at OUTx during OLD trip for VM-connected load, HBX_VM_POLD = 0b		1.2		V
Passive OLD current	I_{OL_VM}	MOSFETs in Hi-Z state, current from VM to OUTx for OLD trip, HBX_VM_POLD = 1b		547		μA
Passive OLD voltage threshold	V_{OL_VM}	MOSFETs in Hi-Z state, voltage at OUTx during OLD trip for VM connected load, HBX_VM_POLD = 1b		3		V
Passive OLD detect resistance threshold	R_{OL}	MOSFETs in Hi-Z state, Full bridge connection	5		100	k Ω
Passive OLD detect resistance threshold	R_{OL}	MOSFETs in Hi-Z State, Load connected to GND	5		100	k Ω
Passive OLD detect resistance threshold	R_{OL}	MOSFETs in Hi-Z State, Load connected to VM, HBX_VM_POLD = 0b	5		400	k Ω
Passive OLD detect resistance threshold	R_{OL}	MOSFETs in Hi-Z State, Load connected to VM, HBX_VM_POLD = 1b	4		100	k Ω
Open load deglitch time	t_{OLD}	Active OLD (Continuous Mode)	2	3	4	ms
Open load deglitch time	t_{OLD}	Active OLD (PWM Mode)	150	200	300	μs

Parameters	Symbol	Test Conditions	Min	Typ	Max	Unit
Thermal warning temperature	T_{OTW}	Die temperature (T_J)	120	140	170	°C
Thermal warning hysteresis	T_{OTW_HYS}	Die temperature (T_J)		25		°C
Thermal shutdown temperature	T_{OTSD}	Die temperature (T_J)	150	180	200	°C
Thermal shutdown hysteresis	T_{OTSD_HYS}	Die temperature (T_J)		25		°C

TIMING REQUIREMENTS

Parameters	Symbol	Test Conditions	Min	Typ	Max	Unit
SPI (CSN, SCLK, SDI, SDO)						
SPI ready after enable	t_{READY}	$V_M > UVLO, ENABLE = 3.3 V$			1	ms
SCLK minimum period	t_{CLK}		200			ns
SCLK minimum high time	t_{CLKH}		100			ns
SCLK minimum low time	t_{CLKL}		100			ns
SDI input data setup time	t_{SU_SDI}		40			ns
SDI input data hold time	t_{HD_SDI}		60			ns
SDO output data delay time	t_{DLY_SDO}	SCLK high to SDO valid			60	ns
CSN input setup time	t_{SU_CSN}		100			ns
CSN input hold time	t_{HD_CSN}		100			ns
CSN minimum high time before active low	t_{HI_CSN}		600			ns
CSN disable delay time	t_{DIS_CSN}	CSN high to SDO high impedance		30		ns

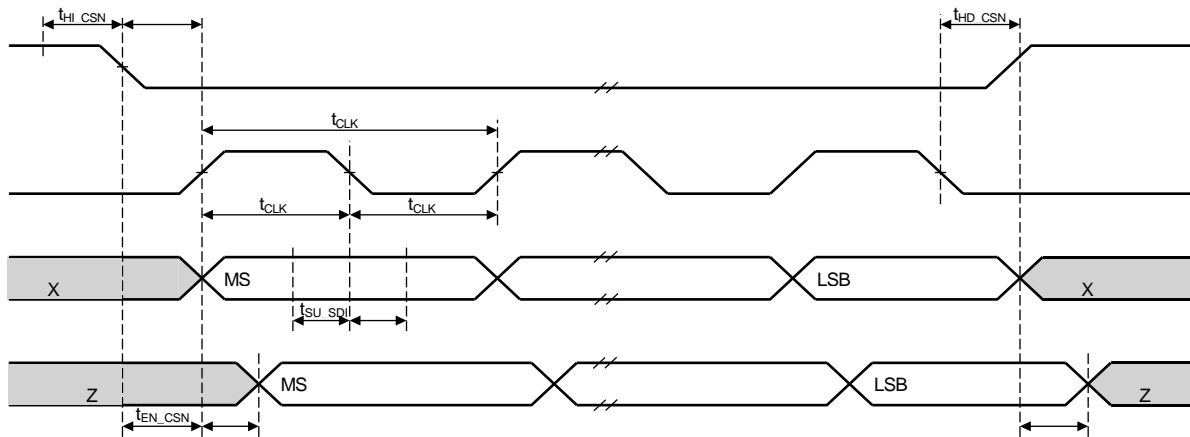
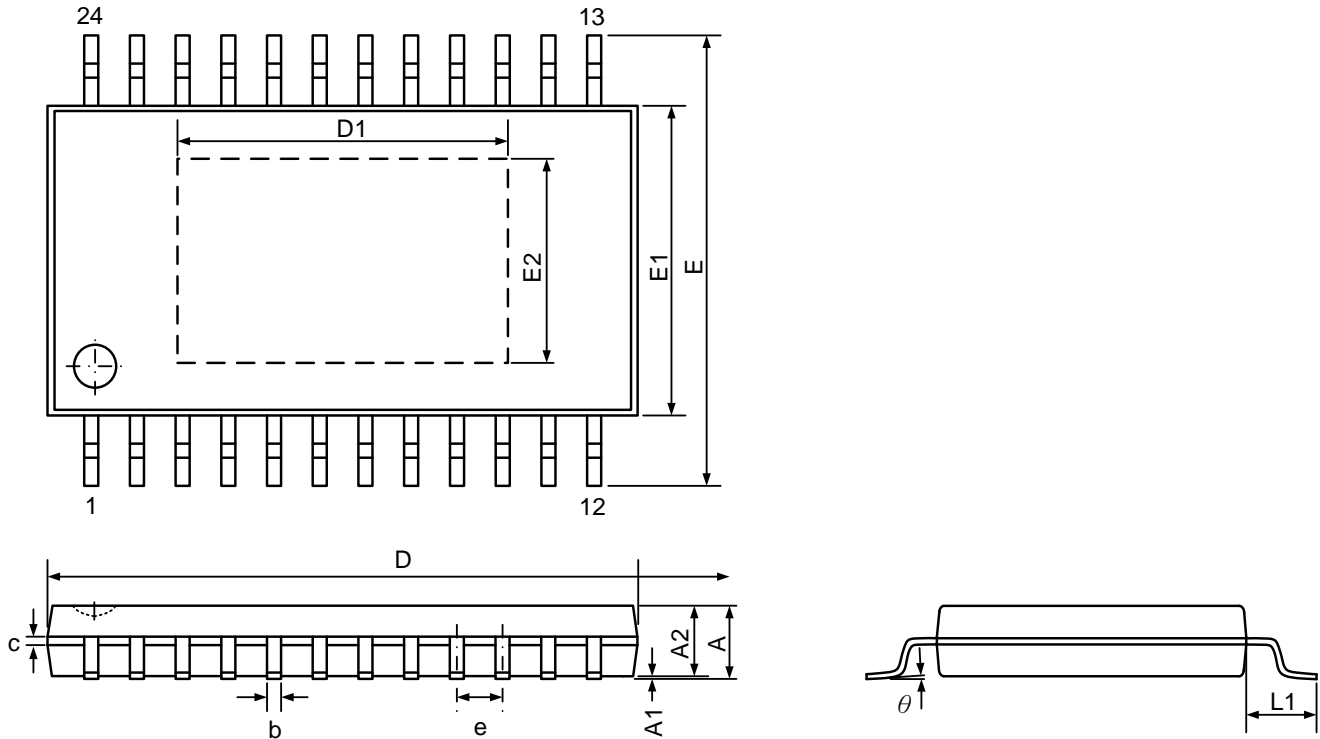


Figure 1. SPI Timing

PACKAGE INFORMATION

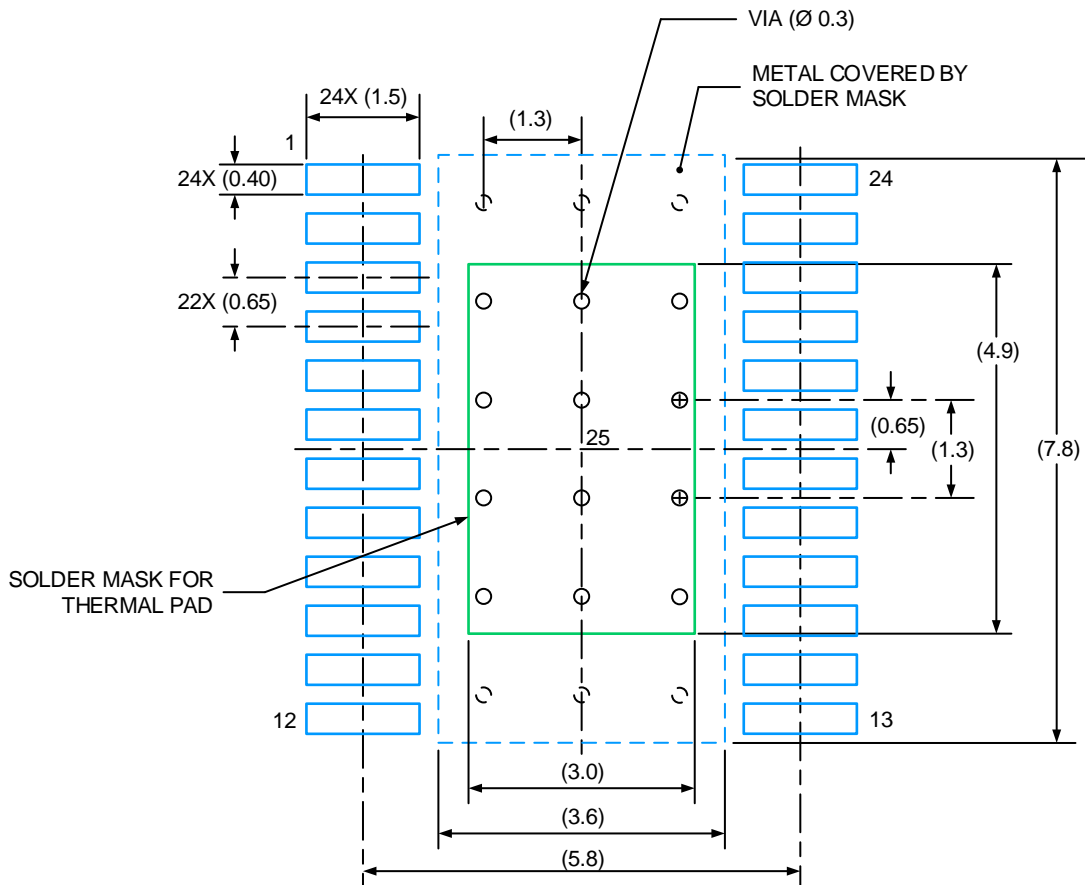
24 PINS, HTSSOP, BODY WIDTH = 4.4MM (173MIL)



Symbol	Dimensions(mm)		
	Min.	Nom.	Max.
A	-	-	1.20
A1	0.00	-	0.15
A2	0.80	1.00	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	7.70	7.80	7.90
E1	4.30	4.40	4.50
D1	3.70	4.70	4.75
E2	2.28	2.90	3.0
E	6.00 BSC		
e	0.65 BSC		
L1		1.00 REF	
θ	0°	-	8°

Note: Refer to JEDEC MO-153 ADT

PCB LAND PATTERN



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