DESCRIPTION

The PT16557 is 1/3 duty and 1/4 duty LCD display drivers that can directly drive up to 164 segments and can control up to four general-purpose output ports. These products also incorporate a key scan circuit that accepts input from up to 30 keys to reduce printed circuit board wiring.

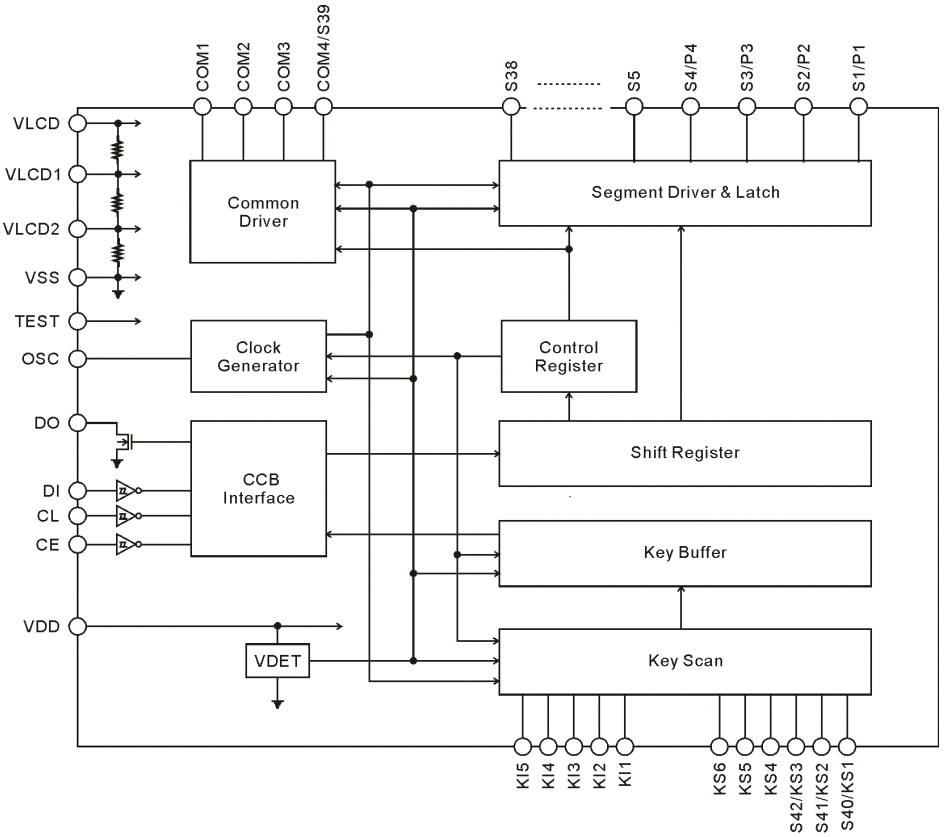
FEATURES

- Key input function for up to 30 keys (A key scan is performed only when a key is pressed.)
- 1/3 duty and 1/4 duty drive schemes can be controlled from serial data.
- 1/2 bias and 1/3 bias drive schemes can be controlled from serial data.
- Capable of driving up to 126 segments using 1/3 duty and up to 164 segments using 1/4 duty.
- Sleep mode and all segments off functions that are controlled from serial data.
- Switching between key scan output and segment output can be controlled from the serial data.
- The key scan operation enabled/disabled state can be controlled from the serial data.
- Switching between segment output port and general-purpose output port can be controlled from serial data.
- The common and segment output waveform frame frequency can be controlled from the serial data.
- Switching between RC oscillator mode and external clock mode can be controlled from the serial data.
- Serial data I/O supports CCB format communication with the system controller.
- Direct display of display data without the use of a decoder provides high generality.
- Independent V_{LCD} for the LCD driver block. (When the logic block supply voltage V_{DD} is in the range 3.6 to 6.0V, V_{LCD} can be set to a voltage in the range 0.75 x V_{DD} to 6.0V, and when V_{DD} is in the range 2.7 to 3.6V, V_{LCD} can be set to a voltage in the range 2.7 to 6.0V.)
- Provision of an on-chip voltage-detection type reset circuit prevents incorrect displays.
- AEC-Q100 Grade2 Compliant for Automotive Applications

APPLICATION

- Electronic Equipment with LCD Display

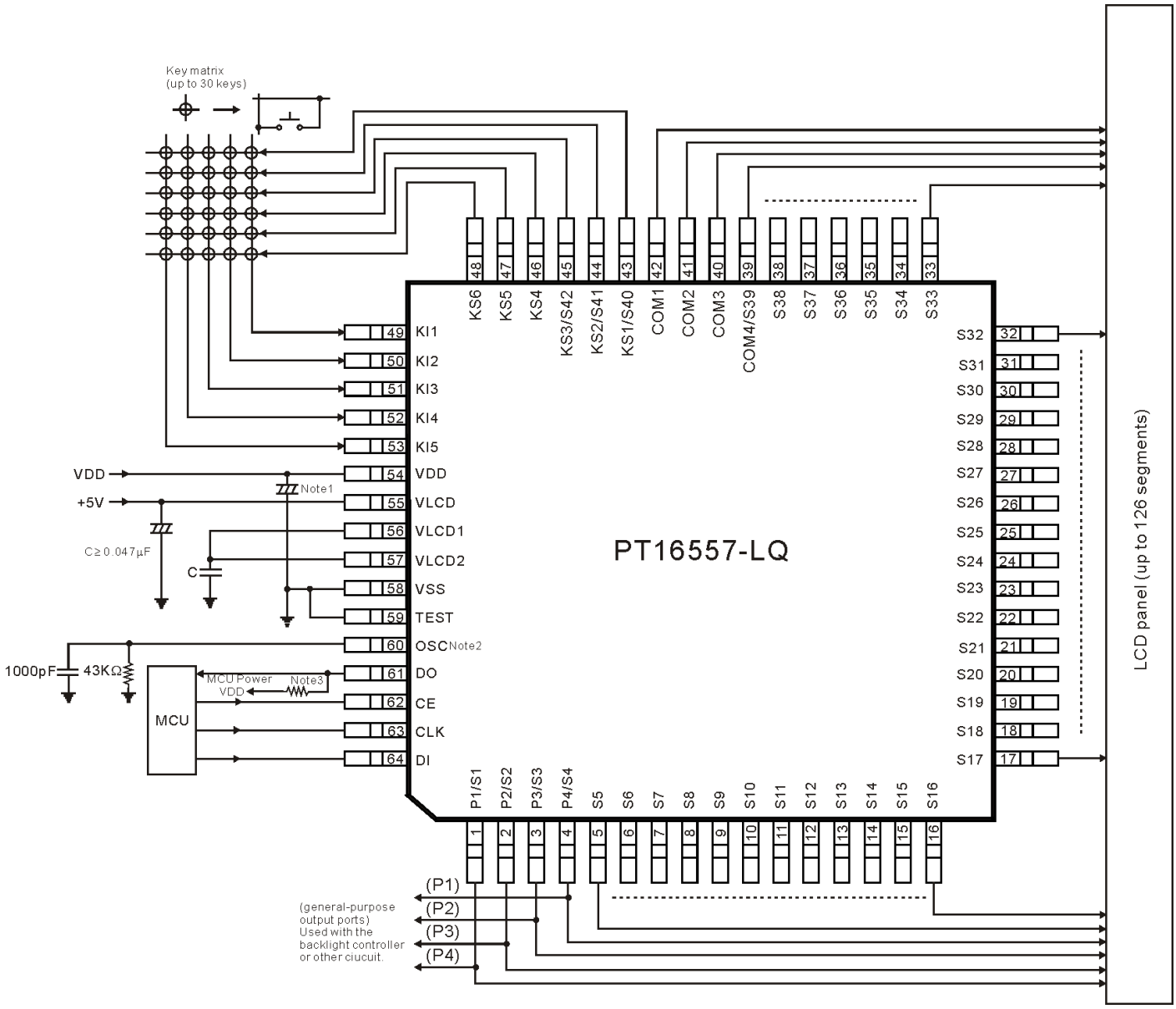
BLOCK DIAGRAM



CONTENTS

1. APPLICATION CIRCUITS

1.1 1/2 BIAS (FOR USE WITH NORMAL PANELS)



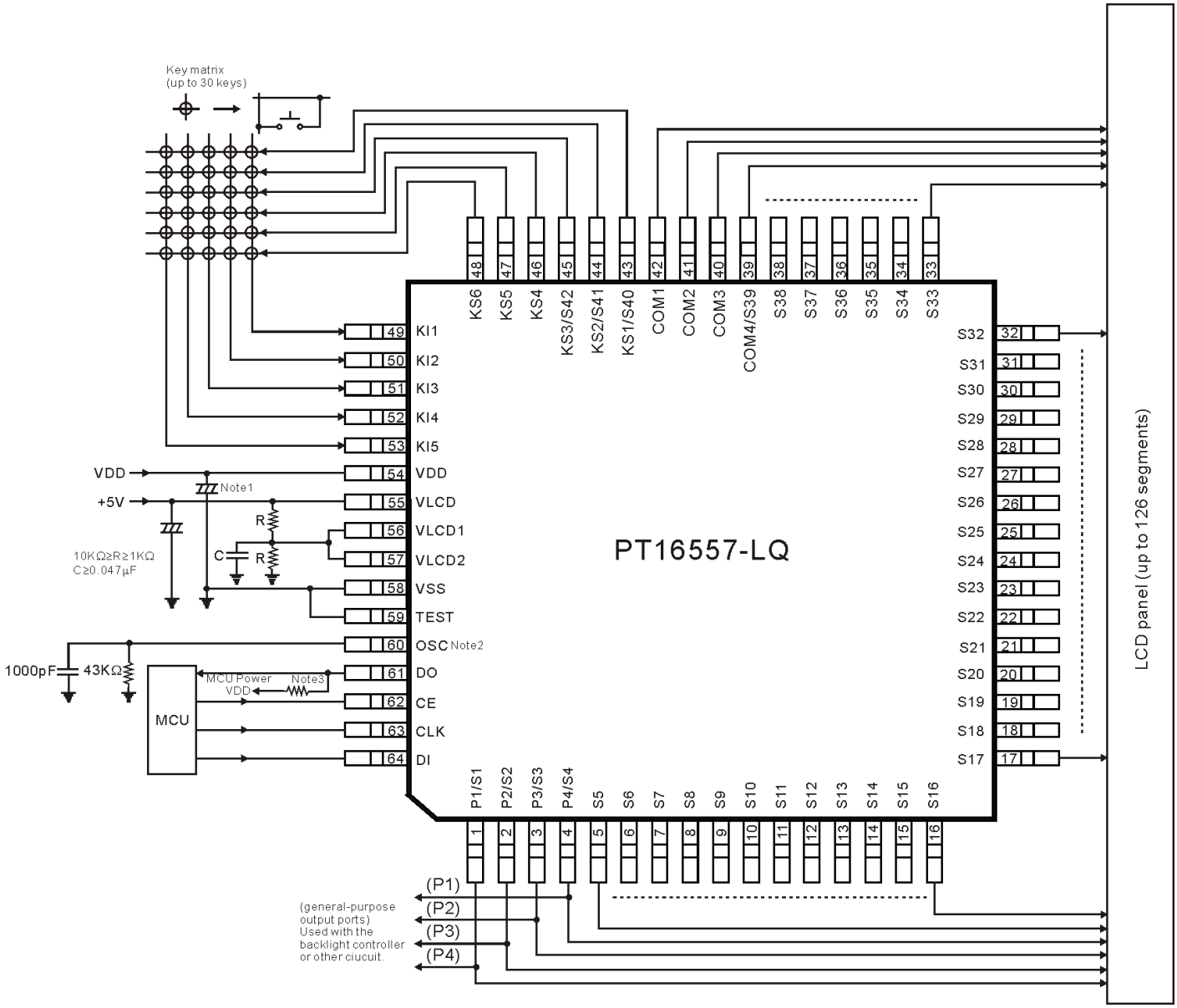
Notes:

1 Add a capacitor to the logic block power supply line so that the logic block power supply voltage V_{DD} rise time when power is applied and the logic block power supply voltage V_{DD} fall time when power drops are both at least 1ms, as the PT16557 is reset by the VDET.

2 When RC oscillator mode is used, the external resistor Rosc and the external capacitor Cosc must be connected between the OSC pin and ground, and when external clock mode is selected the current protection resistor Rg (4.7 to 47KΩ) must be connected between the OSC pin and the external clock output pin (external oscillator). (See the section on the OSC pin peripheral circuit.)

3 The DO pin, being an open-drain output, requires a pull-up resistor. Select a resistance (between 1 and 10KΩ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.

1.2 1/2 BIAS (FOR USE WITH LARGE PANELS)



Notes:

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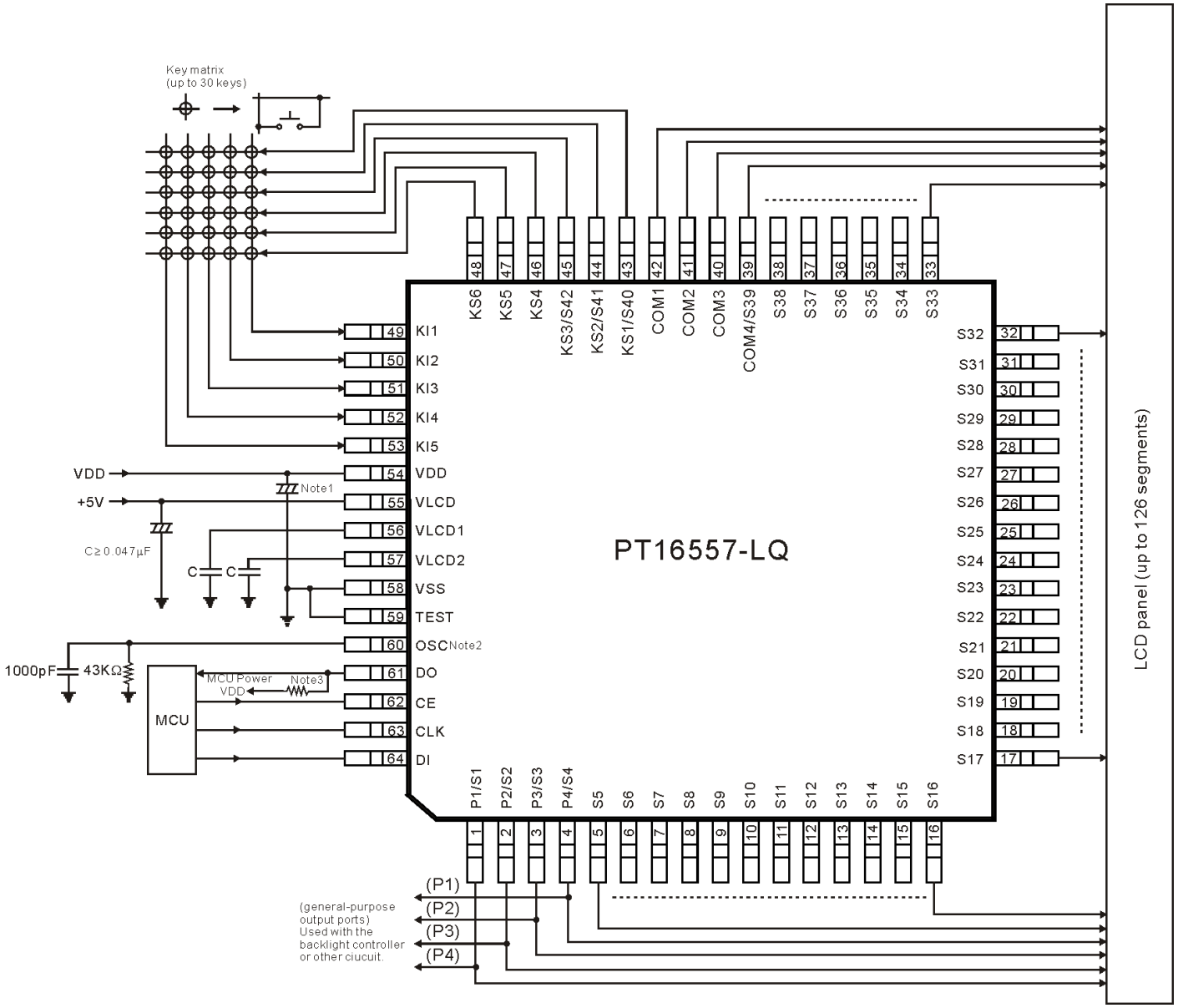
3 The DO pin, being an open-drain output, requires a pull-up resistor. Select a resistance (between 1 and 10KΩ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.

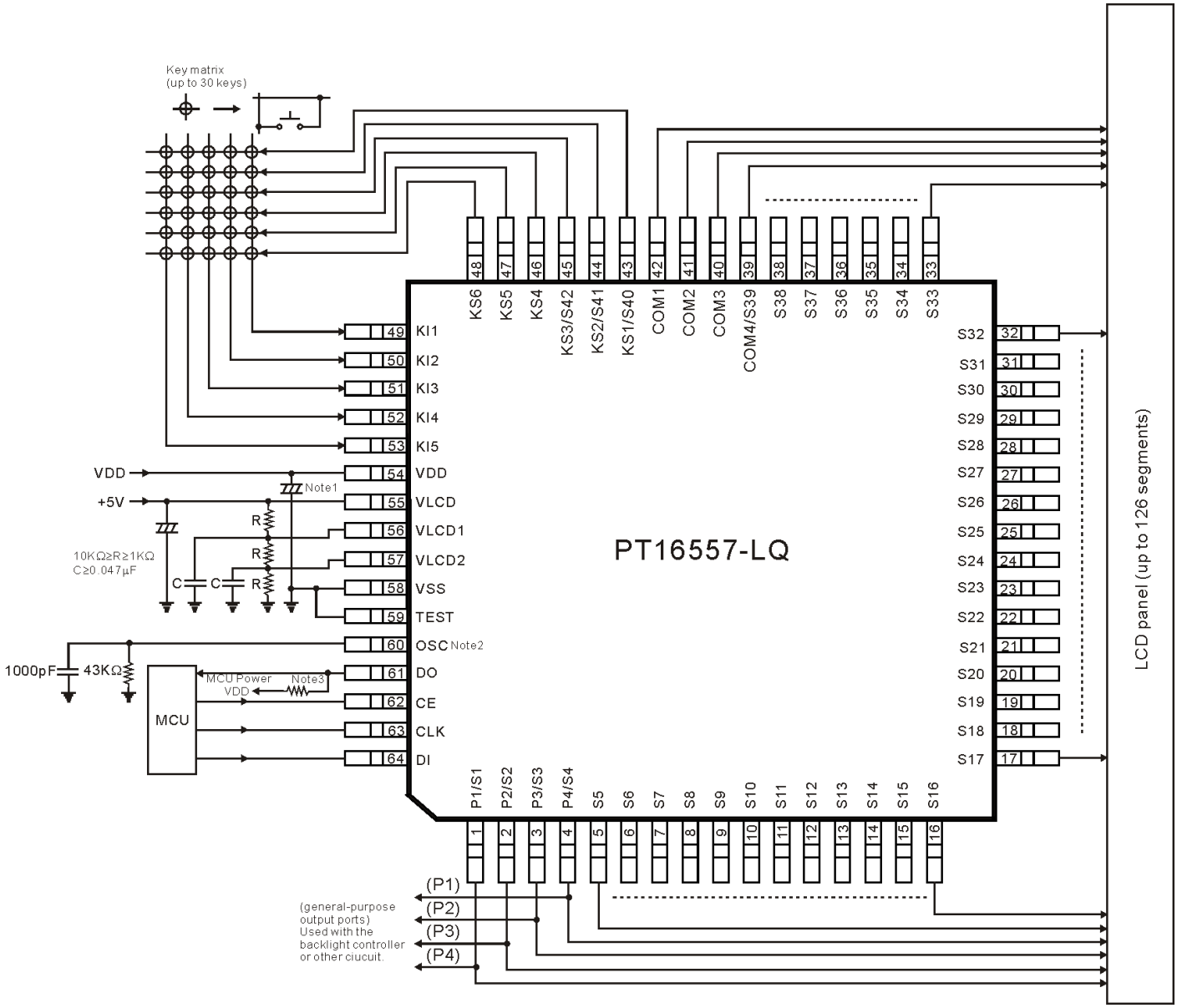
1.3 1/3 BIAS (FOR USE WITH NORMAL PANELS)



Notes:

1. Add a capacitor to the logic block power supply line so that the logic block power supply voltage V_{DD} rise time when power is applied and the logic block power supply voltage V_{DD} fall time when power drops are both at least 1ms, as the PT16557 is reset by the VDET.
2. When RC oscillator mode is used, the external resistor Rosc and the external capacitor Cosc must be connected between the OSC pin and ground, and when external clock mode is selected the current protection resistor Rg (4.7 to 47KΩ) must be connected between the OSC pin and the external clock output pin (external oscillator). (See the section on the OSC pin peripheral circuit.)
3. The DO pin, being an open-drain output, requires a pull-up resistor. Select a resistance (between 1 and 10KΩ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.

1.4 1/3 BIAS (FOR USE WITH LARGE PANELS)



Notes:

1. Add a capacitor to the logic block power supply line so that the logic block power supply voltage V_{DD} rise time when power is applied and the logic block power supply voltage V_{DD} fall time when power drops are both at least 1ms, as the PT16557 is reset by the VDET.
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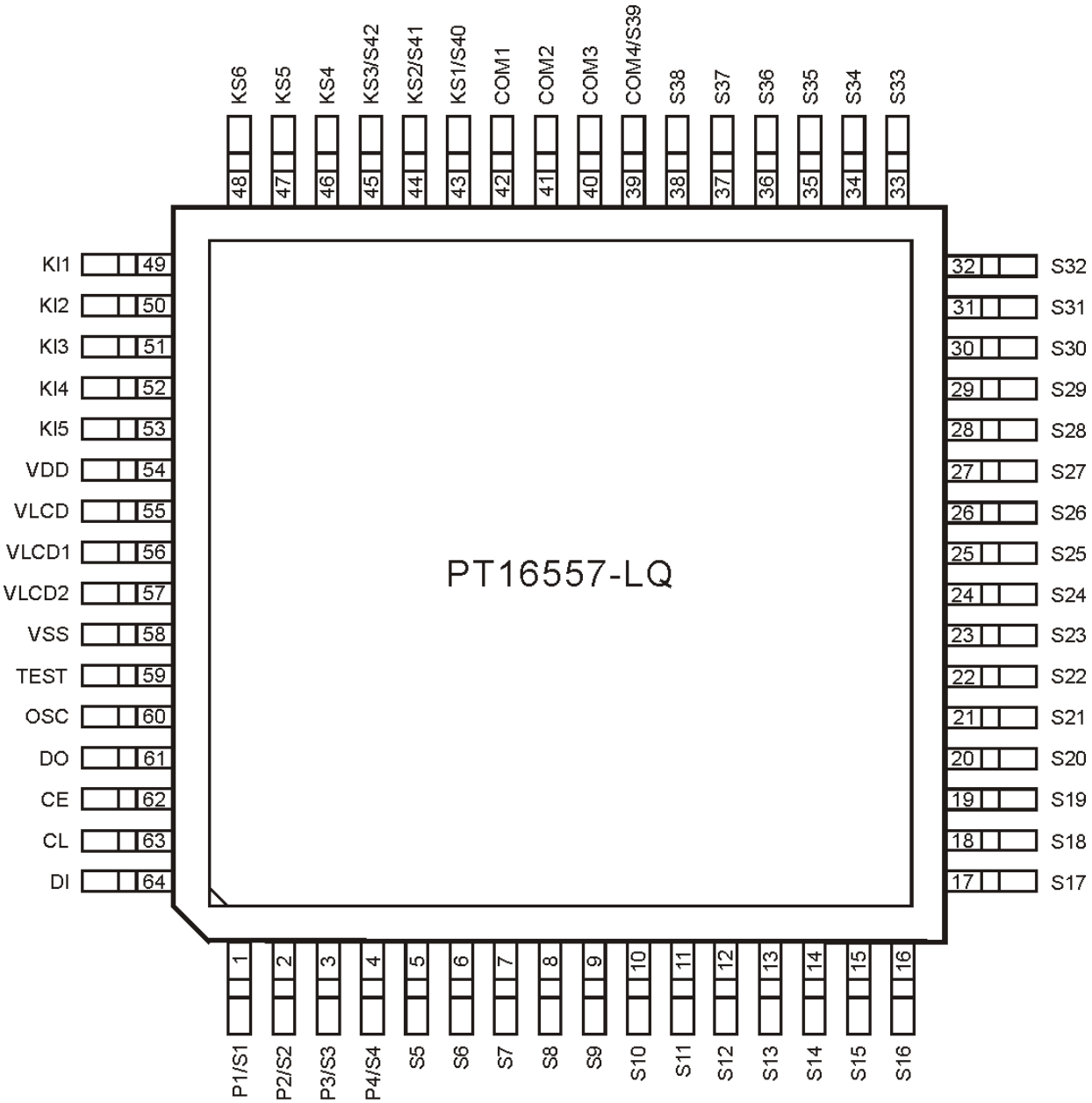
3. The DO pin, being an open-drain output, requires a pull-up resistor. Select a resistance (between 1 and 10KΩ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.

2. ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT16557-LQ	64 Pin, LQFP	PT16557-LQ

3.PIN CONFIGURATION



4.PIN DESCRIPTION

Pin Name	I/O	Active	Handling when unused	Description	Pin No.
S1/P1 to S4/P4 S5 to S38	O	-	OPEN	Segment outputs for displaying the display data transferred by serial data input. The S1/P1 to S4/P4 pins can be used as general-purpose output ports under serial data control.	1 to 4 5 to 38
COM4/S39 COM3 to COM1	O	-	OPEN	Common driver outputs The frame frequency is fo [Hz] The COM4/S39 pin can be used as a segment output in 1/3 duty.	39 40 to 42
KS1/S40 KS2/S41 KS3/S42 KS4 to KS6	O	-	OPEN	Key scan outputs Although normal key scan timing lines require diodes to be inserted in the timing lines to prevent shorts, since these outputs are unbalanced CMOS transistor outputs, these outputs will not be damaged by shorting when these outputs are used to form a key matrix. The KS1/S40 to KS3/S42 pins can be used as segment outputs when so specified by the control data.	43 44 45 46 to 48
KI1 to KI5	I	H	GND	Key scan inputs These pins have built-in pull-down resistors.	49 to 53
V_{DD}	-	-	-	Logic block power supply connection. Provide a voltage of between 2.7 and 6.0V.	54
V_{LCD}	-	-	-	LCD driver block power supply connection. A voltage in the range 0.75 × V_{DD} to 6.0V must be provided when V_{DD} is in the range 3.6 to 6.0V, and a voltage in the range 2.7V to 6.0V must be provided when V_{DD} is in the range 2.7 to 3.6V.	55
V_{LCD1}	-	-	OPEN	Used for applying the LCD drive 2/3 bias voltage externally. Must be connected to V_{LCD2} when a 1/2 bias drive scheme is used.	56
V_{LCD2}	-	-	OPEN	Used for applying the LCD drive 1/3 bias voltage externally. Must be connected toV_{LCD1} when a 1/2 bias drive scheme is used.	57
V_{SS}	-	-	-	Power supply connection. Connect to ground.	58
TEST	-	-	-	This pin must be connected to ground.	59
OSC	I/O	-	V_{DD}	The OSC pin can be used to form an oscillator circuit with an external resistor and an external capacitor. If external clock mode is selected with the control data, this pin is used to input an external clock signal.	60
DO	O	-	OPEN	Serial data interface connections to the controller. Note that DO, being an open-drain output, requires a pull-up resistor. DO: Output data CE: Chip enable CL: Synchronization clock DI : Transfer data	61
CE	I	H	GND		62
CL	I	↑			63
DI	I	-			64

IMPORTANT NOTICE

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