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Princeton Technology Corp.

DESCRIPTION

The PT16589 is 1/4 duty and 1/3 duty LCD display driver that can directly drive up to 224 segments and can control up to 5 general-purpose output ports. This product also incorporates a key scan circuit that accepts input from up to 30 keys to reduce printed circuit board wiring.
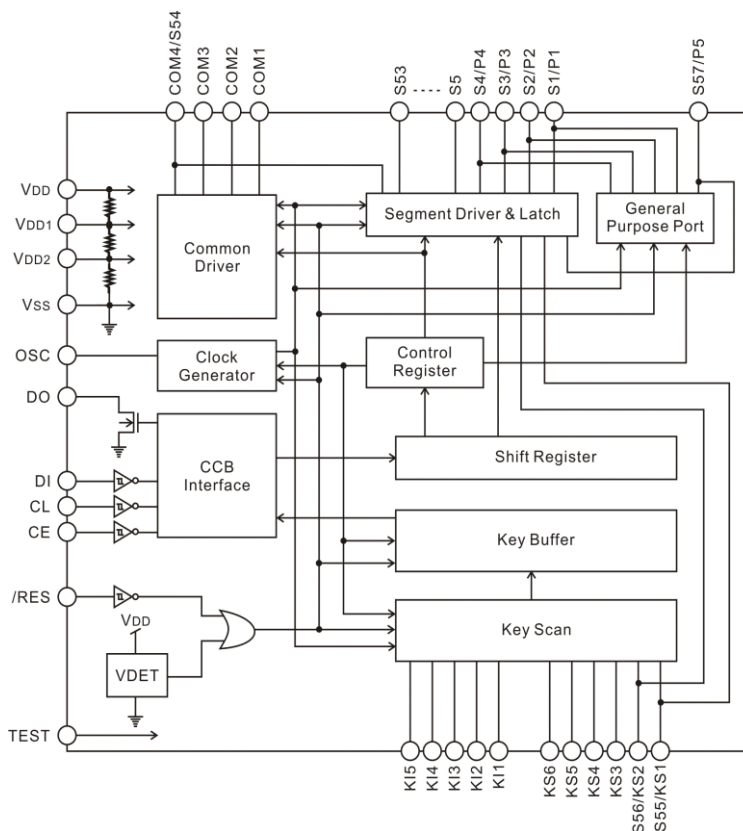
APPLICATION

- Electronic Equipment with LCD Display

FEATURES

- Key input function for up to 30 keys (A key scan is performed only when a key is pressed.)
- 1/4 duty 1/3 bias and 1/3 duty 1/3 bias drive schemes can be controlled from serial data.
- Capable of driving up to 224 segments using 1/4 duty and up to 171 segments using 1/3 duty.
- Switching between key scan output and segment output can be controlled from serial data.
- The key scan operation enabled/disabled state can be controlled from serial data.

- Switching between segment output port and general-purpose output port can be controlled from serial data.
- Switching between general-purpose output port, clock output port, and segment output port can be controlled from serial data. (Up to 5 general-purpose output ports and up to one clock output port)
- Serial data I/O supports CCB format communication with the system controller. (Support 3.3V and 5V operation)
- Sleep mode and all segments off functions that are controlled from serial data.
- The frame frequency of the common and segment output waveforms can be controlled from serial data.
- Switching between RC oscillator operating mode and external clock operating mode can be controlled from serial data.
- Direct display of display data without the use of a decoder provides high generality.
- Provision of an on-chip voltage-detection type reset circuit prevents incorrect displays.
- /RES pin provided for forcibly initializing the IC internal circuits.
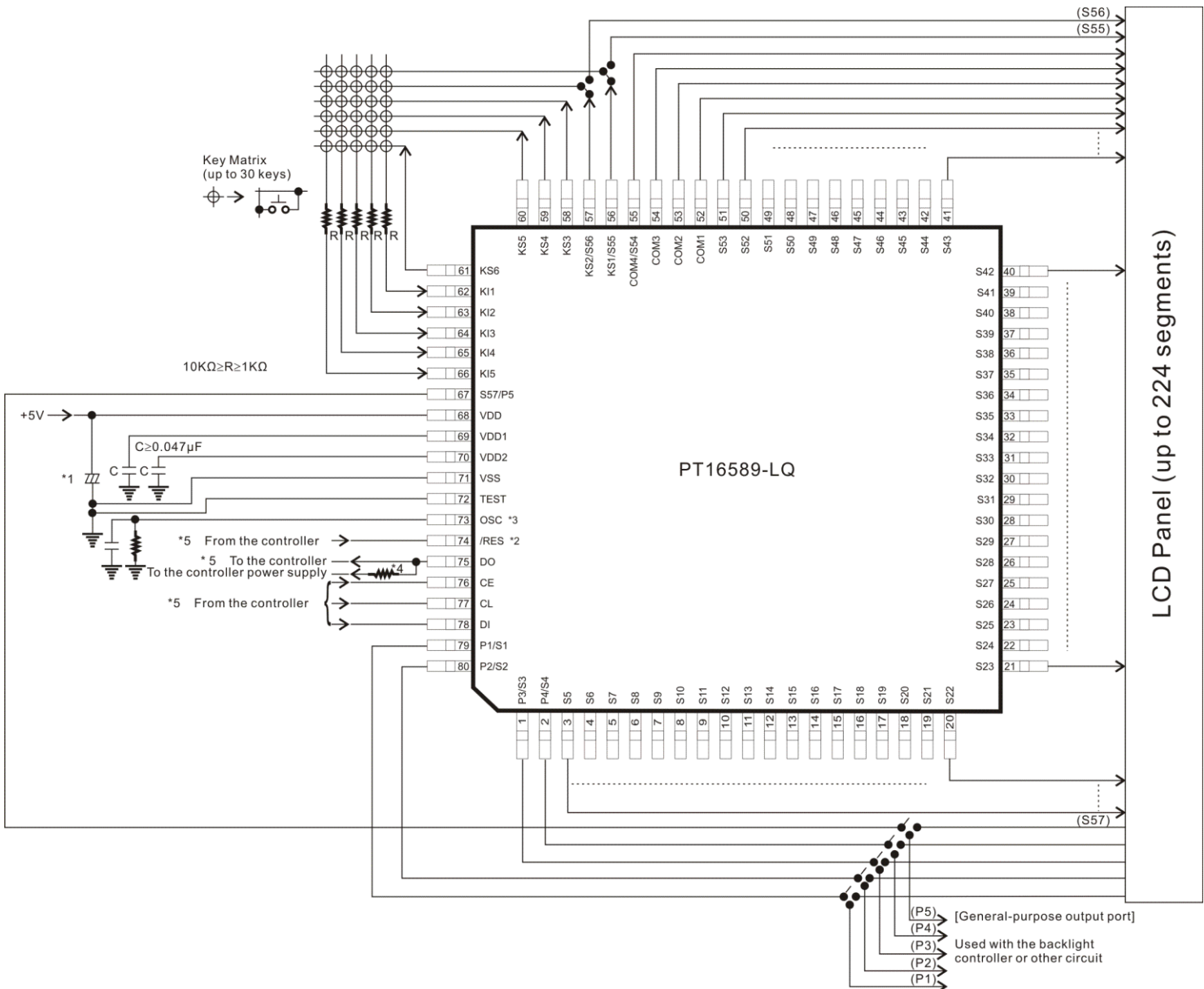
BLOCK DIAGRAM

CONTENTS

1. APPLICATION CIRCUITS

1.1 1/4 DUTY, 1/3 BIAS (FOR USE WITH NORMAL PANELS)

Key Matrix
(up to 30 keys)

$10K\Omega \geq R \geq 1K\Omega$

+5V

$C \geq 0.047\mu F$

*1

From the controller
*5 To the controller
To the controller power supply
*5 From the controller

PT16589-LQ

LCD Panel (up to 224 segments)

(S56)
(S55)

(S57)

(P5) [General-purpose output port]
(P4)
(P3) Used with the backlight
(P2) controller or other circuit
(P1)

Pin	Name	Pin	Name
61	KS6	40	S42
62	KI1	39	S41
63	KI2	38	S40
64	KI3	37	S39
65	KI4	36	S38
66	KI5	35	S37
67	S57/P5	34	S36
68	VDD	33	S35
69	VDD1	32	S34
70	VDD2	31	S33
71	VSS	30	S32
72	TEST	29	S31
73	OSC *3	28	S30
74	/RES *2	27	S29
75	DO	26	S28
76	CE	25	S27
77	CL	24	S26
78	DI	23	S25
79	P1/S1	22	S24
80	P2/S2	21	S23

Top pins: 60 KS5, 59 KS4, 58 KS3, 57 KS2/S56, 56 KS1/S55, 55 COM4/S54, 54 COM3, 53 COM2, 52 COM1, 51 S53, 50 S52, 49 S51, 48 S50, 47 S49, 46 S48, 45 S47, 44 S46, 43 S45, 42 S44, 41 S43

Bottom pins: 1 P3/S3, 2 P4/S4, 3 S5, 4 S6, 5 S7, 6 S8, 7 S9, 8 S10, 9 S11, 10 S12, 11 S13, 12 S14, 13 S15, 14 S16, 15 S17, 16 S18, 17 S19, 18 S20, 19 S21, 20 S22

Notes:
1. Add a capacitor to the power supply line so that the power supply voltage V_{DD} rise time when power is applied and the power supply voltage V_{DD} fall time when power drops are both at least 1ms, as the PT16589 is reset by the V_{DET}.
2. If the /RES pin is not used for system reset, it must be connected to the power supply V_{DD}.
3. When RC oscillator operating mode is used, the external resistor ROSC and the external capacitor COSC must be connected between the OSC pin and GND, and when external clock operating mode is selected the current protection resistor Rg (4.7 to 47KΩ) must be connected between the OSC pin and the external clock output pin (external oscillator). (See the section on the OSC pin peripheral circuit.)
4. The DO pin, being an open-drain output, requires a pull-up resistor. Select a resistance (between 1 to 10KΩ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.
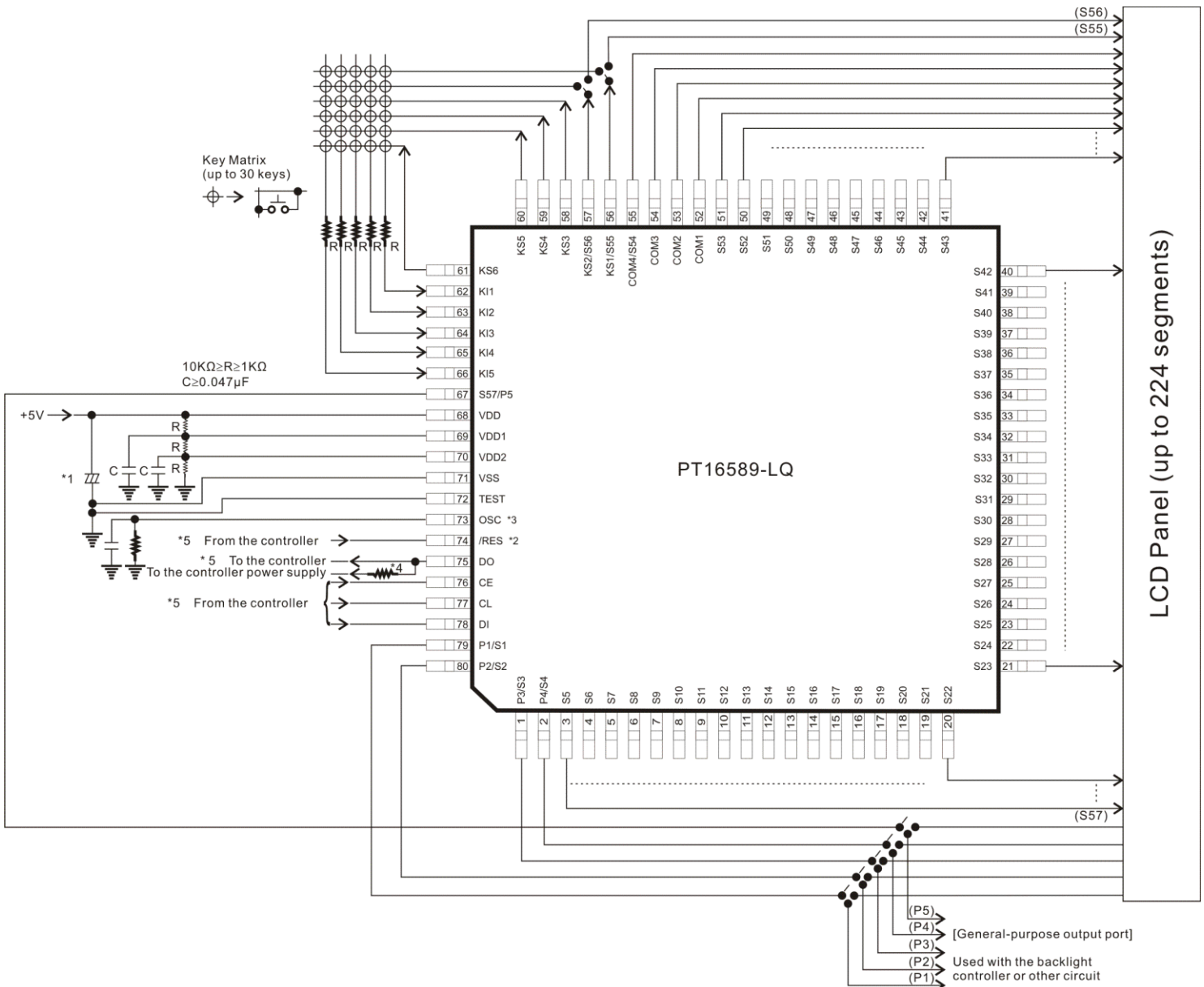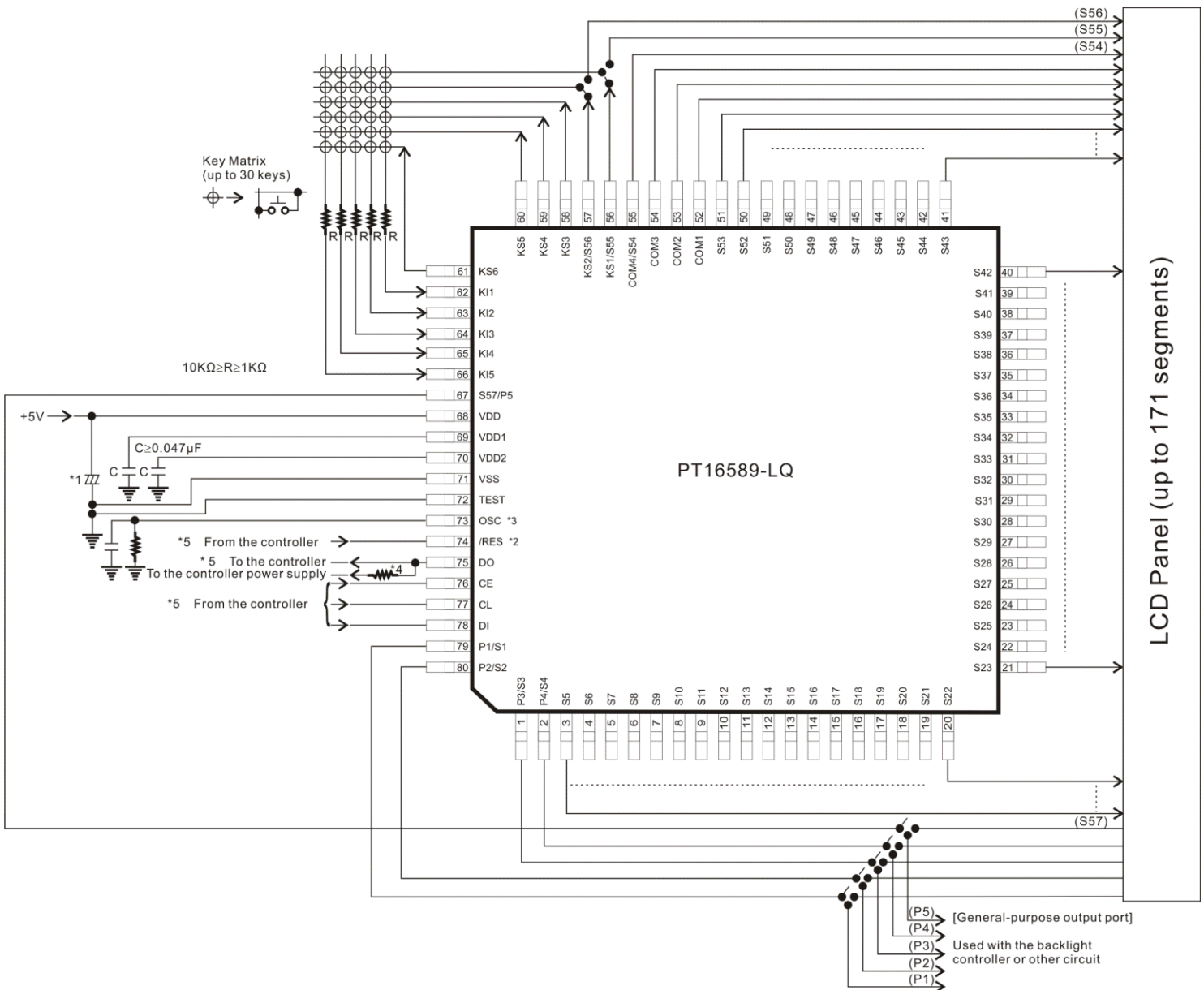5. The pins to be connected to the controller (CE, CL, DI, DO, /RES) can handle 3.3V or 5V.

1.2 1/4 DUTY, 1/3 BIAS (FOR USE WITH LARGE PANELS)

Notes:
1. Add a capacitor to the power supply line so that the power supply voltage V_{DD} rise time when power is applied and the power supply voltage V_{DD} fall time when power drops are both at least 1ms, as the PT16589 is reset by the V_{DET}.
2. If the /RES pin is not used for system reset, it must be connected to the power supply V_{DD}.
3. When RC oscillator operating mode is used, the external resistor ROSC and the external capacitor COSC must be connected between the OSC pin and GND, and when external clock operating mode is selected the current protection resistor Rg (4.7 to 47KΩ) must be connected between the OSC pin and the external clock output pin (external oscillator). (See the section on the OSC pin peripheral circuit.)
4. The DO pin, being an open-drain output, requires a pull-up resistor. Select a resistance (between 1 to 10KΩ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.
5. The pins to be connected to the controller (CE, CL, DI, DO, /RES) can handle 3.3V or 5V.
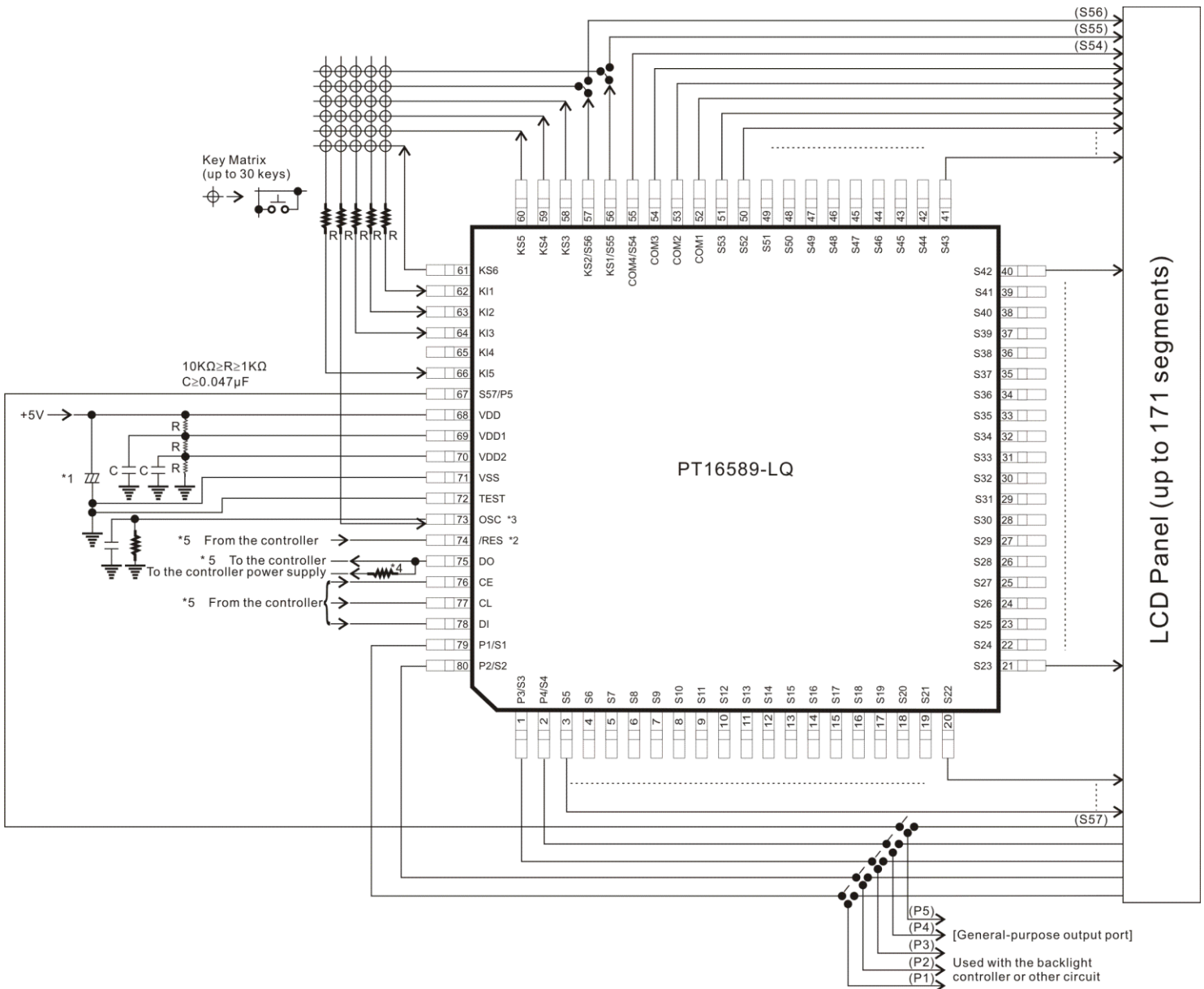
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1.3 1/3 DUTY, 1/3 BIAS (FOR USE WITH NORMAL PANELS)

Notes:

1. Add a capacitor to the power supply line so that the power supply voltage V_{DD} rise time when power is applied and the power supply voltage V_{DD} fall time when power drops are both at least 1ms, as the PT16589 is reset by the V_{DET}.
2. If the /RES pin is not used for system reset, it must be connected to the power supply V_{DD}.
3. When RC oscillator operating mode is used, the external resistor ROSC and the external capacitor COSC must be connected between the OSC pin and GND, and when external clock operating mode is selected the current protection resistor Rg (4.7 to 47KΩ) must be connected between the OSC pin and the external clock output pin (external oscillator). (See the section on the OSC pin peripheral circuit.)
4. The DO pin, being an open-drain output, requires a pull-up resistor. Select a resistance (between 1 to 10KΩ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.
5. The pins to be connected to the controller (CE, CL, DI, DO, /RES) can handle 3.3V or 5V.

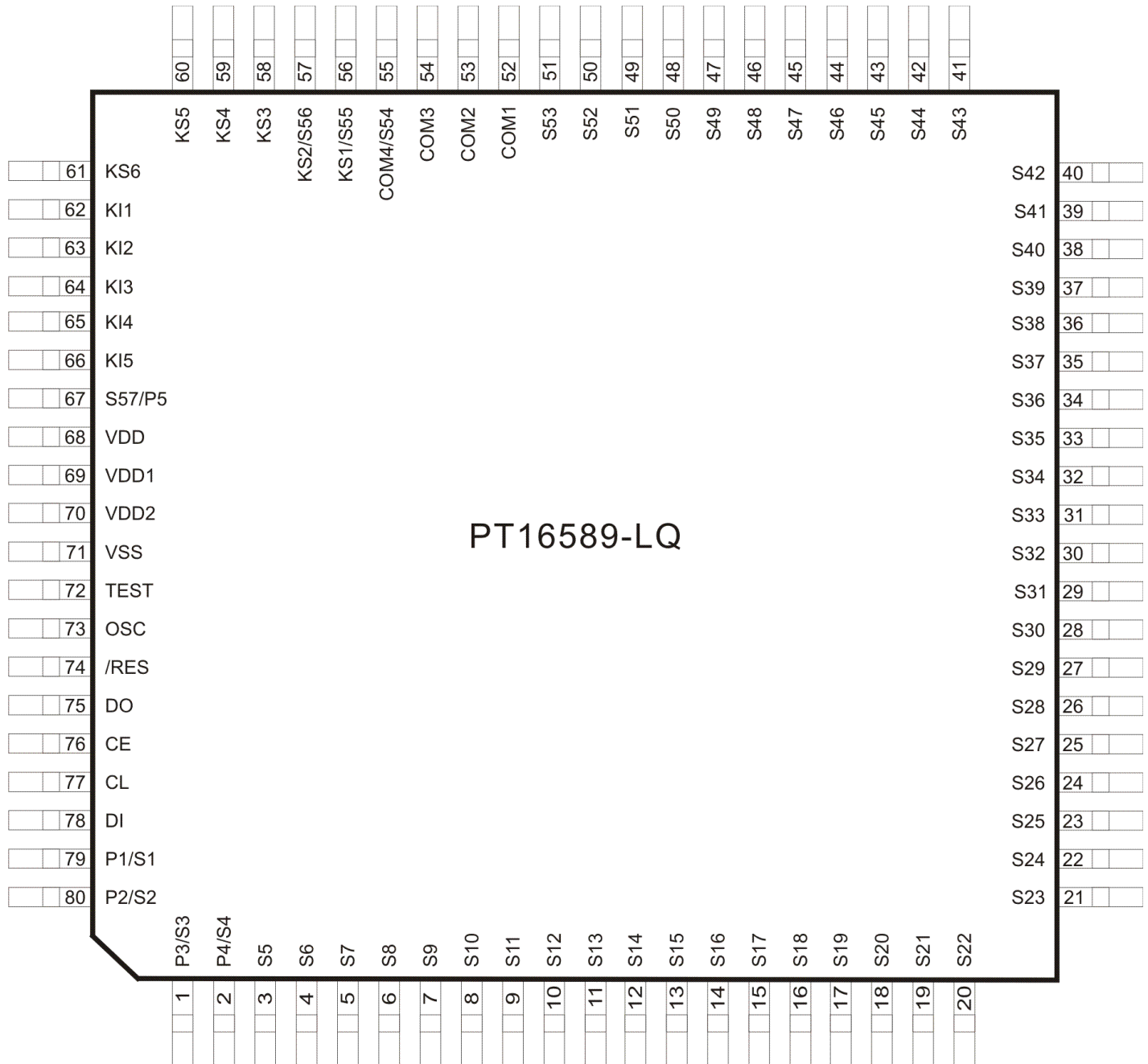# 1.4 1/3 DUTY, 1/3BIAS (FOR USE WITH LARGE PANELS)

Notes:
1. Add a capacitor to the power supply line so that the power supply voltage VDD rise time when power is applied and the power supply voltage VDD fall time when power drops are both at least 1ms, as the PT16589 is reset by the VDET.
2. If the /RES pin is not used for system reset, it must be connected to the power supply VDD.
3. When RC oscillator operating mode is used, the external resistor ROSC and the external capacitor COSC must be connected between the OSC pin and GND, and when external clock operating mode is selected the current protection resistor Rg (4.7 to 47KΩ) must be connected between the OSC pin and the external clock output pin (external oscillator). (See the section on the OSC pin peripheral circuit.)
4. The DO pin, being an open-drain output, requires a pull-up resistor. Select a resistance (between 1 to 10KΩ) appropriate for the capacitance of the external wiring so that signal waveforms are not degraded.
5. The pins to be connected to the controller (CE, CL, DI, DO, /RES) can handle 3.3V or 5V.

2. ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT16589-LQ	80-Pin, LQFP	PT16589-LQ

3.PIN CONFIGURATION

4.PIN DESCRIPTION

Pin Name	I/O	Active	Handling when unused	Description	Pin No.
S1/P1 to S4/P4 S5 to S53	O	-	OPEN	Segment outputs for displaying the display data transferred by serial data input. The S1/P1 to S4/P4 pins can be used as general-purpose output ports under serial data control.	79,80,1,2 3 to 51
COM1 to COM3 COM4/S54	O	-	OPEN	Common driver outputs. The frame frequency is f_O[Hz]. The COM4/S54 pin can be used as a segment output in 1/3 duty.	52 to 54 55
KS1/S55 KS2/S56 KS3 to KS6	O	-	OPEN	Key scan outputs. Although normal key scan timing lines require diodes to be inserted in the timing lines to prevent shorts, since these outputs are unbalanced CMOS transistor outputs, these outputs will not be damaged by shorting when these outputs are used to form a key matrix. The KS1/S55 to KS2/S56 pins can be used as segment outputs when so specified by the control data.	56 57 58 to 61
KI1 to KI5	I	H	GND	Key scan inputs. These pins have built-in pull-down resistors.	62 to 66
S57/P5	O	-	OPEN	Logic block power supply connection. Provide a voltage of between 2.7 and 6.0V.	67
V_{DD}	-	-	-	Power supply connections. Provide a voltage of between 4.5 to 6.0V.	68
V_{DD1}	I	-	OPEN	Used for applying the LCD drive 2/3 bias voltage externally. Must be connected to V_{LCD2} when a 1/2 bias drive scheme is used.	69
V_{DD2}	I	-	OPEN	Used for applying the LCD drive 1/3 bias voltage externally. Must be connected to V_{LCD1} when a 1/2 bias drive scheme is used.	70
V_{SS}	-	-	-	Power supply connection. Connect to ground.	71
TEST	I	-	-	This pin must be connected to ground.	72
OSC	I/O	-	V_{DD}	The OSC pin can be used to form an oscillator circuit with an external resistor and an external capacitor. If external clock mode is selected with the control data, this pin is used to input an external clock signal.	73
/RES	I	L	V_{DD}	Reset signal input . /RES=Low ·····Display off - S1/P1 to S4/P4, KS1/S55, KS2/S56=Low (These pins are forcibly set to the segment output port function and fixed at the low level.) - S5 to S53=Low - COM1 to COM3=Low - COM4/S54=Low (This pin is forcibly set to the common output function and fixed at the low level.) - S57/P5=Low (This pin is forcibly set to the general-purpose output port function and fixed at the low level.) - KS3 to KS6=Low - Key scanning disabled - All the key data is reset to low. - OSC="Z"(High impedance) - RC oscillation stopped - Inhibits external clock input . /RES=High ···· Display on - General-purpose output port state setting is enabled - Key scanning is enabled. - RC oscillation enabled (RC oscillator operating mode) - Enables external clock input (external clock operating mode) However, serial data can be transferred when the RES pin is low	74
DO	O	-	OPEN	Serial data interface connections to the controller. Note that DO, being an open-drain output, requires a pull-up resistor. DO: Output data	75
CE	I	H	GND	CE: Chip enable	76
CL	I	⬏		CL: Synchronization clock	77
DI	I	-		DI: Transfer data	78

IMPORTANT NOTICE

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