

DESCRIPTION

PT16755 is a 1ch high current LED Controller, supports step-up or step-down driver topologies. It incorporates a high voltage (65V) rail-to-rail current sense amplifier that can directly measure LED current using a high-side series sense resistor. The amplifier is designed to achieve low input offset voltage and attain better than $\pm 4\%$ LED current accuracy over junction temperature range of -40°C to 150°C and output voltage range of 3V to 65V.

The device implements a fixed-frequency peak current mode control technique with programmable switching frequency. A unique spread-spectrum modulation (SSM) can reduce emission (EMI) at the switching frequency and its harmonics.

PWM dimming duty can be freely set with built-in PWM generation circuit. PDRV gate driver output can be used to enable series FET dimming functionality to get over 1000:1 contrast ratio ($f_{\text{PWM}}=400\text{Hz}$).

PT16755 has two systems of analog dimming function. It can be used as BIN setting function and thermal derating function. High precision 3.0V output power supply for analog dimming and PWM dimming setting is built-in. An open drain fault indicator output to indicate LED overcurrent, short-current, output overvoltage and output under-voltage conditions.

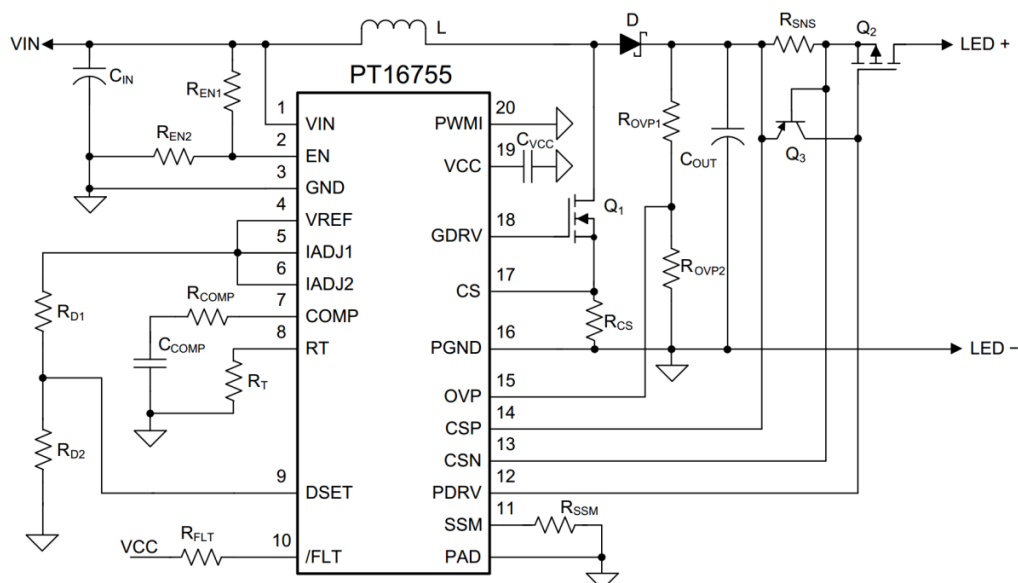
FEATURES

- Automotive AEC-Q100, Grade 1 ($-40^{\circ}\text{C} \sim +125^{\circ}\text{C}$) Qualified
- Input Voltage: 5V to 65V
- Output Voltage Range: 2V to 65V
- Low Input Offset Rail-to-Rail Current Sense Amplifier – Better than $\pm 4\%$ LED Current Accuracy over -40°C to 150°C Junction Temperature Range
- –High-Side Current Sense
- Two Analog Dimming systems
- Integrated P-Channel MOSFET Driver for LED PWM Dimming, Compatible with Direct PWM Input with over 1000:1 Dimming Range ($f_{\text{PWM}}=400\text{Hz}$).
- Spread Spectrum Modulation for Improved EMI
- Programmable Switching Frequency: 100 kHz to 1.1 MHz
- Comprehensive Fault Protection Circuitry Including VCC Under-Voltage Lockout (UVLO), Output Over-Voltage Protection (OVP), Output Under-Voltage Protection (UVP), Output over current protection (OCP), Output short-current protection(SCP), Cycle-by-Cycle Switch Current Limit and Thermal Protection.

APPLICATIONS

- Automotive High(Low) Beam Application
- Automotive Daytime Running Lights and Position Lights
- LED General Lighting Applications
- Exit Signs and Emergency Lighting

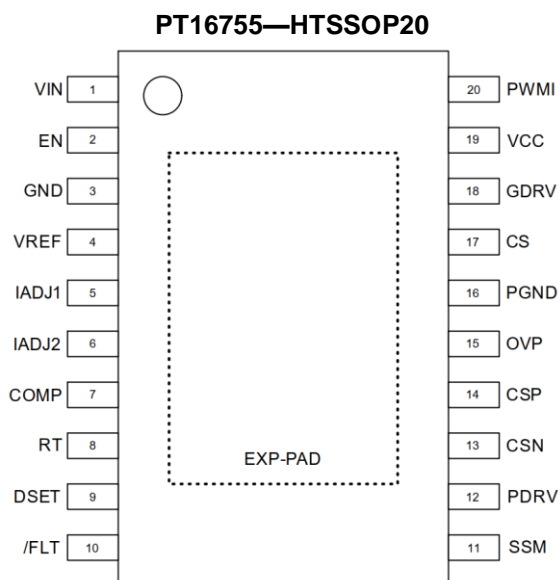
TYPICAL APPLICATION



1. ORDER INFORMATION

Part Number	Package	Top Code
PT16755-HT	20-Pin, HTSSOP	PT16755-HT

2. PIN CONFIGURATION



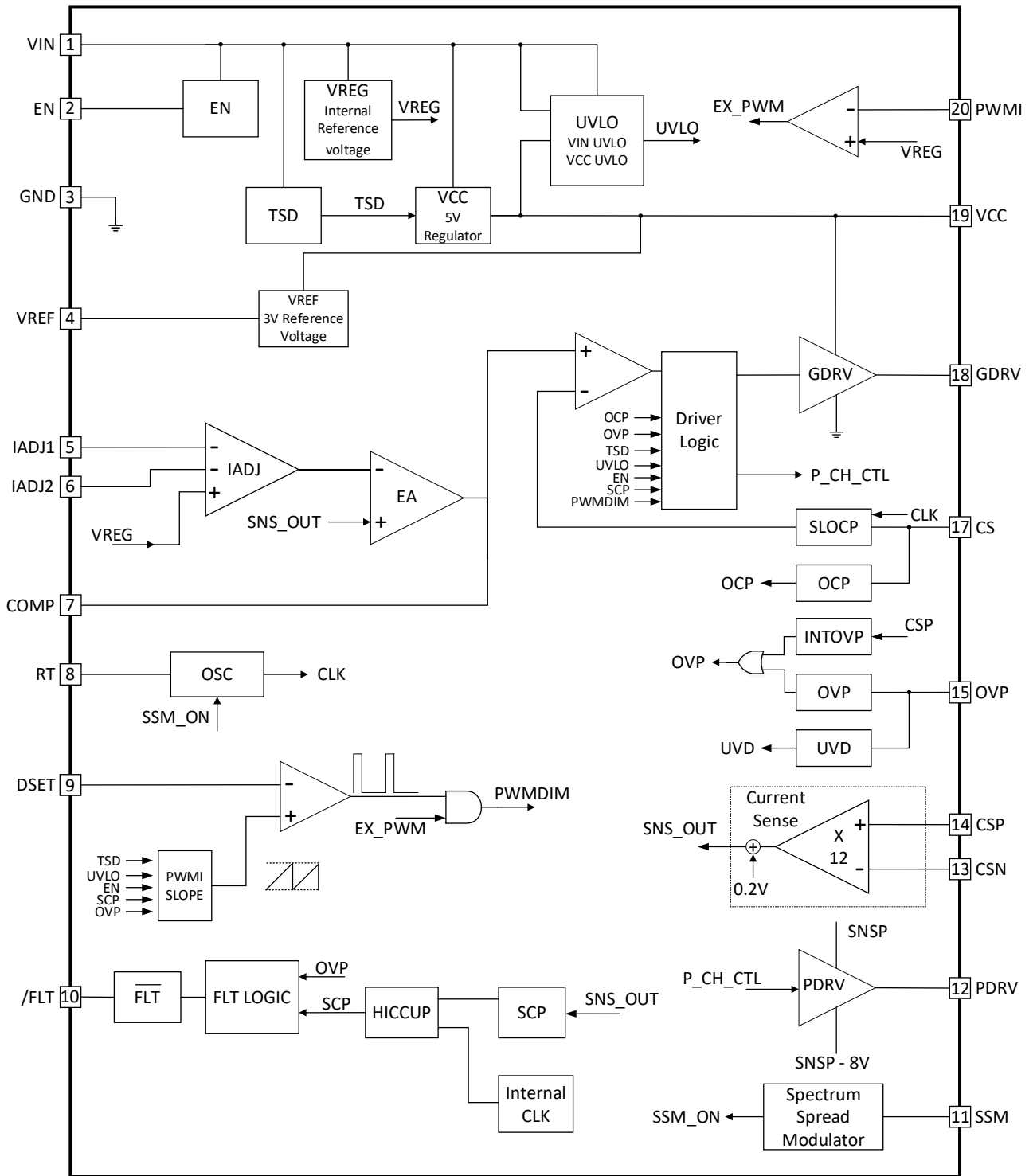
3. PIN DESCRIPTION

PIN Name	I/O	Description	PIN NO.
VIN	--	Supply voltage input.	1
EN	I	Enable input.	2
GND	--	Ground.	3
VREF	O	3.0V reference voltage.	4
IADJ1	I	Analog dimming input 1	5
IADJ2	I	Analog dimming input 2	6
COMP	I/O	Error amplifier compensation. Connect compensation network to achieve desired closed loop response.	7
RT	I/O	Programmable oscillator frequency pin. Connect a resistor to GND to set the switching frequency.	8
DSET	I	PWM dimming duty setting voltage input (connect to resistor divider from VREF to GND)	9
/FLT	O	Open-drain fault indicator. Connect to VREF with a resistor to create active low fault signal output.	10

PIN DESCRIPTION (continued)

PIN Name	I/O	Description	PIN NO.
SSM	O	Spread spectrum frequency modulation enable input (enable when SSM = Low).	11
PDRV	O	P-ch MOSFET gate drive for PWM dimming and LED protection	12
CSN	I	Current sense amplifier negative input (-). Connect directly to the negative node of LED current sense resistor R_{SNS} .	13
CSP	I	Current sense amplifier positive input (+). Connect directly to the positive node of LED current sense resistor R_{SNS} .	14
OVP	I	Output voltage monitor for over voltage protection and under voltage detection (connect to resistor divider from output voltage to GND)	15
PGND	--	Power ground	16
CS	I	Switching current sense pin. Connected to switching current sense resistor, R_{CS} , to monitor the peak current of the main MOSFET.	17
GDRV	O	Gate driver output for switching MOSFET. Connect to gate of the main MOSFET.	18
VCC	--	VCC bias supply pin. Locally decouple to GND using a ceramic capacitor (with a value between 2.2 μ F and 4.7 μ F). Locate close to the controller.	19
PWMI	I	DRL mode (100 % duty) enable input / External PWM dimming signal input.	20
Thermal PAD	--	The GND and PGND pin must be connected to the exposed thermal pad for proper operation. This PAD must be connected to PCB ground plane using multiple vias for good thermal performance.	Thermal PAD

4. FUNCTIONAL BLOCK DIAGRAM



5. FUNCTION DESCRIPTION

5.1 OVERVIEW

The PT16755 is a wide input range (5V to 65V) LED driver controller. It has all of the functions necessary to implement a compact and highly efficient LED driver, supports step-up or step-down converter topologies. The devices implement a fixed-frequency, peak current mode control technique to achieve constant output current and fast transient response. It incorporates a low input offset, rail-to-rail current sense amplifier that supports a wide range of output voltages (2V to 65 V) and is capable of powering the LED string consisting of 1 to 20 LEDs while maintaining better than 4% current accuracy over the operating temperature range.

The device has a built-in PWM dimming pulse generation circuit, provides programmable pulse width modulation (PWM) dimming function for LED current output. PWM dimming duty can be freely set with built-in PWM generation circuit. PWM dimming realizes by driving an external P-ch MOSFET. Two systems of analog dimming are built-in. High precision 3.0 V output power supply for analog dimming and PWM dimming setting is built-in.

An open-drain fault indicator (/FLT) is also provided to report faults including cycle-by-cycle current limit, output overvoltage, output over-current, output short-current and output undervoltage conditions.

5.2 HIGH ACCURACY REFERENCE VOLTAGE(VREF)

The VREF voltage 3.0 V (Typ) is generated from the VCC pin voltage. VREF is used as a reference voltage for PWM dimming duty and analog dimming setting. Input the voltage set by resistor dividing from the VREF pin to the DSET pin, the IADJ1 pin, and the IADJ2 pin.

Do not connect a capacitor to the VREF pin and do not use the VREF as a power supply other than this device.

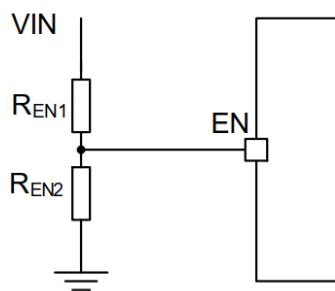
5.3 INTERNAL POWER SUPPLY (VCC)

The VCC voltage 5.0 V (Typ) is generated from the VIN pin voltage. The VCC supply powers the internal circuitry, GDRV driver and PDRV driver. Locally decouple to PGND using a 2.2μF to 4.7μF ceramic capacitor located close to the controller.

The VCC is a regulated output of the internal regulator and cannot be driven from an external power supply

5.4 ENABLE SETTING (EN)

The PT16755 can be ON/OFF controlled by the EN pin. It is possible to set the EN pin voltage by a resistor voltage divider from VIN.



$$V_{ENON} = \frac{(R_{EN1} + R_{EN2})}{R_{EN2}} \times V_{ENIH}$$

$$V_{ENOFF} = \frac{(R_{EN1} + R_{EN2})}{R_{EN2}} \times V_{ENIL}$$

V_{ENIH} : the EN high level threshold voltage 1.0 V (Typ); V_{ENIL} : the EN low level threshold voltage 0.9 V (Typ)
When the EN pin voltage becomes V_{ENIL} or less, the PDRV pin outputs high level to turn off external P-ch MOSFET. The device stops driving and the GDRV pin outputs low level.

When pulling up to the VIN pin to fix the EN pin to high, considering the short circuit between the EN pin and the GND pin, it is recommended to insert a limiting resistor.

5.5 OSCILLATOR

The switching frequency of the device can be set by the resistor R_{RT} connected to the RT pin:

$$R_T = \frac{9900 \times 10^3}{f_{sw}} \text{ (K}\Omega\text{)} \quad f_{sw} = 100 \text{ KHz} \sim 1100 \text{ KHz}$$

Figure 1 shows a graph of switching frequency versus resistance R_{RT} . It recommends a switching frequency setting between 100 KHz and 1100 KHz for optimal performance over input and output voltage operating range and for best efficiency. Operation at higher switching frequencies requires careful selection of N-channel MOSFET characteristics as well as detailed analysis of switching losses.

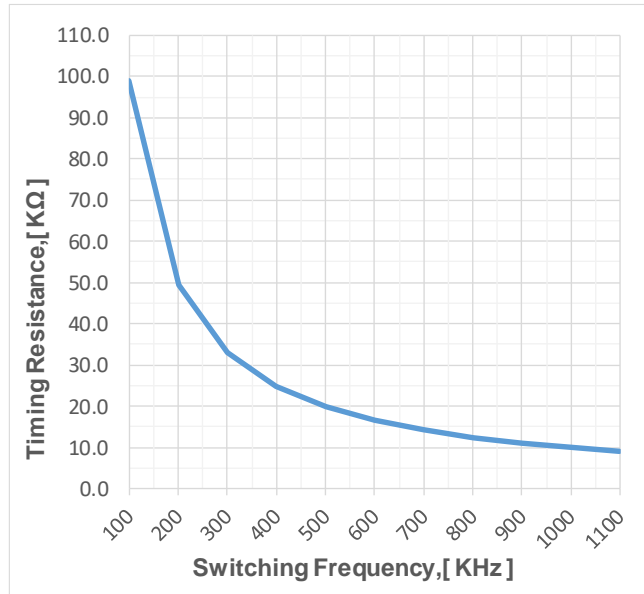


Figure 1. Timing Resistance (R_{RT}) VS Switching Frequency

5.6 ANALOG DIMMING ($IADJ1/2$)

The PT16755 has two systems of analog dimming function. For example, it can be used as in Figure 2. (a) Thermal Derating Function and BIN Setting Function or in Figure 2. (b) Thermal Derating Function and Input Low Voltage Derating Function.

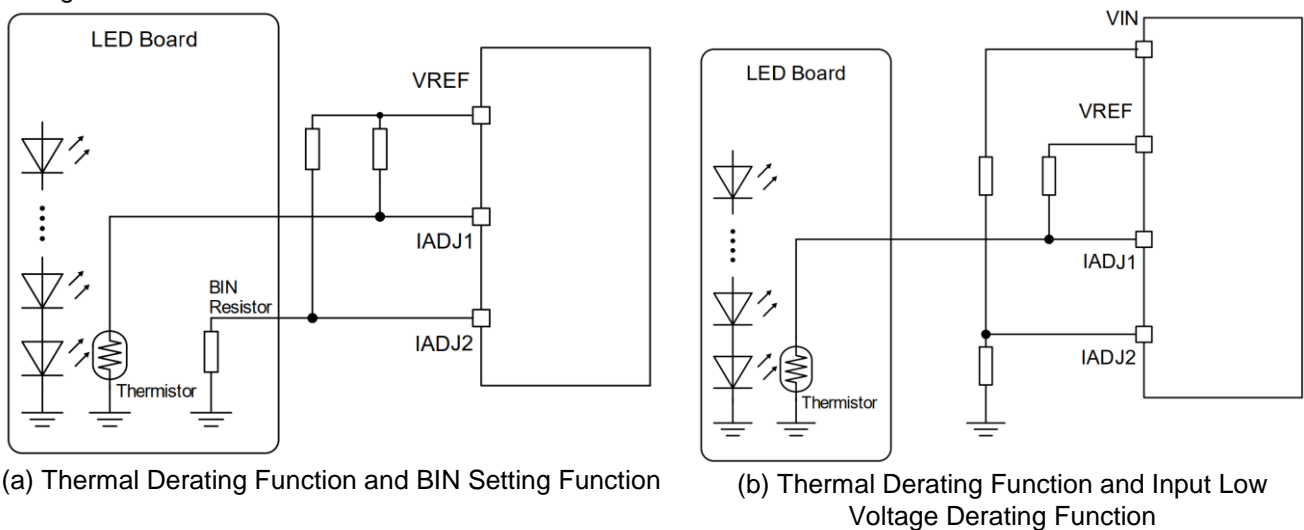


Figure 2. Analog Dimming Application Example

When the IADJ1 or IADJ2 pin (The lower voltage takes precedence) becomes 2.18 V (Typ) or less, the LED current Decreases.

When not using the analog dimming function, set it to 2.5 V or more, such as connecting IADJ1, IADJ2 pins to the VREF pin.

When the analog dimming rate is low, the device control may become unstable and the LED may flicker. Confirm enough in the evaluation.

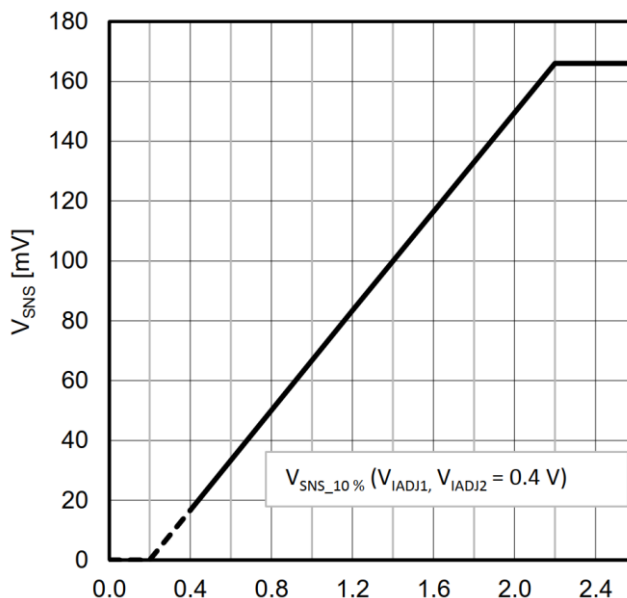


Figure 3. V_{SNS} vs IADJ Voltage

5.7 LED CURRENT SETTING (CSP, CSN)

LED current can be set by resistor R_{SNS} connected between the CSP pin and CSN pin:

$$I_{LED} = \frac{V_{SNS_100\%}}{R_{SNS}} [A]$$

V_{SNS_100%} : current sense threshold voltage between CSP pin and CSN pin, 164 mV (Typ), V_{IADJ1}, V_{IADJ2} >2.5 V.

For example: R_{SNS} = 0.16 Ω

$$I_{LED} = \frac{0.164}{0.16} = 1.025 A$$

5.8 SPREAD SPECTRUM MODULATION (SSM)

The PT16755 provide a frequency dithering function. It operates at a frequency of ±6 % (Typ) around the frequency f_{SW} set by R_{RT}. The spread spectrum function can be set to ON/OFF by the SSM pin. Connect the SSM pin to GND to enable frequency dither circuit operation, and connect the SSM pin to VCC pin to disable spread spectrum function. Considering a short circuit between the SSM pin and the PDRV pin, it is recommended to insert a pull up resistor or a pull down resistor (47 kΩ or more).

5.9 PWM DIMMING

5.9.1 EXTERNAL P-CH MOSFET DRIVE

The PDRV output is a function of the internal PWM signal and is capable of sinking and sourcing up to 38 mA of peak current to control a high-side series connected P-channel dimming FET. The PDRV switches between V_{CSP} and (V_{CSP} – 8 V) based on the status of PWM signal to completely turn-off and turn-on the external P-channel dimming FET. The series dimming FET is required to achieve high contrast ratio as it ensures fast rise and fall times of the LED current in response to the PWM input. Without any dimming FET, the rise and fall times are limited by the inductor slew rate and the closed-loop bandwidth of the system. Leave the PDRV pin unconnected if not used.

The PDRV output voltage and the CSP voltage have the characteristics shown below figure. When the number of LED lights is small, design and evaluate in consideration of the characteristics shown below figure. There is a possibility that the external P-ch MOSFET cannot be driven.

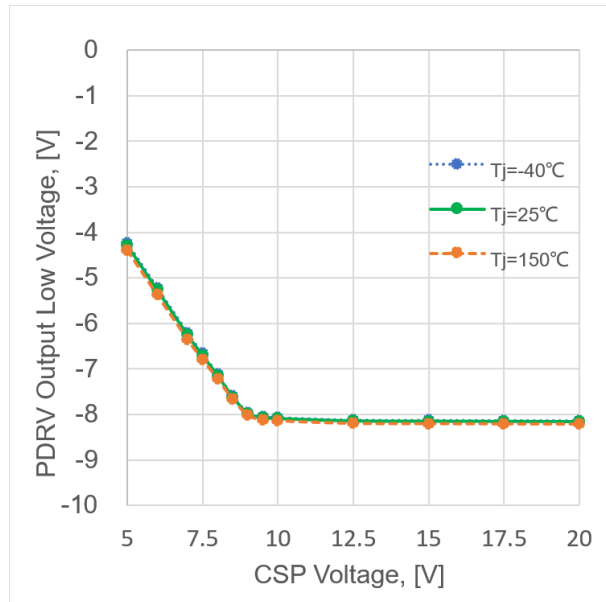


Figure 4 PDRV Output Low Voltage vs CSP Voltage

5.9.2 PWM DIMMING DUTY CYCLE SETTING

The PT16755 has a built-in PWM dimming pulse generation circuit. The PWM dimming duty is set by the internal ramp waveform and the voltage input to the DSET pin. The DSET pin voltage is set from VREF by a resistor voltage divider.

Setting duty D_{PWM} can be calculated by the following formula.

$$D_{PWM} = \frac{V_{DSET} - V_{RAMPB}}{V_{RAMPP} - V_{RAMPB}} \times 100\%$$

V_{RAMPP} : the internal ramp peak voltage, 2.38 V (Typ)

V_{RAMPB} : the internal ramp valley voltage, 0.40 V (Typ)

$$V_{DSET} = \frac{V_{VREF}}{R_{D1} + R_{D2}} \times R_{D2}$$

For example: $R_{D1}=39\text{ k}\Omega$, $R_{D2}=10\text{ k}\Omega$

$$V_{DSET} = \frac{3.0V}{39\text{ k}\Omega + 10\text{ k}\Omega} \times 10\text{ k}\Omega = 0.612\text{ V}$$

$$D_{PWM} = \frac{0.612 - 0.4}{2.38 - 0.4} \times 100\% = 10.7\%$$

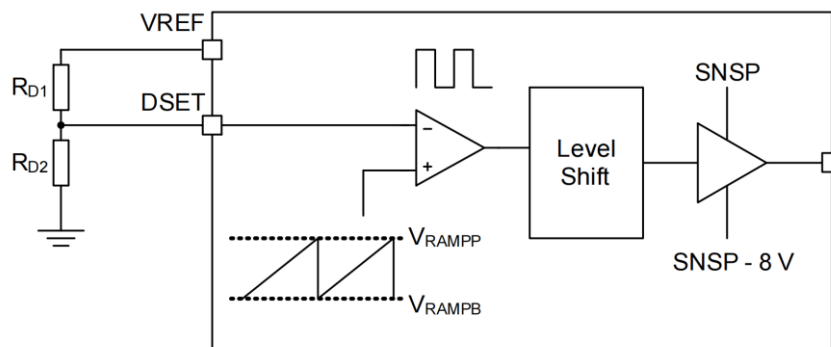


Figure 5 PT16755 Internal PWM Generation Circuit

At UVLO detection, OVP detection, SCP detection (during hiccup operation), TSD detection or EN = Low input, the internal ramp waveform becomes V_{RAMPB} voltage.

5.9.3 DIRECT PWM DIMMING

When the PWMI pin voltage is V_{PWMIH} or more, PT16755 operates at $D_{PWM}=100\%$ duty setting. When the PWMI pin voltage is V_{PWML} or less, it operates at the PWM dimming duty set by the DSET pin. To control PWM dimming with external PWM pulse signal, connect the DSET pin to GND and input the PWM signal to the PWMI pin.

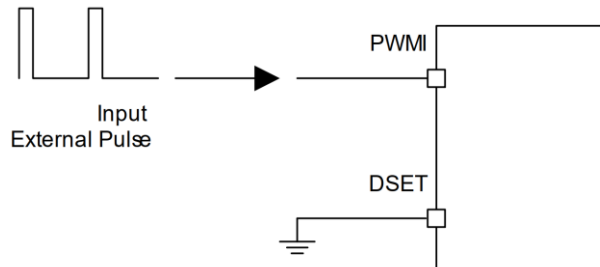


Figure 6 Direct PWM Dimming

5.9.4 DRL MODE (100% DUTY CYCLE)

Switching between PWM dimming mode and DRL mode (100 % Duty cycle) can be done with the input voltage at PWMI pin. When the PWMI pin voltage is V_{PWMIH} or more, it operates at $D_{PWM}=100\%$ duty setting. When the PWMI pin voltage is V_{PWML} or less, it operates at the PWM dimming duty set by the DSET pin.

The PWMI pin is composed of a high-voltage element, it is possible to directly input the battery voltage. The PWMI comparator integrates a 1uA pull down current source to ensure that the pin is not in floating.

Considering the short circuit between the PWMI pin and the VCC pin, it is recommended to insert a limiting resistor R_{PWML} ($\geq 47\text{ k}\Omega$) as shown below figure.

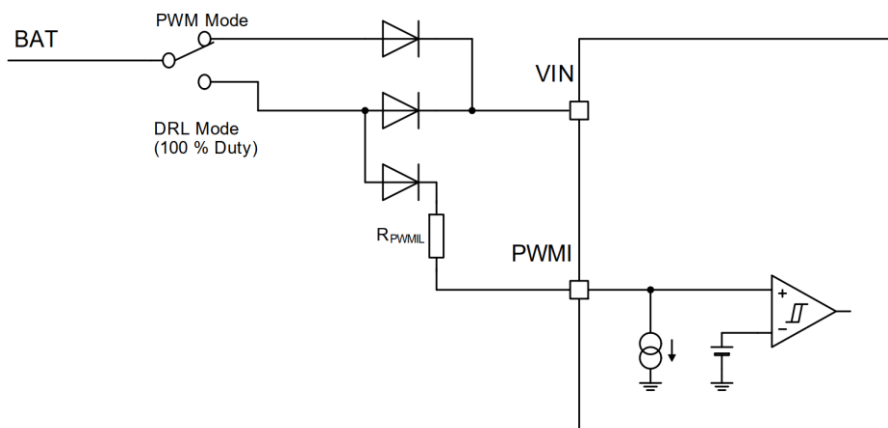


Figure 7 DRL Mode Switching Application

5.10 FAULT PROTECTION

5.10.1 UNDER VOLTAGE LOCK OUT (UVLO)

UVLO is a protection circuit that prevents the device working abnormally at power-on or power-off.

When the VIN pin voltage becomes V_{INUVL} or less or the VCC pin voltage becomes V_{VCCUVL} or less, the PDRV pin outputs high level to turn off external P-ch MOSFET. The device is stopped driving and GDRV outputs low level.

5.10.2 THERMAL SHUTDOWN (TSD)

Internal thermal shutdown circuitry is implemented to protect the controller in the event the maximum junction temperature is exceeded. When activated, typically at 165°C , the controller is forced into a shutdown mode, disabling the internal regulator. This feature is designed to prevent overheating and damage to the device.

A startup sequence is initiated when the junction temperature falls below 145°C. The /FLT pin remains in a high-impedance state when the thermal protection occurs.

5.10.3 OVER CURRENT PROTECTION (OCP)

When the CS pin voltage becomes V_{CSOCP} or more, over current is detected and the GDRV pin outputs Low until the next switching cycle.

The peak inductor current can be calculated as follow:

$$I_{OCP} = \frac{V_{CSOCP}}{R_{CS}} [A]$$

5.10.4 OVER VOLTAGE PROTECTION (OVP)

The PT16755 includes a dedicated OVP pin which can be used for output overvoltage protection. The overvoltage threshold limit is set by a resistor divider network from the output terminal to GND.

When the OVP pin voltage exceeds the reference threshold 1.0V (Typ), the device stops working, the GDRV outputs low level and the PDRV pin outputs high level to turn off the external P-ch MOSFET. /FLT outputs low level and outputs error detection.

The GDRV and PDRV outputs are enabled and a new startup sequence is initiated after the OVP pin voltage drops below the protection is released threshold 0.9V (Typ).

LED open failure can also be detected by the OVP function. When LED is open, OVP is detected again and the OVP detection operation is repeated.

The detection voltage $V_{O(OVP)}$ is set by the following formula:

$$V_{O(OVP)} = 1.0 \times \left(1 + \frac{R_{OVP1}}{R_{OVP2}}\right)$$

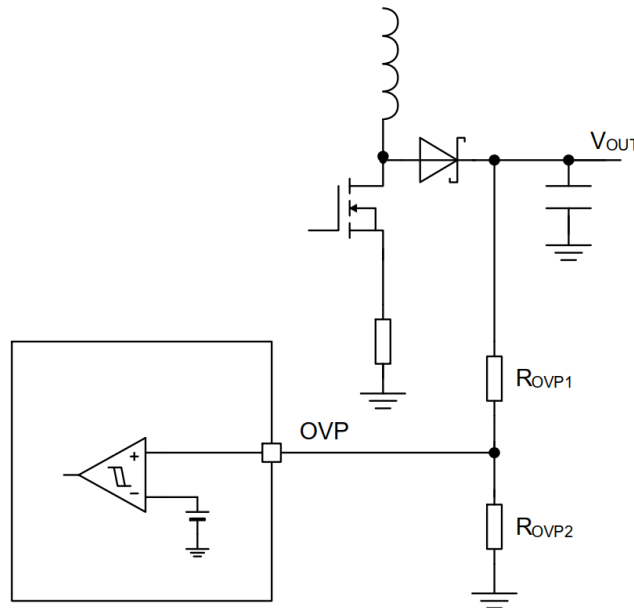


Figure 8 OVP Setting Circuit

When OVP is released and the voltage between the CSP pin and the CSN pin becomes V_{SG} (Status Good Voltage) or more, /FLT outputs high level. /FLT holds low output until t_{FAULT_L} elapses after OVP is released.

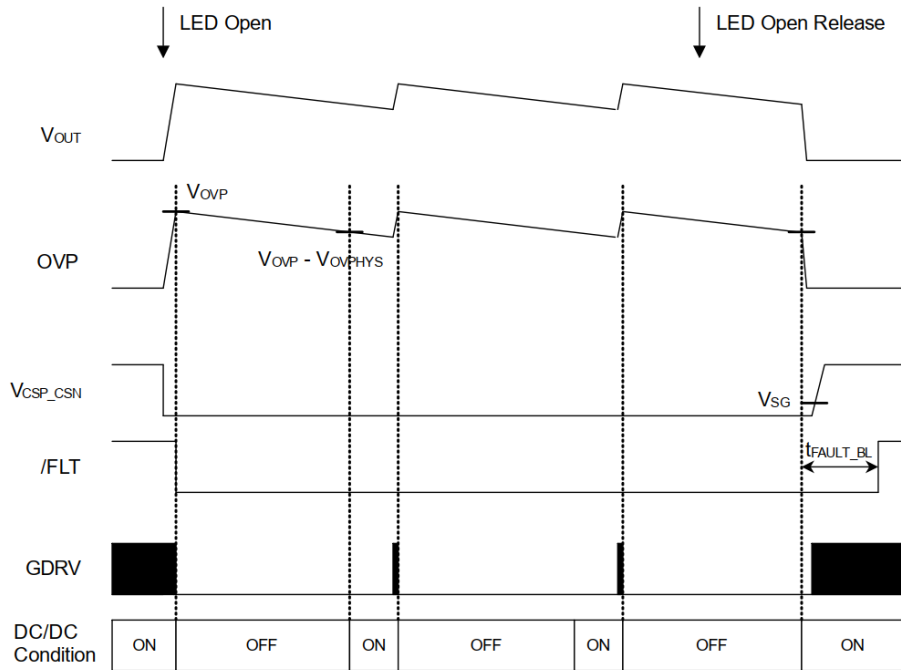


Figure 9 OVP Timing

5.10.5 UNDER VOLTAGE DETECTION (UVD)

When the voltage across the OVP pin and GND falls below 100 mV, /FLT outputs low level. UVD voltage can be set by dividing resistors R_{OVP1} , R_{OVP2} connected between output terminal and GND. The under-voltage fault threshold can be calculated as follow:

$$V_{O(UV)} = 0.1 \times \left(1 + \frac{R_{OVP1}}{R_{OVP2}}\right)$$

UVD is detected when the OVP pin voltage become V_{UVD} or less. UVD is monitored when the voltage between the CSP pin and the CSN pin becomes V_{SG} or more in the ON section of PWM dimming.

After detection the internal counter starts. When the voltage between the CSP pin and the CSN pin becomes V_{SG} or more in the ON section of PWM dimming, it counts up. When the total time reaches t_{UVD} , the /FLT outputs becomes Low.

After UVLO, TSD, SCP, OVP is released or after EN = High input, until t_{UVDIS} has elapsed, UVD does not be detected.

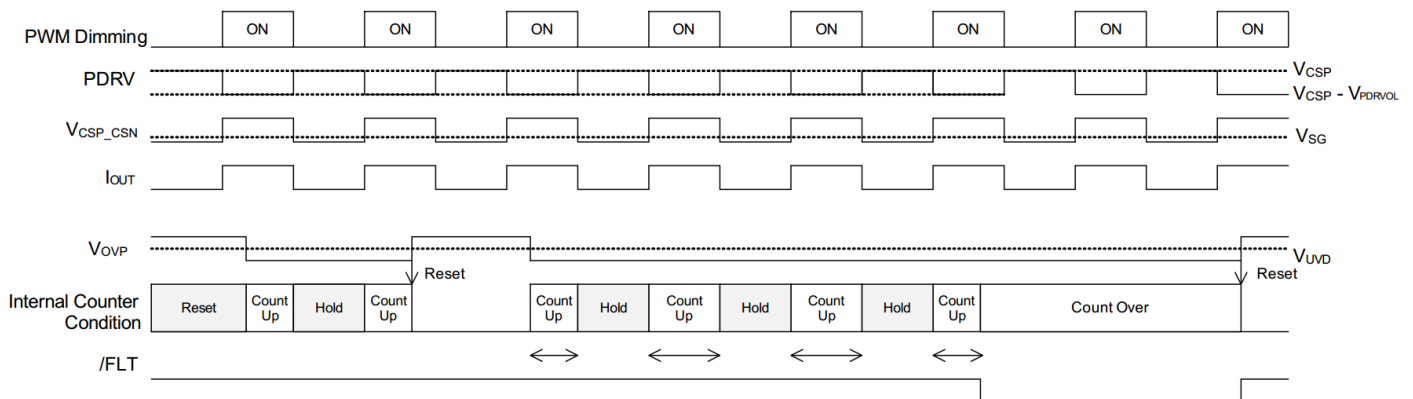


Figure 10 UVD Timing

5.10.6 INTERNAL OVER VOLTAGE PROTECTION (INTOVP)

If the LED opens with the resistor R_{OVP1} open or the OVP pin grounded, the DC/DC is over voltage and the device destroyed. The PT16755 has an internal OVP circuit that monitors the CSP pin voltage and prevents destruction of the device. However, since the threshold value is fixed (V_{INTOVP}), when the absolute voltage of the external parts is low, the parts may be destroyed.

When INTOVP is detected, the PDRV pin outputs High level to turn off the external P-ch MOSFET. The device stops working and GDRV outputs low level. /FLT outputs Low level and outputs error detection. When INTOVP is released and the voltage between the CSP pin and the CSN pin becomes V_{SG} or more, /FLT outputs high level.

/FLT holds low output until t_{FAULT_L} elapses after OVP is released.

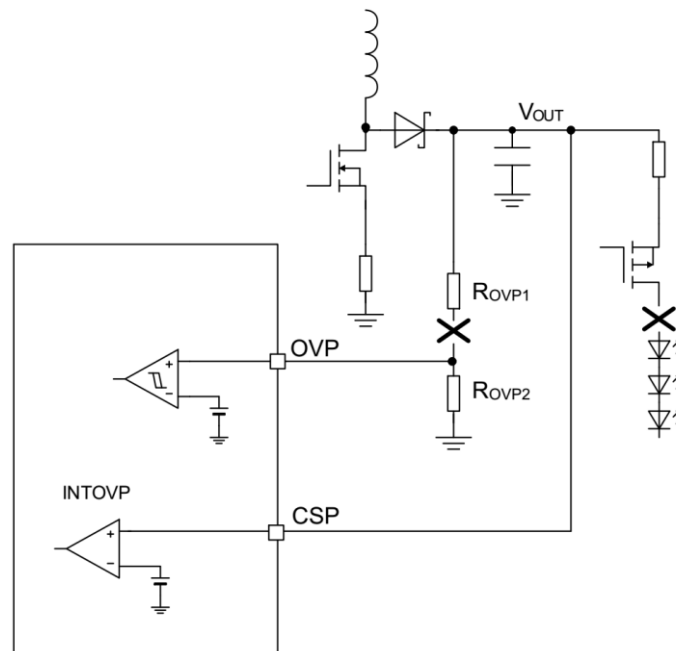


Figure 11 INTOVP Circuit

5.10.7 SHORT CIRCUIT PROTECTION (SCP)

When the anode of the LED is shorted to GND, the voltage between the CSP pin and the CSN pin can be monitored and protected by SCP. When the voltage between the CSP pin and the CSN pin become V_{SCPON} or more, SCP is detected after SCP delay time (t_{SCPDLY}).

When SCP is detected, the PDRV pin outputs High level to turn off the external P-ch MOSFET. The device stops working and GDRV outputs low level. /FLT outputs Low level and outputs error detection.

Restart after hiccup time (t_{HICCUF}) elapses. If the anode of the LED is shorted to GND, the SCP is detected again and the operation is repeated.

/FLT holds Low output until t_{FAULT_L} after restart.

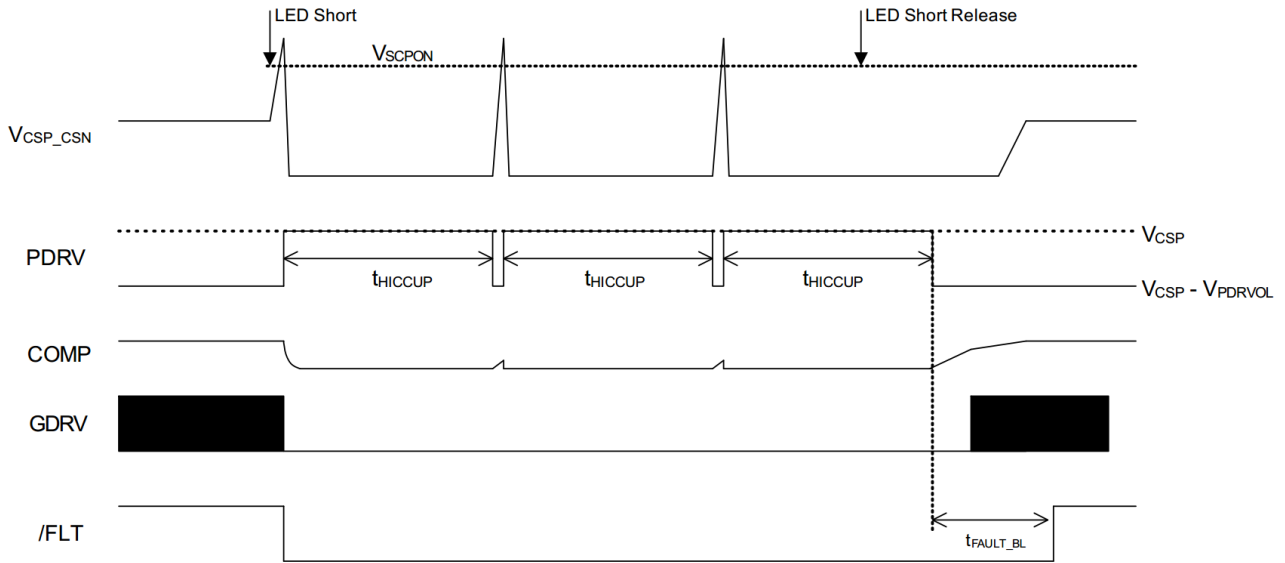


Figure 12 SCP Timing

When the anode of the LED is shorted to GND, the voltage between the CSP pin and the CSN pin may exceed the absolute voltage. It is recommended to insert a PNP transistor as shown below figure and clamp the voltage. Design to take full consideration of power dissipation of R_{SNS} and P-ch MOSFET.

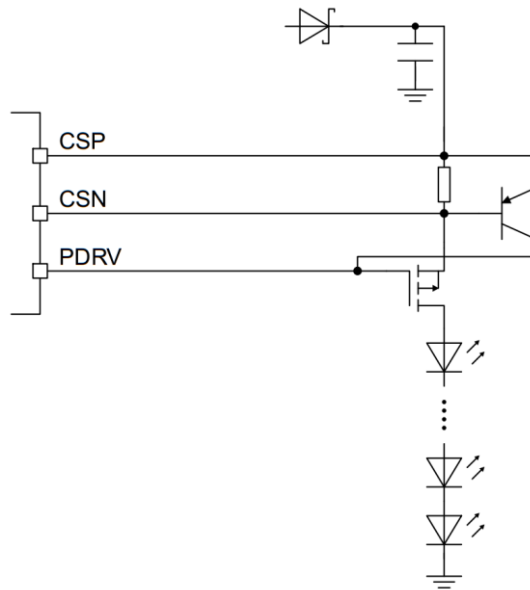


Figure 13 CSP, CSN Clamp Circuit

5.11 FAULT OUTPUT

Fault Description

Protection Function	Operation at Detection			/FLT Output
	DC/DC	PDRV Pin	COMP Pin	
EN = Low	OFF	High (= CSP)	Discharge	Hiz (High-impedance)
VIN UVLO	OFF	High (= CSP)	Discharge	Hiz
VCC UVLO	OFF	High (= CSP)	Discharge	Hiz
TSD	OFF	High (= CSP)	Discharge	Hiz
OCP	OFF	-	-	-
OVP	OFF	High (= CSP)	Discharge	Low
INTOVP	OFF	High (= CSP)	Discharge	Low
UVD	-	-	-	Low (after counting t_{UVB})
SCP	OFF	High (= CSP)	Discharge	Low

6. ABSOLUTE MAXIMUM RATINGS

		MIN	MAX	UNIT
Input	VIN, EN, SSM, PDRV, CSP, CSN, OVP, PWMI	-0.3	70	V
	IADJ1, IADJ2, RT, DSET, CS	-0.3	7	V
Output	VCC, VREF, COMP, GDRV, /FLT	-0.3	7	V
	CSP to PDRV	-0.3	10	V
	CSP to CSN	-0.3	0.6	V
Operating junction temperature, T _J		-40	150	°C
Storage temperature, T _{stg}			150	°C

7. ESD RATINGS

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM)	±2000	V
		Charged-device model (CDM)	±750	

8. RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
VIN	Supply input voltage	5	14	65	V
V _{CSP} , V _{CSN}	Output Voltage	3	-	65	V
f _{PWMI}	PWM dimming frequency	30	-	2000	Hz
t _{MIN}	PWM minimum pulse width	10	-	-	us
f _{SW}	Switching frequency	200	400	1100	kHz
T _A	Operating ambient temperature	-40		125	°C

9. THERMAL INFORMATION

			UNIT
R _{θJA}	Junction-to-ambient thermal resistance	41.6	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	26.8	°C/W
R _{θJB}	Junction-to-board thermal resistance	22.4	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	2.6	°C/W

10. ELECTRICAL CHARACTERISTICS

 $-40^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$, $V_{IN} = 14\text{V}$

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input Voltage						
VIN Input standby current	I _{IN1}	-	380	500	μA	V _{EN} = 0 V, No switching
VIN Input switching current	I _{IN2}	-	1.7	2.3	mA	V _{EN} = 5 V V _{CSP_CSN} > V _{SNS_100%} V _{IADJ1} = V _{IADJ2} = 3.0 V
VIN UVLO falling threshold	V _{INUVDF}	4.1	4.25	4.4	V	VIN falling
VIN UVLO rising threshold	V _{INUVDR}	4.5	4.65	4.8	V	VIN rising
VIN UVLO Hysteresis	V _{INUVHYS}	-	0.4	-	V	V _{INUVDR} - V _{INUVDF}
VCC UVLO falling threshold	V _{VCCUVD}	4.0	4.1	4.2	V	VCC falling
VCC UVLO rising threshold	V _{VCCUVR}	4.3	4.4	4.5	V	VCC rising
VCC UVLO Hysteresis	V _{VCCUVHYS}	-	0.3	-	V	V _{VCCUVR} - V _{VCCUVD}
VCC and VREF Voltage						
VCC Reference voltage	V _{VCC}	4.85	5.0	5.15	V	C _{VCC} = 2.2 μF I _{VCC} = 0 mA to 10 mA load
VCC Drop voltage	V _{VCCDP}	0.15	0.26	0.45	V	V _{IN} = 4.75 V I _{VCC} = 10 mA load
VCC Current limit	I _{VCCLM}	30	45	55	mA	
VREF Reference voltage	V _{VREF}	2.9	3.0	3.1	V	I _{VREF} = 0 mA to 2 mA load
VREF Current limit	I _{VREFLM}	50	70	80	mA	
EN						
EN Pull down current	I _{EN}	0.6	1.1	1.6	μA	V _{EN} = 5 V
EN High level threshold	V _{ENIH}	0.95	1.00	1.05	V	V _{EN} rising
EN Low level threshold	V _{ENIL}	0.85	0.90	0.95	V	V _{EN} falling
EN Hysteresis	V _{ENHYS}	-	0.1	-	V	V _{ENIH} - V _{ENIL}
Oscillator and Spread Spectrum Modulation						
Switching frequency	f _{SW}	270	300	330	kHz	R _{RT} = 33 kΩ
RT Output voltage	V _{RT}	-	0.8	-	V	V _{SSM} = 4 V
Spread spectrum frequency	f _{SSM}	-	f _{sw} /1024	-	Hz	V _{SSM} = 0 V
SSM Frequency range	f _{SSMW}	-	±5	-	%	V _{SSM} = 0 V
SSM High level input voltage	V _{SSMIH}	3.0	-	-	V	SSM disable
SSM Low level input voltage	V _{SSMIL}	-	-	0.4	V	SSM enable
SSM Pull down resistor	R _{SSMD}	200	400	800	kΩ	V _{SSM} = 4 V
GDRV Driver						
GDRV High-side resistance	R _{GDRVH}	1	1.3	2.5	Ω	I _{GDRV} = 10 mA load
GDRV Low-side resistance	R _{GDRVL}	0.7	1	1.4	Ω	I _{GDRV} = 10 mA input
Minimum OFF Time	t _{OFFMIN}	-	90	-	ns	R _{RT} = 33 kΩ

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITIONS
Peak Current Sense (CS)						
CS Current limit threshold	V _{CSOCP}	275	300	321	mV	V _{CS} rising
CS Leading edge blanking time	t _{CSBLK}	-	150	-	ns	
Slope Compensation current	I _{CSLPP}	-	50	-	μA	
CS to COMP Level shift voltage	V _{CSCMPLS}	-	1.26	-	V	
Error Amplifier (COMP)						
Trans conductance	g _M	-	1300	-	μS	V _{CSP_CSN} = 164 mV
COMP Sink current	I _{COMPSSI}	-	220	-	μA	V _{CSP_CSN} = 82 mV V _{IADJ1} = V _{IADJ2} = 0 V
COMP Source current	I _{COMPSSO}	-	220	-	μA	V _{CSP_CSN} = 82 mV V _{IADJ1} = V _{IADJ2} = 3.0 V
Current Sense Amplifier						
LED Current sense voltage, 100 %	V _{SNS_100%}	159	164	169	mV	V _{SNS_100%} = V _{CSP} - V _{CSN} V _{CSN} = 0 V, 30 V V _{IADJ1} = V _{IADJ2} = 2.5 V
LED Current sense voltage, 90 %	V _{SNS_90%}	142	146	150	mV	V _{SNS_90%} = V _{CSP} - V _{CSN} V _{CSN} = 0 V, 30 V V _{IADJ1} = 2.0 V V _{IADJ2} = 2.5 V
LED Current sense voltage, 10 %	V _{SNS_10%}	12.5	15.5	18.5	mV	V _{SNS_10%} = V _{CSP} - V _{CSN} V _{CSN} = 0 V, 30 V V _{IADJ1} = 0.4 V V _{IADJ2} = 2.5 V
Common-mode Input range High-side voltage detection	V _{CSN_HSS}	1.9	2.0	2.1	V	V _{CSN} rising
Common-mode Input range Low-side voltage detection	V _{CSN_LSS}	1.8	1.9	2.0	V	V _{CSN} falling
CSP Input current (High-side)	I _{CSP_HSS}	250	400	650	μA	V _{CSP_CSN} = 164 mV V _{CSN} = 60 V
CSN Input current (High-side)	I _{CSN_HSS}	18	28	38	μA	V _{CSP_CSN} = 164 mV V _{CSN} = 60 V
CSP Input current (Low -side)	I _{CSP_LSS}	-6	-3.5	-1	μA	V _{CSP_CSN} = 164 mV V _{CSN} = 0 V
CSN Input current (Low -side)	I _{CSN_LSS}	-56	-42	-28	μA	V _{CSP_CSN} = 164 mV V _{CSN} = 0 V
Short circuit protection threshold voltage	V _{SCPON}	310	340	370	mV	V _{CSP_CSN} rising
Short circuit protection delay time	t _{SCPDLY}	35	45	55	μs	
Hiccup time	t _{HICcup}	28	38	48	ms	
Over Voltage Protection / Under Voltage Detection						
Over voltage protection detect voltage	V _{OVP}	0.96	1.00	1.04	V	V _{OVP} rising
Over voltage protection detect hysteresis	V _{OVPHYS}	-	0.1	-	V	
Under voltage detection threshold voltage	V _{UVD}	-	100	-	mV	
Internal over voltage protection detect voltage	V _{INTOVP}	65		-	V	V _{CSP} monitor

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITIONS
PWM Dimming						
PWM Dimming frequency	f _{PWM}	320	400	480	Hz	
Ramp signal valley	V _{RAMPB}	0.38	0.4	0.42	V	
Ramp signal peak	V _{RAMPP}	2.34	2.38	2.42	V	
DSET Input current	I _{DSET}	-	0.1	1	μA	V _{DSET} = 3.0 V
PDRV Pull up ON resistor	R _{PDRV_U}	-	22	50	Ω	I _{PDRV} = 10 mA load V _{CSP} = 30 V V _{DSET} = 0 V, V _{PWMI} = 0 V
PDRV Pull down current	I _{PDRV_D}	28	38	48	mA	V _{CSP_PDRV} = 0 V, V _{CSP} = 30 V V _{DSET} = 5 V, V _{PWMI} = 0 V
PDRV Output low voltage	V _{PDRVOL}	7	8	9	V	V _{CSP_PDRV} , V _{CSP} = 30 V
DRL Mode						
DRL Mode PWMI Input threshold	V _{DRLIH}	1.42	1.50	1.58	V	V _{PWMI} rising
PWM Mode PWMI Input threshold	V _{DRLIL}	0.95	1.00	1.05	V	V _{PWMI} falling
DRL/PWMI Hysteresis voltage	V _{DRLIHYS}	-	0.5	-	V	V _{DRLIH} - V _{DRLIL}
PWMI Pull Down Current	I _{PWMI}	0.5	1.0	2.0	μA	V _{PWMI} = 5 V
Analog Dimming						
IADJ1, IADJ2 I _{LED} =0% Threshold	V _{IADJ_0%}	0.17	0.22	0.26	V	
IADJ1, IADJ2 I _{LED} =100% Threshold	V _{IADJ_100%}	2.10	2.18	2.26	V	
IADJ1, IADJ2 Input current	I _{IADJ}	-	0.1	1	μA	V _{IADJ1} = V _{IADJ2} = 3.0 V
Fault Indicator (/FLT)						
/FLT Output low voltage	V _{FAULT_OL}	-	0.1	0.4	V	I _{/FLT} = 5 mA input
/FLT Leak current	I _{FAULT}	-	0	1	μA	V _{/FLT} = 5.5 V
Under Voltage detection time	t _{UVD}	16	20	24	ms	
Under Voltage detection disable time	t _{UVDIS}	30	38	46	ms	EN = Low to High VIN UVLO or VCC UVLO or TSD release
/FLT Holds low output	t _{FAULT_L}	16	20	24	ms	SCP or OVP release
Status Good voltage	V _{SG}	18	23	28	mV	V _{CSP_CSN} rising
THERMAL SHUTDOWN						
Thermal shutdown temperature	T _{SD}	-	165	-	°C	
Thermal shutdown hysteresis	T _{SD(HYS)}	-	20	-	°C	

11. TYPICAL PERFORMANCE CURVES

(Unless otherwise specified $V_{IN} = 13\text{ V}$, $T_j = +25\text{ }^\circ\text{C}$)

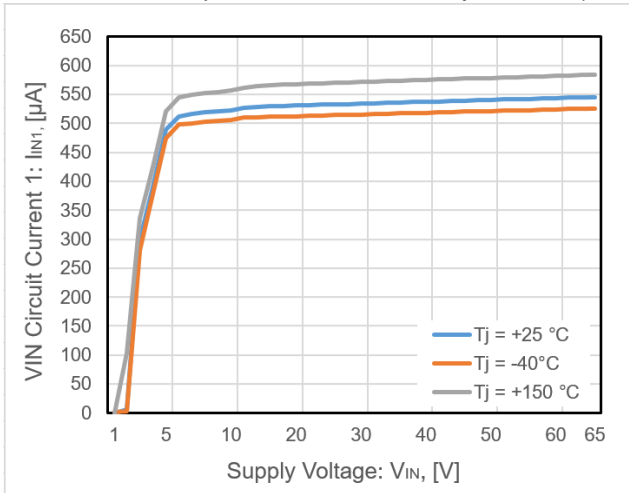


Figure 14. VIN Circuit Current 1 vs Supply Voltage

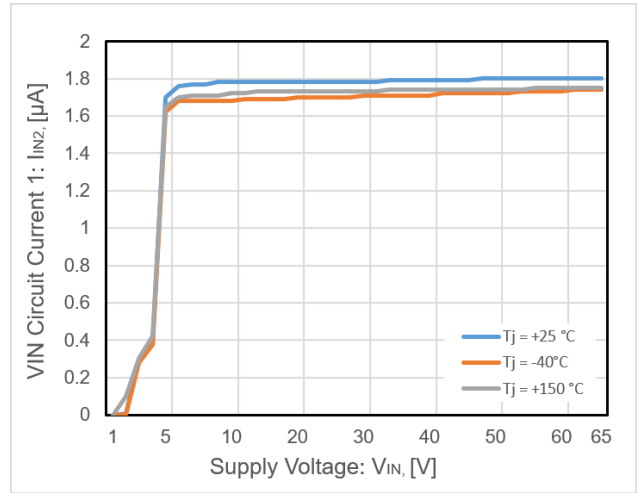


Figure 15. VIN Circuit Current 2 vs Supply Voltage

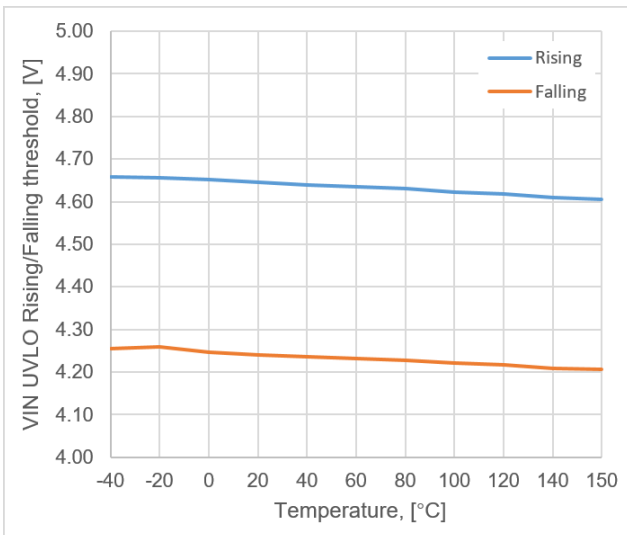


Figure 16. VIN UVLO Rising/Falling threshold vs Temperature

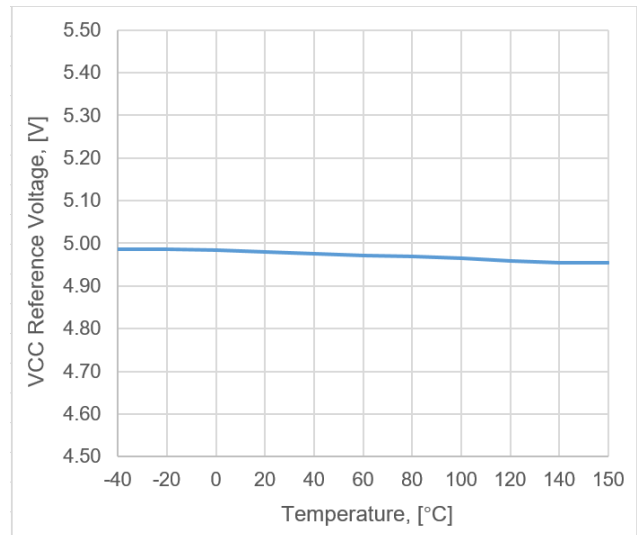


Figure 17. VCC Reference Voltage vs Temperature

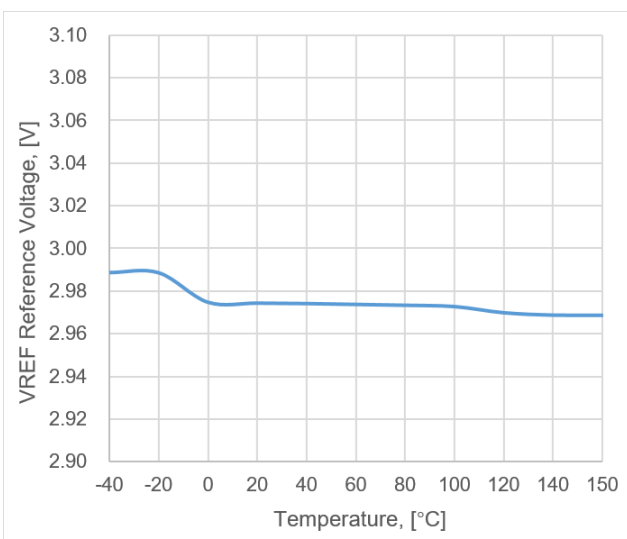


Figure 18. VREF Reference Voltage vs Temperature
($I_{VREF} = 0\text{ mA to }2\text{ mA load}$)

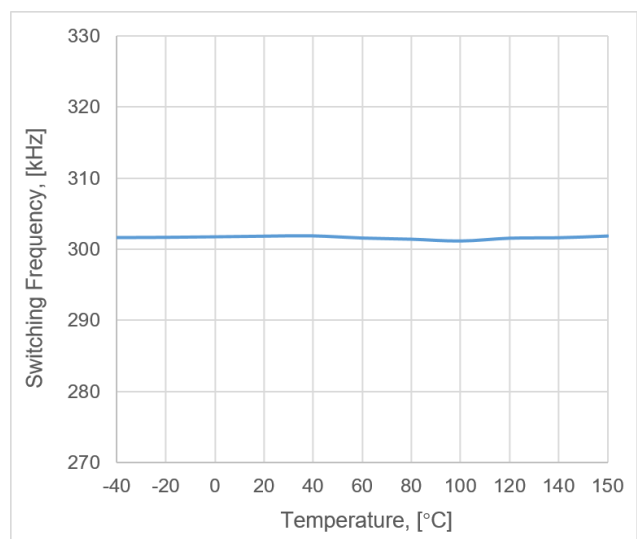


Figure 19. Switching Frequency vs Temperature

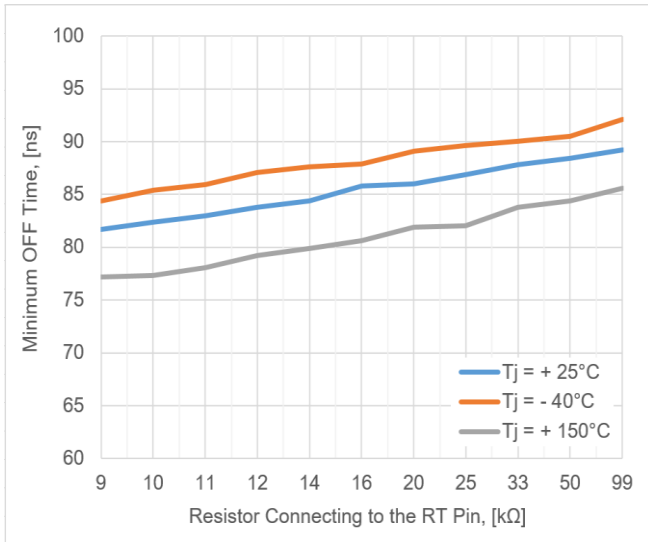


Figure 20. Minimum OFF Time vs RT Resistor

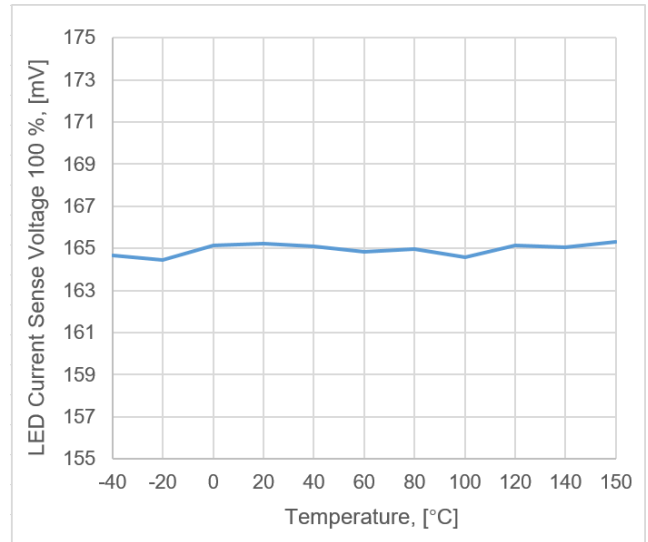


Figure 21. LED Current Sense Voltage vs temperature
 $V_{SNS_100\%}$, ($V_{IADJ1} = V_{IADJ2} = 2.5\text{ V}$)

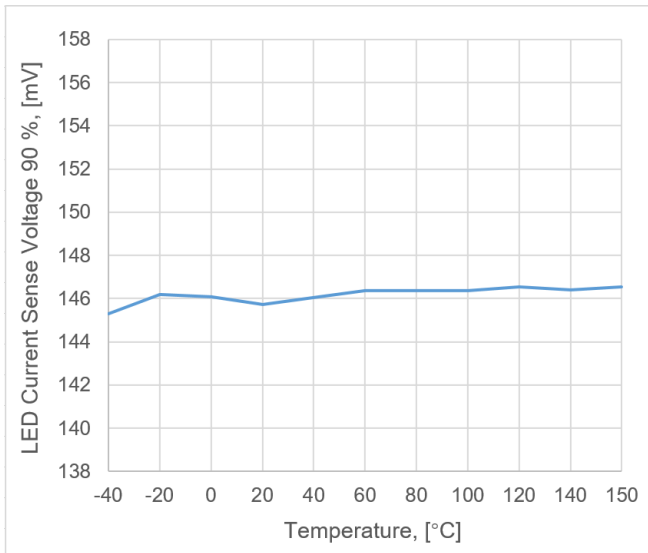


Figure 22. LED Current Sense Voltage vs temperature
 $V_{SNS_90\%}$, ($V_{IADJ1} = 2.0\text{ V}$, $V_{IADJ2} = 2.5\text{ V}$)

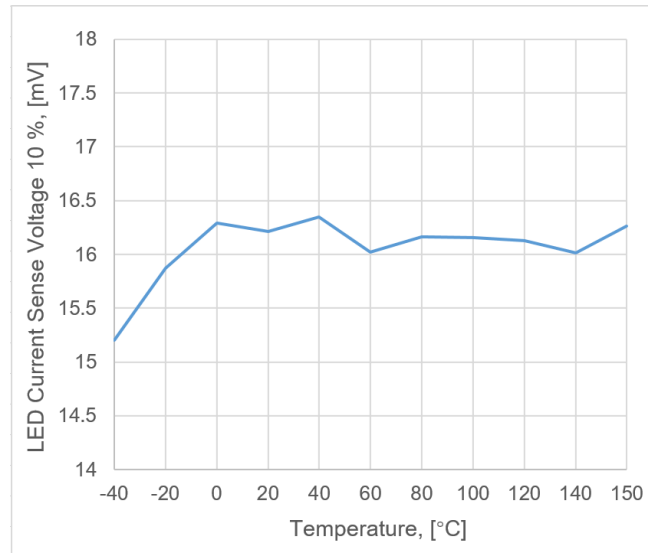


Figure 23. LED Current Sense Voltage vs temperature
 $V_{SNS_10\%}$, ($V_{IADJ1} = 0.4\text{ V}$, $V_{IADJ2} = 2.5\text{ V}$)

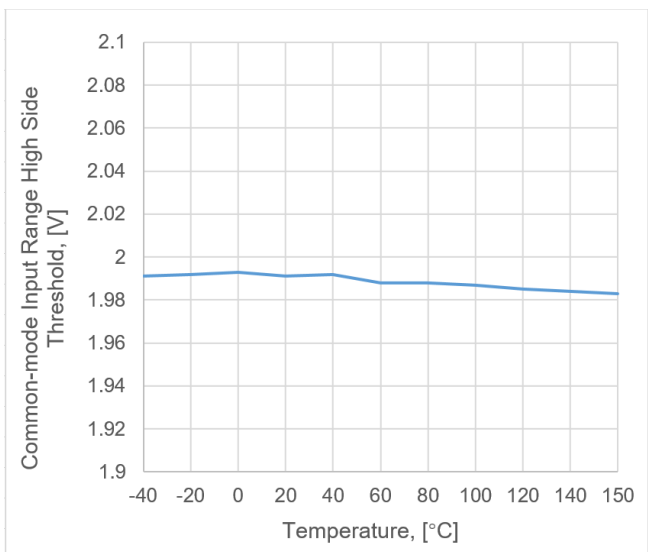


Figure 24. Common-mode Input Range High Side Voltage Detection vs Temperature

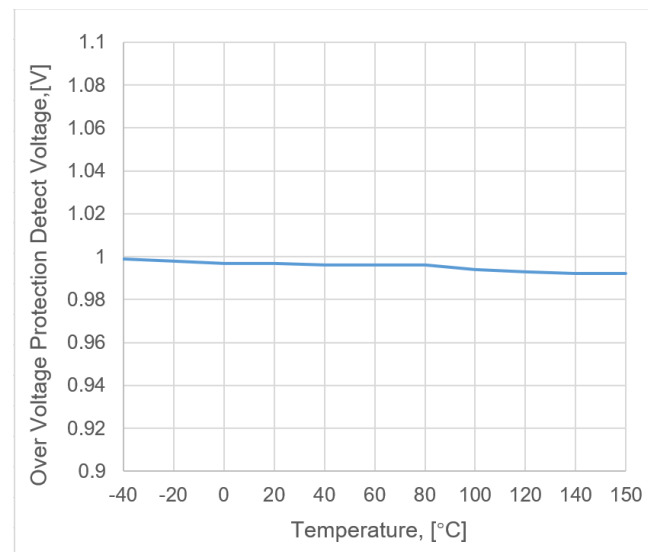


Figure 25. Over Voltage Protection Detect Voltage vs Temperature

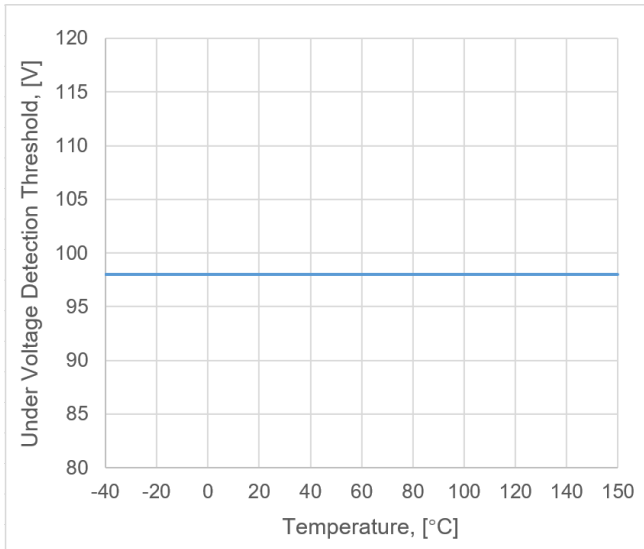


Figure 26. Under Voltage Detection Threshold Voltage vs Temperature

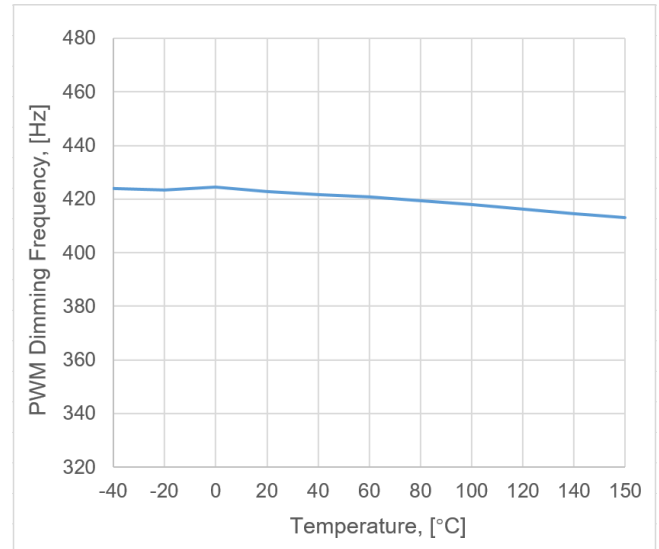


Figure 27. PWM Dimming Frequency vs Temperature

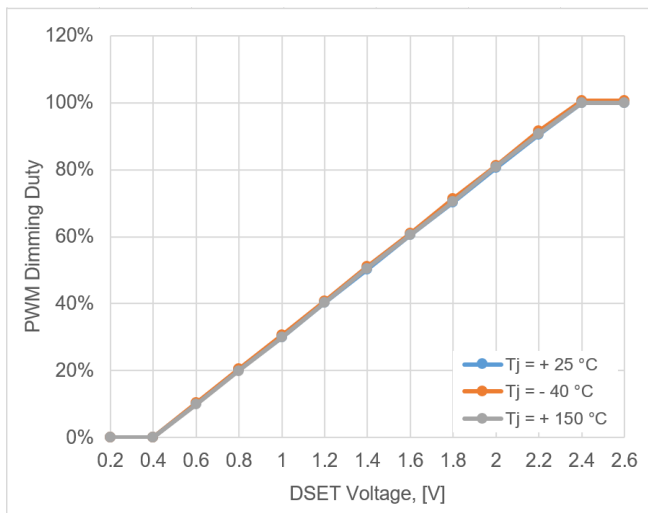


Figure 28. PWM Dimming Duty vs DSET Voltage

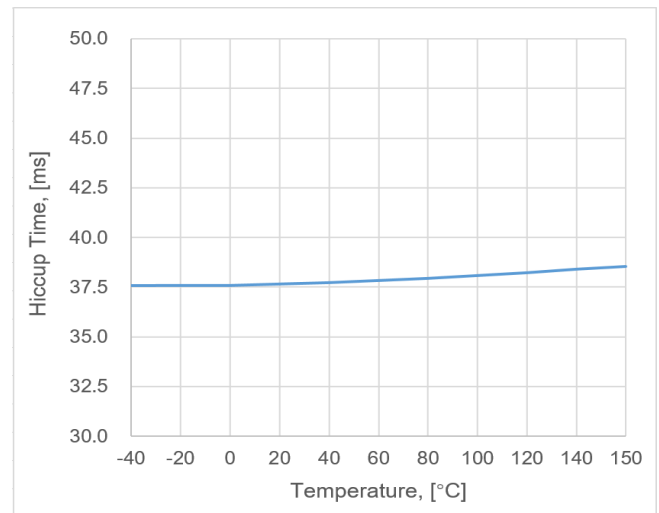


Figure 29. Hiccup Time vs Temperature

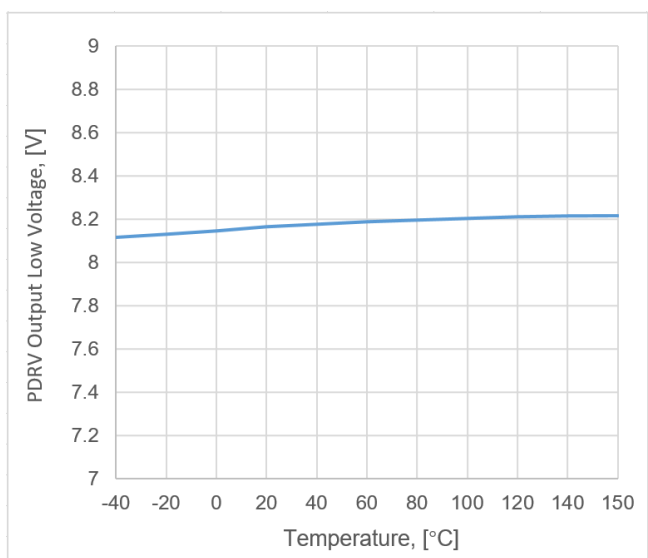


Figure 30. PDRV Output Low Voltage vs Temperature

12. DESIGN GUIDE

APPLICATION CIRCUIT

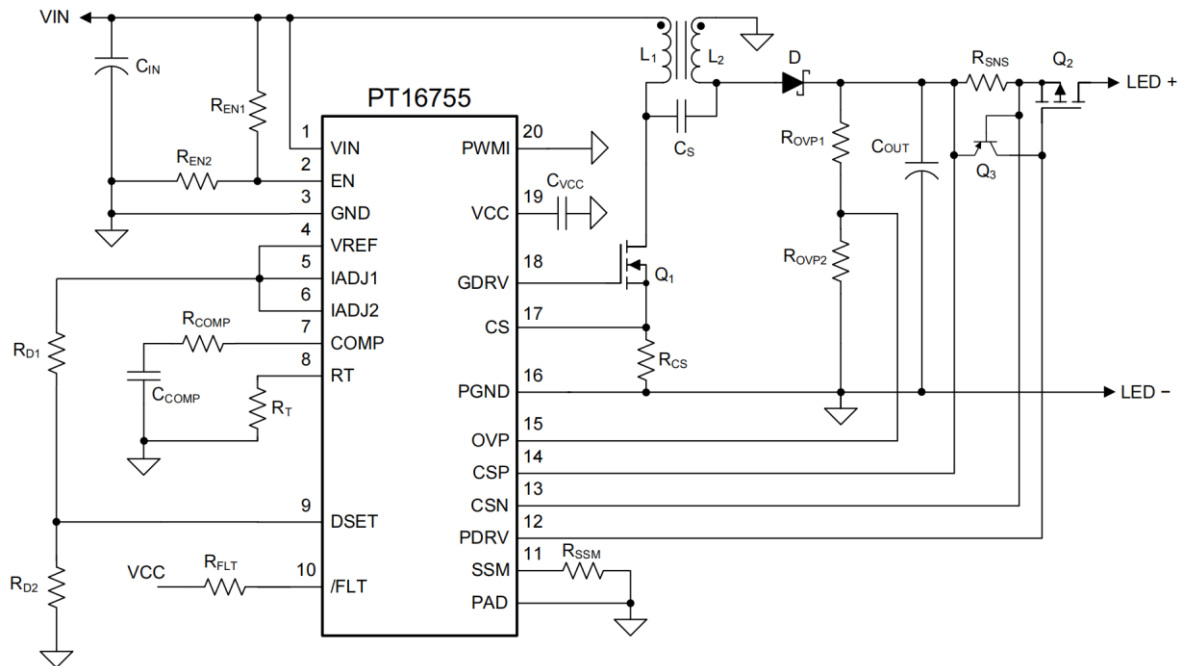


Figure 31. SEPIC LED Driver

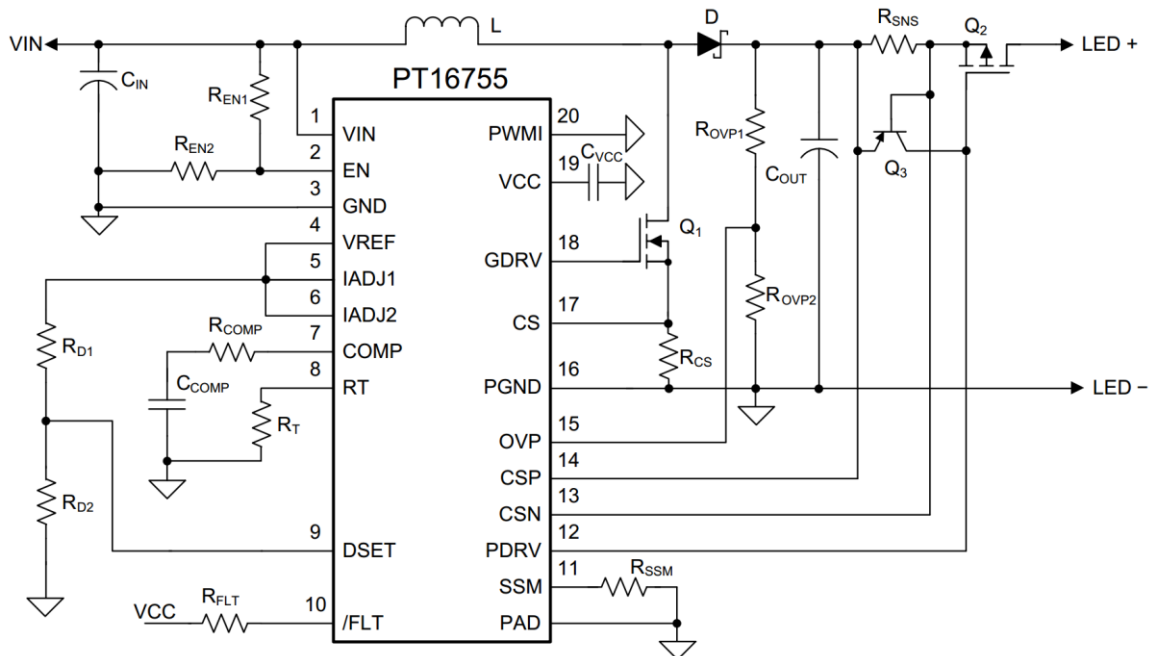


Figure 32. BOOST LED Driver

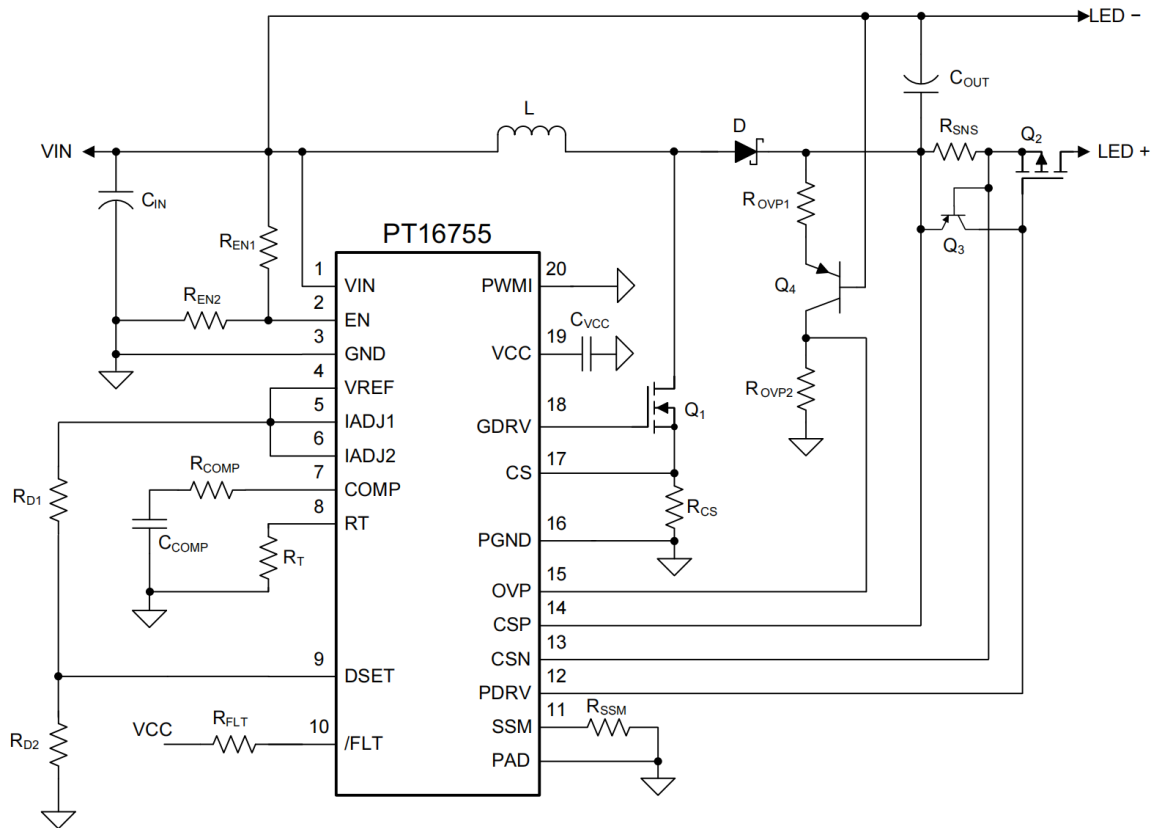


Figure 33. Buck-Boost LED Driver

DESIGN PROCEDURE

1) Duty Cycle Calculation

The switching duty cycle (D) defines the converter operation, and is related to the input and output voltages. In steady state, the duty cycle is calculated using following expression:

Buck:	Boost:	SEPIC/Buck-Boost:
$D = \frac{V_O}{V_{IN}}$	$D = \frac{V_O - V_{IN}}{V_O}$	$D = \frac{V_O}{V_O + V_{IN}}$
$D_{MIN} = \frac{V_O}{V_{IN(MAX)}}$	$D_{MIN} = \frac{V_O - V_{IN(MAX)}}{V_O}$	$D_{MIN} = \frac{V_O}{V_O + V_{IN(MAX)}}$
$D_{MAX} = \frac{V_O}{V_{IN(MIN)}}$	$D_{MAX} = \frac{V_O - V_{IN(MIN)}}{V_O}$	$D_{MAX} = \frac{V_O}{V_O + V_{IN(MIN)}}$

The duty cycle must be within the operating range of the controller to ensure that the closed-loop LED current regulation is in the specified input and output voltage range.

2) LED Output Current Calculation

The LED current is set by the current sense resistor, R_{SNS} , and the analog adjust voltage, V_{IADJ1} or V_{IADJ2} (which is lower). The current sense resistor is placed in series with the LED load. The CSP and CSN inputs of the internal rail-to-rail current sense amplifier are connected to the R_{SNS} resistor to achieve closed-loop regulation. When ($V_{IADJ1} = V_{IADJ1}$) > 2.2V, the internal reference clamps the $V_{(CSP-CSN)}$ to 0.164V, the LED current is set by flowing equation:

$$I_{LED} = \frac{0.164}{R_{CS}}$$

The LED current can be programmed by varying $V_{IADJ1(2)}$ between 200mV to 2.2V. The LED current can be calculated using:

$$I_{LED} = \frac{V_{IADJ1(2)} - 0.2}{12 \times R_{SNS}}$$

3) Switching Frequency Setting

The switching frequency of the DC/DC can be set by the resistor R_{RT} connected to the RT pin. For example: Switching Frequency = 400 kHz

$$R_T = \frac{9900 \times 10^3}{f_{sw}} \text{ (K}\Omega\text{)} = \frac{9900 \times 10^3}{400 \times 10^3} = 24.75 \text{ (K}\Omega\text{)}$$

4) Inductance Calculation

Consider a good compromise between core loss and copper loss of the inductor, the inductor peak-to-peak ripple current, Δi_{L-PP} , is typically set between 20% and 80% of the maximum inductor current, I_L . Higher ripple inductor current allows a smaller inductor size, but needs more capacitors on the output to smooth the LED current ripple. Knowing the desired ripple ratio RR , switching frequency f_{sw} , maximum duty cycle D_{MAX} , and the typical LED current I_{LED} , the inductor value can be calculated as follows:

Buck:

$$\begin{aligned} \Delta i_{L(PP)} &= RR \times I_L = RR \times I_{LED} \\ L &= \frac{(V_{IN(MIN)} - V_O) \times D_{MAX}}{\Delta i_{L(PP)} \times f_{sw}} \times 10^6 \text{ (uH)} \\ I_{L_{AV}} &= I_{LED} \end{aligned}$$

Boost and Buck-Boost (SEPIC):

$$\begin{aligned} \Delta i_{L(PP)} &= RR \times I_L = RR \times \frac{I_{LED}}{1 - D_{MAX}} \\ L &= \frac{V_{IN(MIN)} \times D_{MAX}}{\Delta i_{L(PP)} \times f_{sw}} \times 10^6 \text{ (uH)} \\ I_{L_{AV_MAX}} &= \frac{I_{LED}}{1 - D_{MAX}} \end{aligned}$$

Select inductor with saturation current rating greater than the peak inductor current, $I_{L(PK)}$, at the maximum operating temperature.

$$I_{L(PK)} = I_{L_{AV_MAX}} + \frac{1}{2} \times \Delta i_{L(PP)}$$

5) Over Current Protection Setting

Select R_{CS} (resistance for over current detection) to realize below. Set a sufficient margin in consideration of the variation of the inductor.

$$I_{OCP_MIN} = \frac{V_{CSOCP_MIN}}{R_{CS}} > I_{L(PK)}$$

Where:

I_{OCP_MIN} is the minimum over current detection current.

V_{CSOCP_MIN} is the minimum over current detection voltage, 0.275V.

As power voltage varies, the switching may become unstable due to sub-harmonic oscillation, and the LED may flicker. The condition can be eased by adding R_{SLP} . However, be aware that adding R_{SLP} will also change OCP detection (I_{OCP}) level. The formula for calculating the OCP detection level (I_{OCP}) when R_{SLP} is added is as follows.

$$I_{OCP_MIN} = \frac{(V_{CSOCP_MIN} - \frac{1.06}{R_{RT}} \times \frac{1.2 \times 10^{-6}}{f_{sw}} \times \frac{D_{MAX}}{f_{sw}} \times R_{SLP})}{R_{CS}}$$

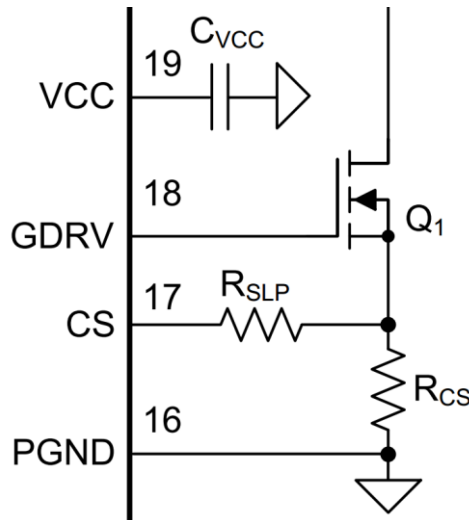


Figure 34 CS pin Slope Compensation Application

6) Input Capacitor Value Calculation

The input capacitors, C_{IN} , smooth the input voltage ripple and store energy to supply input current during input voltage drop or PWM dimming transients. In the Boost and SEPIC topology, the series inductor provides continuous input current so that requires a smaller input capacitor to achieve desired input ripple voltage, $\Delta v_{IN(PP)}$.

The Buck and Buck-Boost topology have discontinuous input current, and larger capacitors are required to achieve the same input voltage ripple. Based on the switching frequency, f_{SW} , and the maximum duty cycle, D_{MAX} , the input capacitor value can be calculated as follows:

Buck:

$$C_{IN} = \frac{I_{LED} \times D_{MAX} \times (1 - D_{MAX})}{f_{SW} \times \Delta v_{IN(PP)}}$$

Boost:

$$C_{IN} = \frac{\Delta i_{L(PP)}}{8 \times f_{SW} \times \Delta v_{IN(PP)}}$$

Buck-Boost:

$$C_{IN} = \frac{I_{LED} \times D_{MAX}}{f_{SW} \times \Delta v_{IN(PP)}}$$

For most applications, it highly recommends to select X7R dielectric-based ceramic capacitors due to their low ESR, high ripple current rating, and good temperature performance. For PWM dimming application, aluminum electrolytic capacitor and ceramic capacitor are recommended to minimize the voltage deviation due to large input current transients generated in conjunction with the rising and falling edges of the LED current.

7) Output Capacitor Value Calculation

Using the output capacitors to attenuate the discontinuous or large ripple current generated by switching and achieve the desired LED output current ripple, $\Delta i_{LED(PP)}$. The capacitor value depends on the total series resistance of the LED string, r_D and the switching frequency, f_{SW} . The capacitance required for the target LED ripple current can be calculated based on following equations.

Buck:

$$C_{OUT} = \frac{\Delta i_{L(PP)}}{8 \times f_{SW} \times r_D \times \Delta i_{LED(PP)}}$$

Boost and Buck-Boost:

$$C_{OUT} = \frac{I_{LED} \times D_{MAX}}{f_{SW} \times r_D \times \Delta i_{LED(PP)}}$$

For the Buck topology, the inductor is in series with LED load and requires a smaller capacitor than the Boost, Buck-Boost, and SEPIC topologies to achieve the same LED ripple current.

The ESR and the ESL characteristics must be considered when selecting the output capacitors, as they directly impact the LED current ripple. Ceramic capacitors are the best choice because of its low ESR, high ripple current

rating, long lifetime, and good temperature performance. When selecting ceramic capacitors, it is important to consider the derating factors associated with higher temperature and DC bias operating conditions. It is recommended to use X7R dielectric with rated voltage greater than the maximum LED voltage. Aluminum electrolytic capacitors can be used in parallel with ceramic capacitors to provide large capacity energy storage. The aluminum capacitors must have the necessary RMS current and temperature ratings to ensure extended operating lifetime. The minimum allowable output capacitor RMS current rating, $I_{COUT(RMS)}$, can be approximated:
Buck:

$$I_{COUT(RMS)} = \frac{\Delta i_{LED(PP)}}{\sqrt{12}}$$

Boost and Buck-Boost:

$$I_{COUT(RMS)} = I_{LED} \times \sqrt{\frac{D_{MAX}}{1 - D_{MAX}}}$$

For applications that need to support different LED string configurations with a wide range of programmable LED current set points, rearrange the previous expressions based on the maximum output power to reflect output capacitance, to ensure that LED current ripple meets the requirements over the entire range of operation.

8) Main Power MOSFET Selection

The power MOSFET should be able to endure the maximum switch node voltage, V_{SW} , and switch RMS current derived based on the converter topology. In order to ensure safe operation, the drain voltage V_{DS} is at least 20% greater than the maximum switch node voltage. The MOSFET Drain-Source breakdown voltage, V_{DS} , and RMS current ratings are calculated using the following expressions.

Buck:

$$V_{DS} = V_{IN(MAX)} \times 1.2$$

$$I_{Q(RMS)} = I_{LED} \times \sqrt{D_{MAX}}$$

Boost:

$$V_{DS} = V_{O(OVP)} \times 1.2$$

$$I_{Q(RMS)} = I_{LED} \times \frac{\sqrt{D_{MAX}}}{1 - D_{MAX}}$$

Buck-Boost:

$$V_{DS} = (V_{IN(MAX)} + V_{O(OVP)}) \times 1.2$$

$$I_{Q(RMS)} = I_{LED} \times \frac{\sqrt{D_{MAX}}}{1 - D_{MAX}}$$

Where the voltage, $V_{O(OVP)}$, is the overvoltage protection threshold and the worst-case output voltage under fault conditions.

A MOSFET with low total gate charge, Q_g is selected to minimize gate drive and switching losses. The R_{DS} resistance of MOSFET is usually an unimportant parameter because the switch conduction losses are not a significant part of the total converter losses at high operation frequency. The switching and conduction losses are calculated as follows:

$$P_{COND} = R_{DS} \times I_{Q(RMS)}^2$$

$$P_{SW} = \frac{(t_R + t_F)}{2} \times f_{SW} \times V_{OUT} \times I_{L(AV)}$$

t_R , t_F are the rise time and fall time of the main power mosfet drain-source.

The MOSFET power rating and package should be selected based on the total calculated loss, the ambient operating temperature, and maximum allowable temperature rise.

9) Rectifier Diode Selection

It suggests that use a Schottky diode as rectifier diode, because it provides the best efficiency due to the low forward voltage drop and near-zero reverse recovery time. Choose a diode with a reverse breakdown voltage, $V_{D(BR)}$, greater than or equal to MOSFET drain-to-source voltage, V_{DS} , for reliable performance. It is important to understand the leakage current characteristics of the Schottky diode, especially at high operating temperatures because it impacts the overall converter operation and efficiency.

The current through the diode, I_D , is given by:

$$I_D = I_{LED(MAX)}$$

The diode power rating and package is selected based on the calculated current, the ambient temperature and the maximum allowable temperature rise.

10) Feedback Compensation

Concerning stability condition of application.

Stability condition for system with negative feedback is as shown below.

Phase-lag when gain is 1 (0 dB) is no more than 150° (namely, phase margin is 30° or more).

Further, since DC/DC converter application is sampled by switching frequency, GBW of the entire system is set to be 1/10 or less of switching frequency. To wrap up, target characteristics of application are as shown below.

Phase-lag when gain is 1 (0 dB) is 150° or less (namely, phase margin is 30° or more).

GBW at the time (namely, frequency when gain is 0 dB) is 1/10 or less of switching frequency. Therefore, in order to raise responsiveness by limiting GBW, higher switching frequency is required.

Phase margin: 60° or more.

GBW: 1/20 or less of switching frequency is recommended.

The knack for securing stability feedback compensation is to insert phase-lead f_{z1} near GBW. GBW is determined by C_{OUT} and phase-lag f_p due to output impedance $R_L (= V_{OUT} / I_{LED})$.

They are shown in the following formulae.

$$f_{z1} = \frac{1}{2\pi \times C_{comp} \times R_{comp}}$$

$$f_p = \frac{1}{2\pi \times R_L \times C_{OUT}}$$

As described above, secure phase margin. For R_L value at max load should be inserted. In addition, with boost DC/DC, right half plane zero (RHP zero) is to be considered. This zero has a characteristic of zero as a gain and as the pole with phase. Because it causes an oscillation when this zero effects on a control loop, it is necessary to bring GBW just before RHP zero. RHP zero f_{z2} can be calculated with an equation below and shows good characteristic by setting GBW to be lower than 1/10 of RHP zero or less.

$$f_{z2} = \frac{R_L \times \left(\frac{V_{IN}}{V_{OUT}}\right)^2}{2\pi \times L}$$

Particularly when supply voltage rises and gets close to output voltage, the switching output becomes irregular and ripple of the output voltage increases. Ripple of the LED current may thereby get bigger.

Since this setting is obtained by simplified, not strict, calculation, adjustment by actual equipment may be required in some cases. Further, since these characteristics will vary depending upon substrate layout, load condition, etc., confirm satisfactorily with actual equipment when planning mass production.

11) Overvoltage and Under-Voltage Protection

The controller includes a dedicated OVP pin which can be used for output overvoltage protection.

For Boost and SEPIC topologies, the overvoltage threshold is programmed using a resistor divider, R_{OVP1} and R_{OVP2} , from the output voltage (V_O) to GND.

In the Buck-Boost or Buck configuration, if the LEDs are referenced to a potential other than ground, the output voltage is sensed and translated to ground by using a PNP transistor and level-shift resistors.

The overvoltage turn-off threshold, $V_{O(OVP)}$, is:

SEPIC and Boost:

$$V_{O(OVP)} = V_{OVP} \times \left(\frac{R_{OVP1} + R_{OVP2}}{R_{OVP2}} \right)$$

Buck-Boost:

$$V_{O(OVP)} = V_{OVP} \times \frac{R_{OVP1}}{R_{OVP2}} + 0.7$$

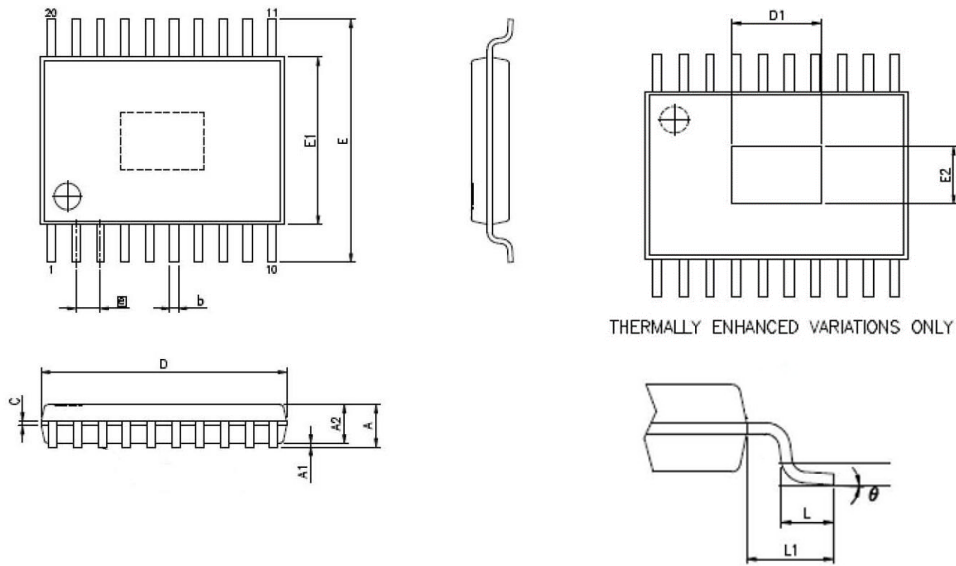
The corresponding under-voltage fault threshold, $V_{O(UV)}$ is:

$$V_{O(UV)} = 0.1 \times \left(\frac{R_{OVP1} + R_{OVP2}}{R_{OVP2}} \right)$$

12) About PCB layout

1. Locate the decoupling capacitor of C_{VIN} , C_{VCC} close to the pins as much as possible.
2. R_{RT} locates it close to the RT pin.
3. Because high current may flow in PGND, lower impedance.
4. Prevent noise to be applied to the EN, VREF, COMP, RT, IAJD1, IADJ2, DSET, OVP, CSP and CSN pins.
5. As the GDRV, CS, PDRV pins are switching, be careful not to affect the neighboring patterns.
6. For noise reduction, PGND of R_{CS} and PGND of C_{OUT} recommend to have one common grounds. In addition, consider the PCB layout so that the current path of $Q1 \rightarrow R_{CS}$, $R_{CS} \rightarrow PGND$ and the current path of $Q1 \rightarrow D \rightarrow C_{OUT} \rightarrow PGND$ are the shortest and with the lowest impedance on the same surface without vias etc.

13. PACKAGE INFORMATION



Refer to JEDEC MO-153 ACT

Symbol	Dimensions		
	Min.	Nom.	Max.
A	—	—	1.20
A1	0.05	—	0.15
A2	0.80	1.00	1.05
b	0.19	—	0.30
c	0.09	—	0.20
e	0.65 BSC		
D	6.40	6.50	6.60
D1	—	3.99	—
E	6.40 BSC		
E1	4.30	4.40	4.50
E2	—	2.8	—
S	0.2	—	—
L	0.5	0.60	0.75
L1	1.00 REF		
θ	0°	—	8°

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