

DESCRIPTION

The PT16940 is a serial-in parallel-out controlled LED driver with 35V output voltage rating. With the input of 3-line serial data, it turns the 12ch open drain output on/off. Due to its compact size, it is optimal for small space.

FEATURES

- Open Drain Output.
- 3-line Serial Control + Enable Signal.
- Cascade Connection Compatible.
- TSSOP-20 Package.
- Internal 12ch Power Transistor.
- AEC-Q100 Qualified.
- Output Slew Rate Typical 20V/μs .
(for Low EMC Noise)

KEY SPECIFICATIONS

- Input voltage range: 3.0V to 5.5V
- Output voltage range: 35V (Max.)
- DC Output Current (per CH): 50mA(Max.)
- Output ON Resistance: 6Ω(Typ.)
- Standby current: 0μA (Typ.)
- Operating temperature range: -40°C to +105°C

APPLICATION

- For indicator of Cluster Panel

BLOCK DIAGRAM

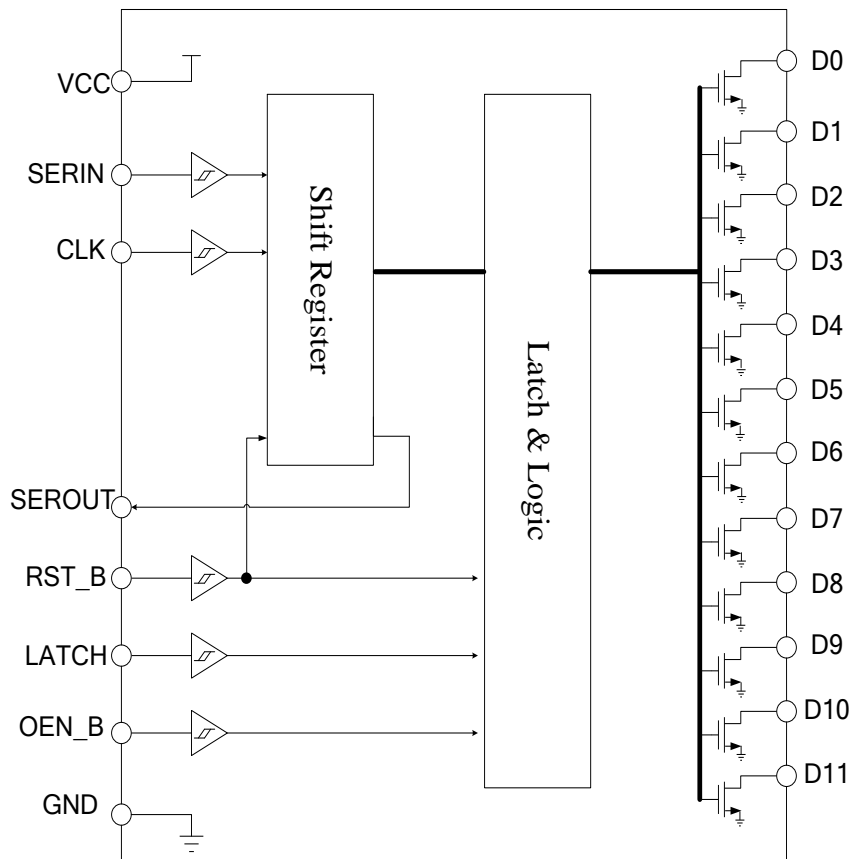


Figure 1. Block Diagram

APPLICATION CIRCUIT

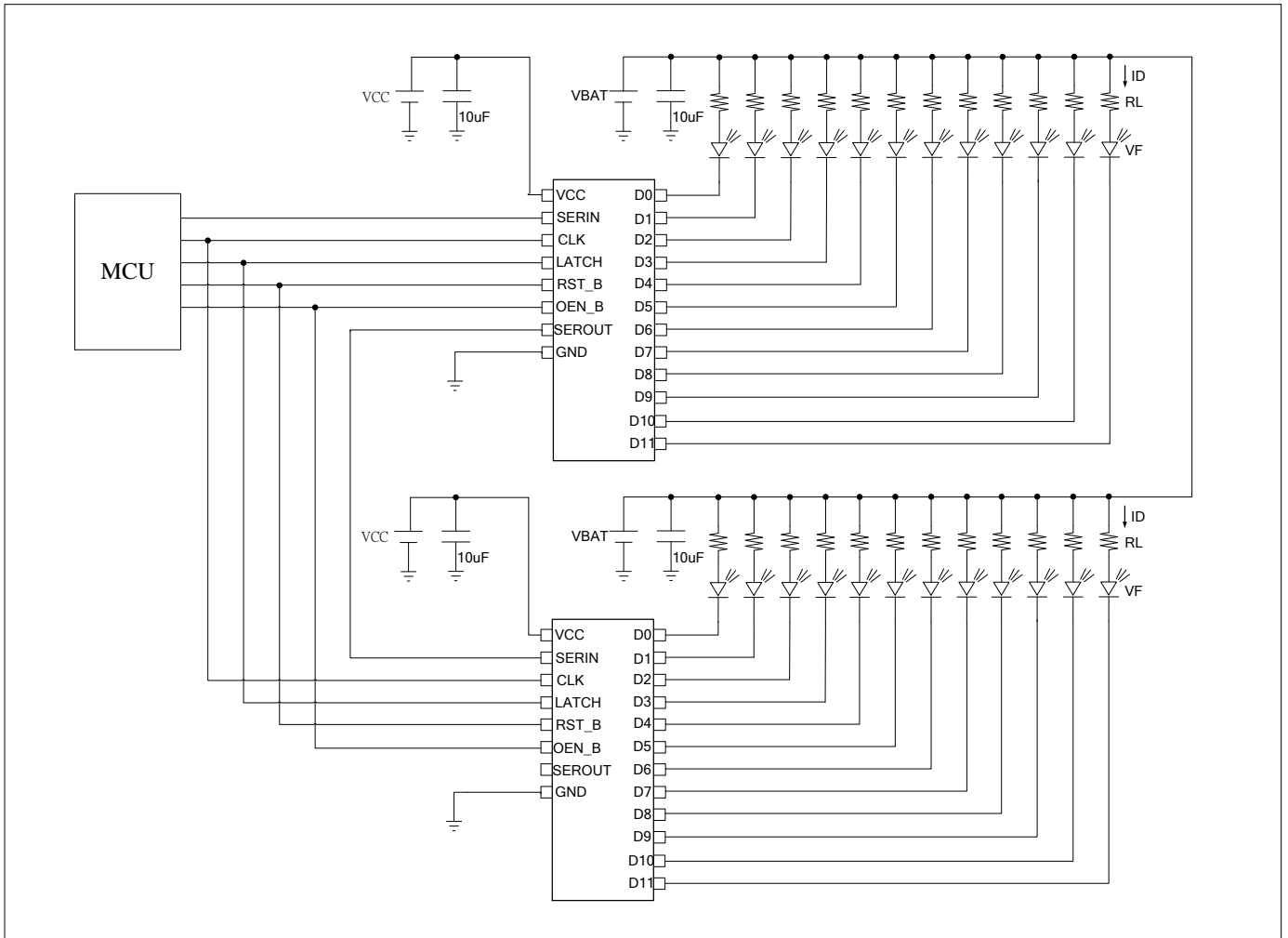


Figure 2. Application Circuit

ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT16940-TX	20 Pins, TSSOP	PT16940-TX

PIN CONFIGURATION

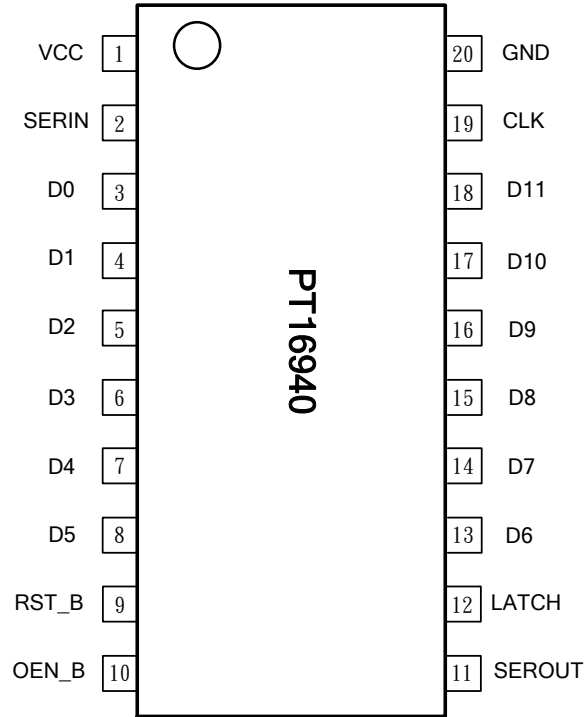


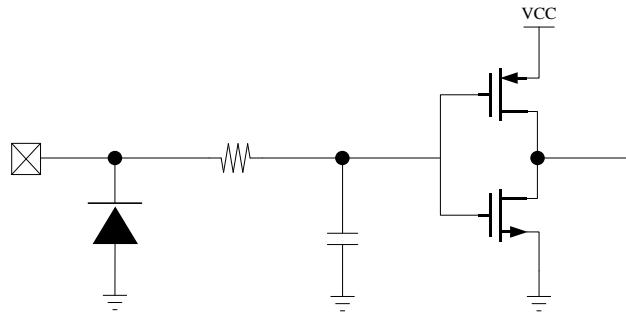
Figure 3. Pin Configuration

PIN DESCRIPTION

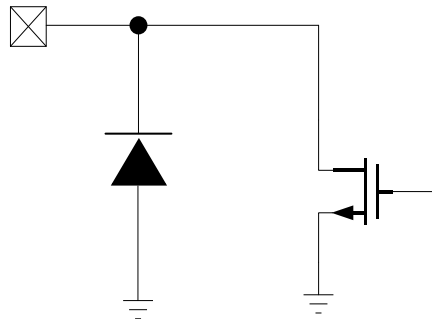
Pin Name	Description	Pin No.
VCC	Power supply voltage input	1
SERIN	Serial data input	2
D0	Drain output 0	3
D1	Drain output 1	4
D2	Drain output 2	5
D3	Drain output 3	6
D4	Drain output 4	7
D5	Drain output 5	8
RST_B	Reset invert input (Low:FF data 0)	9
OEN_B	Output enable (High:Output OFF)	10
SEROUT	Serial data output	11
LATCH	Latch signal input (High:Data latch)	12
D6	Drain output 6	13
D7	Drain output 7	14
D8	Drain output 8	15
D9	Drain output 9	16
D10	Drain output 10	17
D11	Drain output 11	18
CLK	Clock input	19
GND	GND	20

I/O EQUIVALENCE CIRCUITS

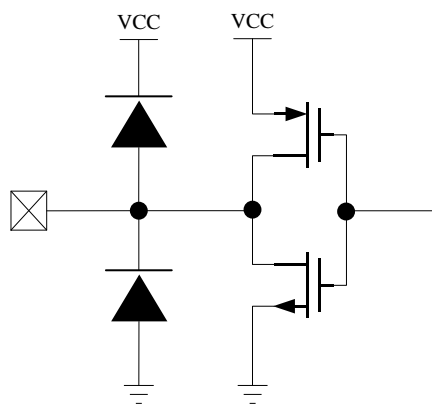
2PIN (SERIN), 9PIN (RST_B), 10PIN (OEN_B), 12PIN (LATCH), 19PIN (CLK)



3PIN (D0), 4PIN (D1), 5PIN (D2), 6PIN (D3), 7PIN (D4), 8PIN (D5), 13PIN (D6), 14PIN (D7), 15PIN (D8), 16PIN (D9), 17PIN (D10), 18PIN (D11)



11PIN (SEROUT)



SERIAL COMMUNICATION

The serial I/F is composed of a shift register which changes the CLK and SERIN serial signals to parallel signals, and a register to store those signals with a LATCH signal. The registers are reset by applying a voltage below VTL to the RST_B terminal, and D11 to D0 become open. To prevent erroneous LED lighting, please apply voltage below VTL to RST_B during start-up.

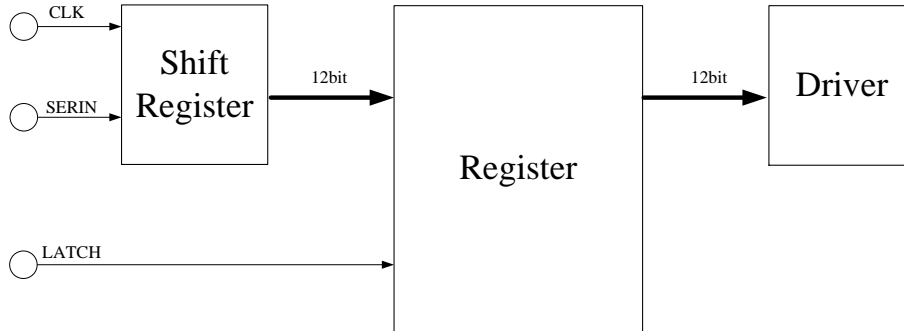


Figure 4. Block Diagram of Serial Communication

1) Serial Communication Timing

The 12-bit serial data input from SERIN is taken into the shift register by the rising edge of the CLK signal, and is recorded in the register by the rising edge of the LATCH signal. The recorded data is valid until the next rising edge of the LATCH signal.

2) Serial Communication Data

The serial data input configuration of SERIN terminal is shown below:

First →	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0	←Last
Data													

Terminal	Output Condition	Data											
		d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0
D11	ON	1	*	*	*	*	*	*	*	*	*	*	*
	OFF	0	*	*	*	*	*	*	*	*	*	*	*
D10	ON	*	1	*	*	*	*	*	*	*	*	*	*
	OFF	*	0	*	*	*	*	*	*	*	*	*	*
D9	ON	*	*	1	*	*	*	*	*	*	*	*	*
	OFF	*	*	0	*	*	*	*	*	*	*	*	*
...
D2	ON	*	*	*	*	*	*	*	*	*	1	*	*
	OFF	*	*	*	*	*	*	*	*	*	0	*	*
D1	ON	*	*	*	*	*	*	*	*	*	*	1	*
	OFF	*	*	*	*	*	*	*	*	*	*	0	*
D0	ON	*	*	*	*	*	*	*	*	*	*	*	1
	OFF	*	*	*	*	*	*	*	*	*	*	*	0

3) Enable Signal

By applying voltage at least V_{TH} or more to the OEN_B terminal, D11 to D0 become open forcibly. D11 to D0 become PWM operation by having the PWM signal to the OEN_B terminal.

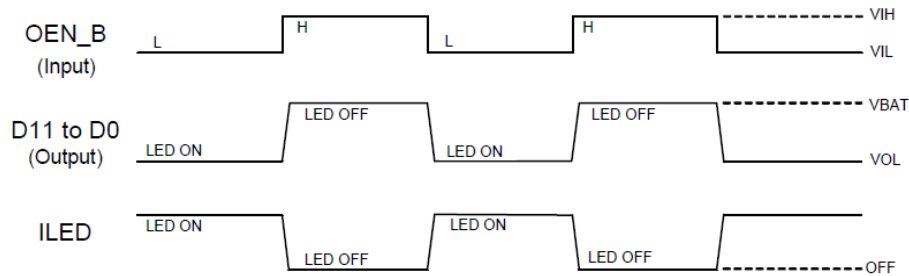


Figure 5. PWM Signal

4) SEROUT

A cascade connection can be made (connecting at least 2 or more IC's in serial).

Serial signal input from SERIN is transferred into receiver IC by the falling edge of the CLK signal.

Since this functionality gives enough margins for the setup time prior to the rising edge of the CLK signal on the receiver IC (using the exact same CLK signal of sender IC), the application reliability can be improved as cascade connection functionality.

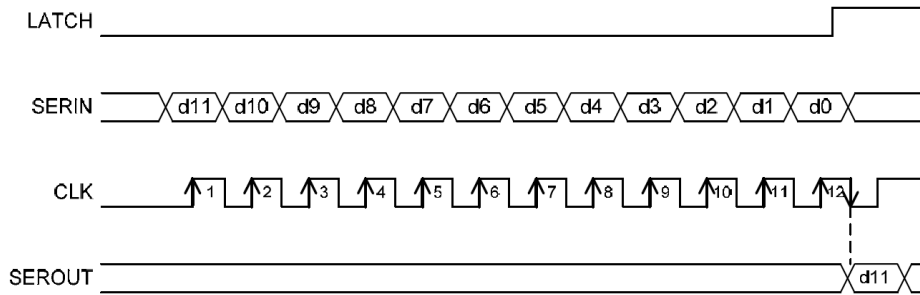


Figure 6. SEROUT Output Signal

CASCADE CONNECTION

By using (at least) 2 ICs, each IC's D11 to D0, at (at least) 24ch, can be controlled by the 24-bit SERIN signal.

The serial data input to the sender IC can be transferred to the receiver IC by inputting 12 CLK to the CLK terminal.

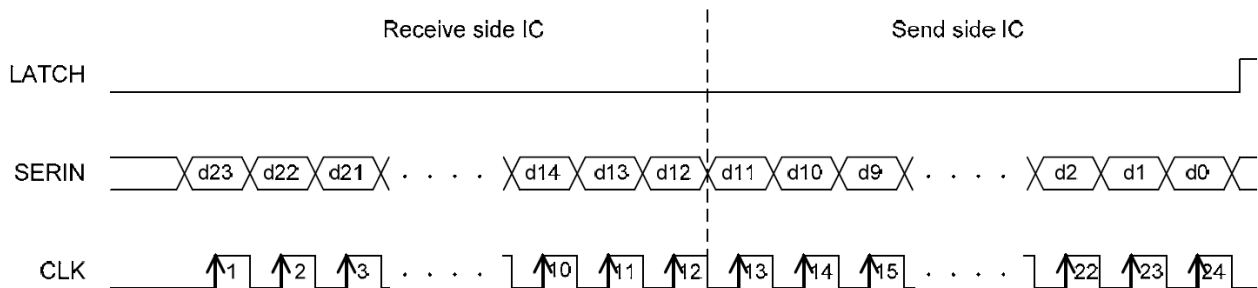


Figure 7. Cascade Connection

INPUT SIGNAL TIMMING CHART

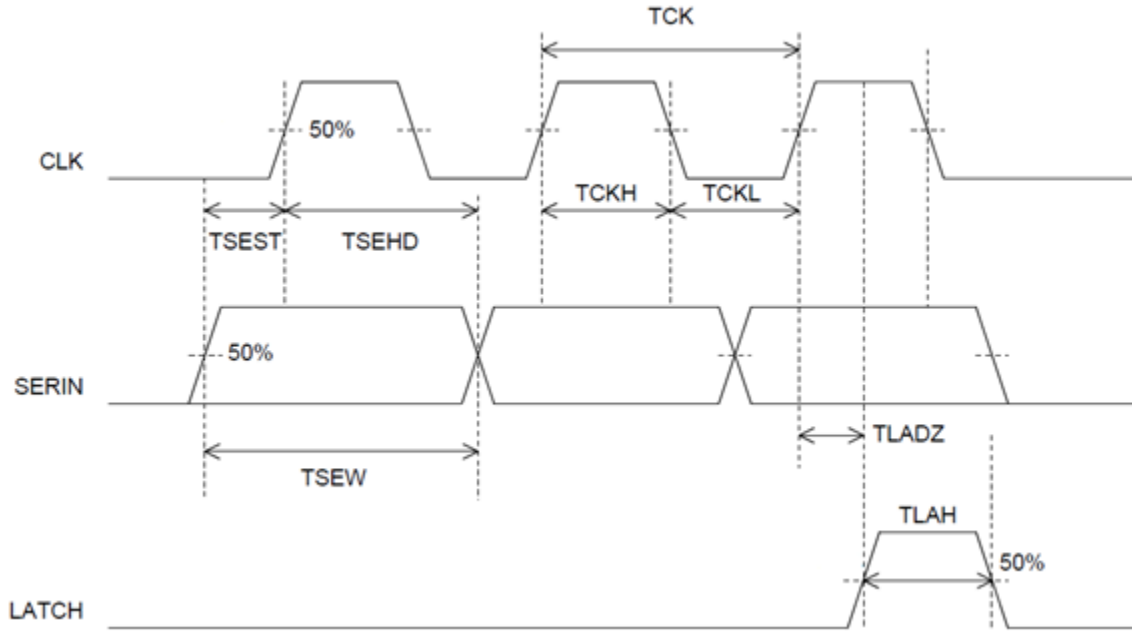


Figure 8. Timing Chart of Input Signal

INPUT SIGNAL'S TIMING RULE

($T_a = -40$ to 105°C VCC=3.0 to 5.5V)

Parameter	Symbol	Min	Unit
CLK Period	TCK	800	ns
CLK High Pulse Width	TCKH	380	ns
CLK Low Pulse Width	TCKL	380	ns
SERIN High and Low Pulse Width	TSEW	780	ns
SERIN Setup Time Prior to CLK Rise	TSEST	150	ns
SERIN Hold Time After CLK Rise	TSEHD	150	ns
LATCH High Pulse Time	TLAH	380	ns
Last CLK Rise To LATCH Rise	TLADZ	200	ns

OUTPUT SIGNAL DELAY CHART

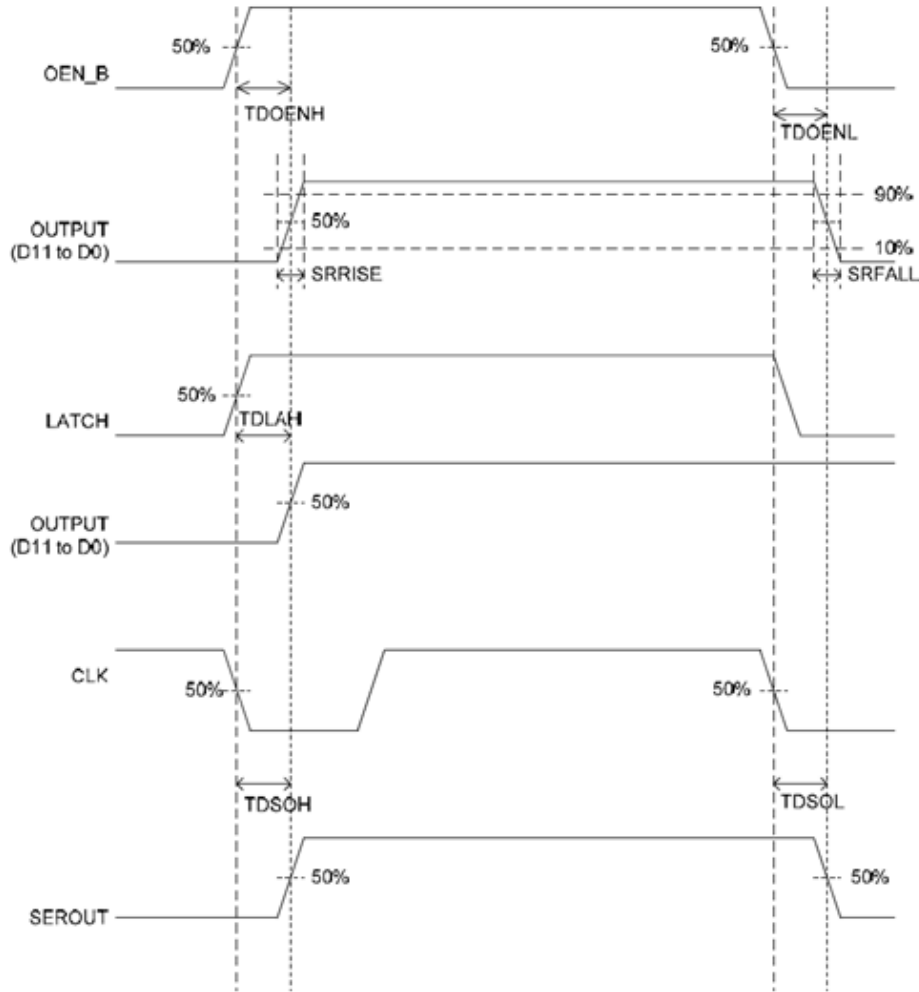


Figure 9. Delay Chart of Output Signal

OUTPUT SIGNAL'S DELAY TIME

(Ta=-40 to 105°C VCC=3.0 to 5.5V)

Parameter	Symbol	Condition	Min	Typ.	Max.	Unit
OEN_B Switching Time (L→H)	TDOENH		-		3000	ns
OEN_B Switching Time (H→L)	TDOENL		-		3000	ns
LATCH Switching Delay Time	TDLAH		-	-	3000	ns
SEROUT Propagation Delay Time (L→H)	TDSOH		-	-	350	ns
SEROUT Propagation Delay Time (H→L)	TDSOL		-		350	ns
Rising Slew Rate	SRRISE	Ta=25°C, VCC=5V, RL=500Ω, VBAT=10V	-	20	-	V/μs
Falling Slew Rate	SRFALL	Ta=25°C, VCC=5V, RL=500Ω, VBAT=10V	-	20	-	V/μs

POWER DISSIPATION

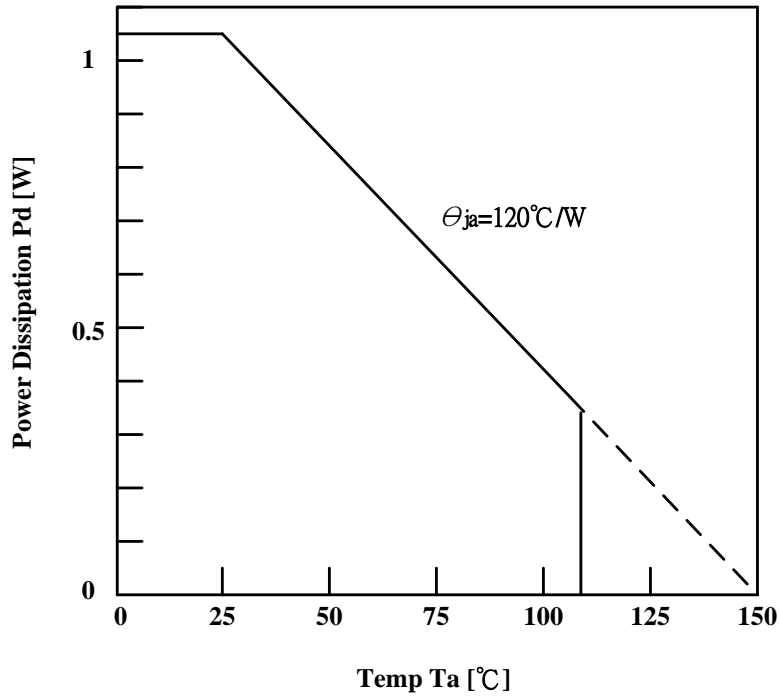


Figure 10. TSSOP-20 Power Dissipation

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Power Supply Voltage	VCC	5.5	V
Output Voltage	VDmax	36	V
Input Voltage	VIN	-0.3 to VCC	V
Power Dissipation	Pd	940*	mW
Operating Temperature Range	Topr	-40 to +105	°C
Storage Temperature Range	Tstg	-40 to +150	°C
Drive Current (DC)	IomaxD	50	mA
Drive Current (Pulse)	IomaxP	150*	mA
Junction Temperature	Tjmax	150	°C
ESD*	HBM	4	KV
	CDM	0.5	KV

*Will be determined after evaluation

*HBM : JEDEC 22-A114 ; CDM : AEC-Q100-011C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Power Supply Voltage	VCC	3.0 to 5.5	V
Operational Temperature	Topr	-40 to 105	°C

ELECTRICAL CHARACTERISTICS

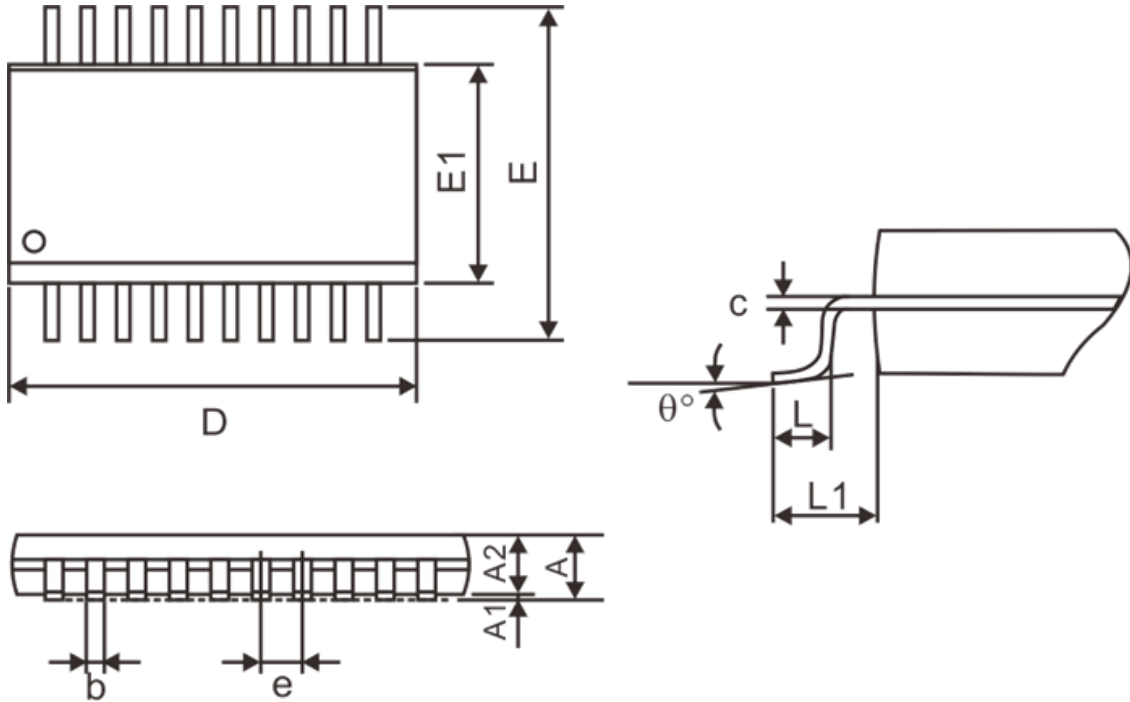
(Unless specified, Ta=-40 to 105°C VCC=3.0 to 5.5V)

Parameter	Symbol	Condition	Min	Typ.	Max.	Unit
【Output D0~D11】 (Pin 3~8, Pin 13~18)						
ON Resistor1	RON1	ID=20mA, VCC=4.5 to 5.5V	-	6	12	Ω
ON Resistor2	RON2	ID=20mA, VCC=3.0 to 4.5V	-	9	18	Ω
Output Leakage Current1	IDL1	VD=34V	-	-	1	μA
Output Leakage Current2	IDL2	VD=16V, Ta=25°C	-	-	0.5	μA
【Logic input】 (Pin 2,9,10,12,19)						
Upper Limit Threshold Voltage1	VTH1	VCC=4.5 to 5.5V	VCC*0.5	-	-	V
Upper Limit Threshold Voltage2	VTH2	VCC=3.0 to 4.5V	VCC*0.6	-	-	V
Bottom Limit Threshold Voltage1	VTL1	VCC=4.5 to 5.5V	-	-	VCC*0.2	V
Bottom Limit Threshold Voltage2	VTL2	VCC=3.0 to 4.5V	-	-	VCC*0.3	V
OEN-B Hysteresis Width	VHYS	VCC=5.0, OEN-B PIN	0.15	0.30	0.50	V
Serial Clock Frequency	FCLK		-	-	1.25	MHz
Input Leakage Current L	IINLL	VIN=0V	-5	0	-	μA
Input Leakage Current H	IINLH	VIN=5V	-	0	5	μA
【WHOLE】						
Circuit Current	ICC	Serial Data Input, VCC=5V, CLK=500KHz, VTH=VCC, VTL=0V SEROUT=OPEN	-	0.05	1	mA
Static Current	ISTN	SEROUT=OPEN	-	0	50	μA
【SEROUT】 (Pin 11)						
Output Voltage High1	VOH1		4.6	4.8	-	V
Output Voltage Low1	VOL1		-	0.2	0.4	V
Output Voltage High2	VOH2		2.7	3.0	-	V
Output Voltage Low2	VOL2		-	0.3	0.6	V

* This product is not designed for protection against radioactive rays.

PACKAGE INFORMATION

20-PIN, TSSOP, 173MIL



Symbol	Dimensions(mm)		
	Min.	Typ.	Max.
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	1.00	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	6.40	6.50	6.60
e	0.65 BSC.		
E	6.40 BSC.		
E1	4.30	4.40	4.50
L	0.45	0.60	0.75
L1	1.0 REF.		
θ	0°	-	8°

Notes:

1. Refer to JEDEC MO-153 AC

IMPORTANT NOTICE

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