

DESCRIPTION

The PT16941 is a serial-in parallel-out controlled LED driver with 35V output voltage rating. With the input of 3-line serial data, it turns the 8ch open drain output on/off. Due to its compact size, it is optimal for small space.

FEATURES

- Open Drain Output
- 3-line Serial Control + Enable Signal
- Cascade Connection Compatible
- TSSOP-16 / SOP16 (150mil) Package
- Internal 8ch Power Transistor
- AEC-Q100 Qualified.
- Output Slew Rate Typical 20V/ μ s (for Low EMC Noise)

KEY SPECIFICATIONS

- Input voltage range: 3.0V to 5.5V
- Output voltage range: 35V (Max.)
- DC Output Current (per CH): 50mA(Max.)
- Output ON Resistance: 6 Ω (Typ.)
- Standby current: 0 μ A (Typ.)
- Operating temperature range: -40 $^{\circ}$ C to +105 $^{\circ}$ C
- Package: 16 pins TSSOP / SOP(150mil)

APPLICATION

- For indicator of Cluster Panel

BLOCK DIAGRAM

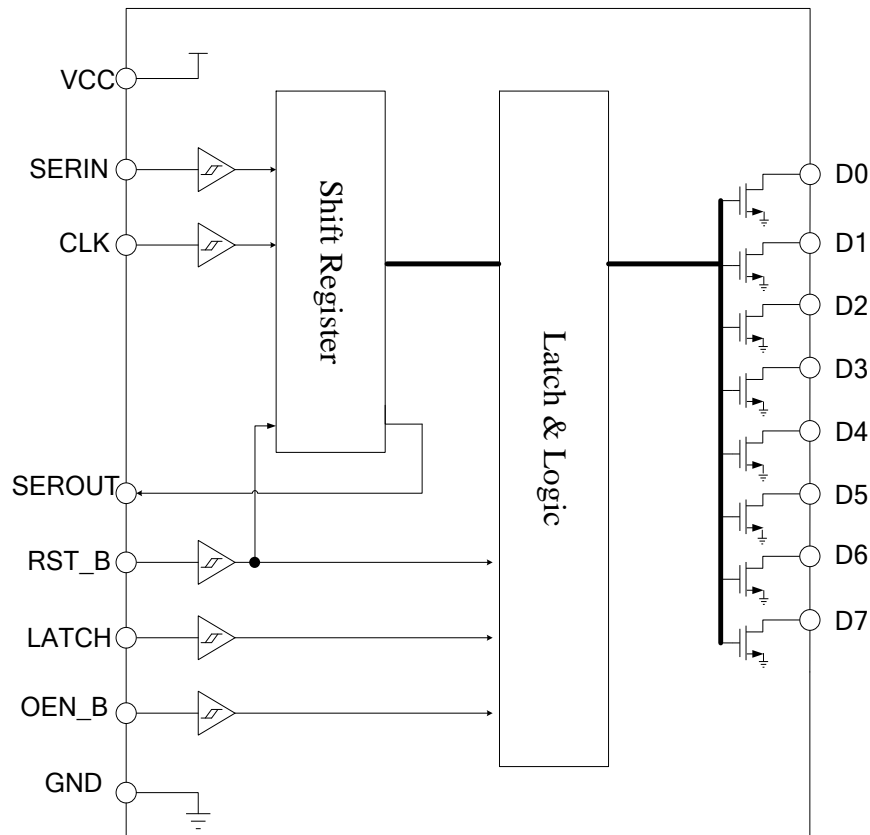


Figure 1. Block Diagram

APPLICATION CIRCUIT

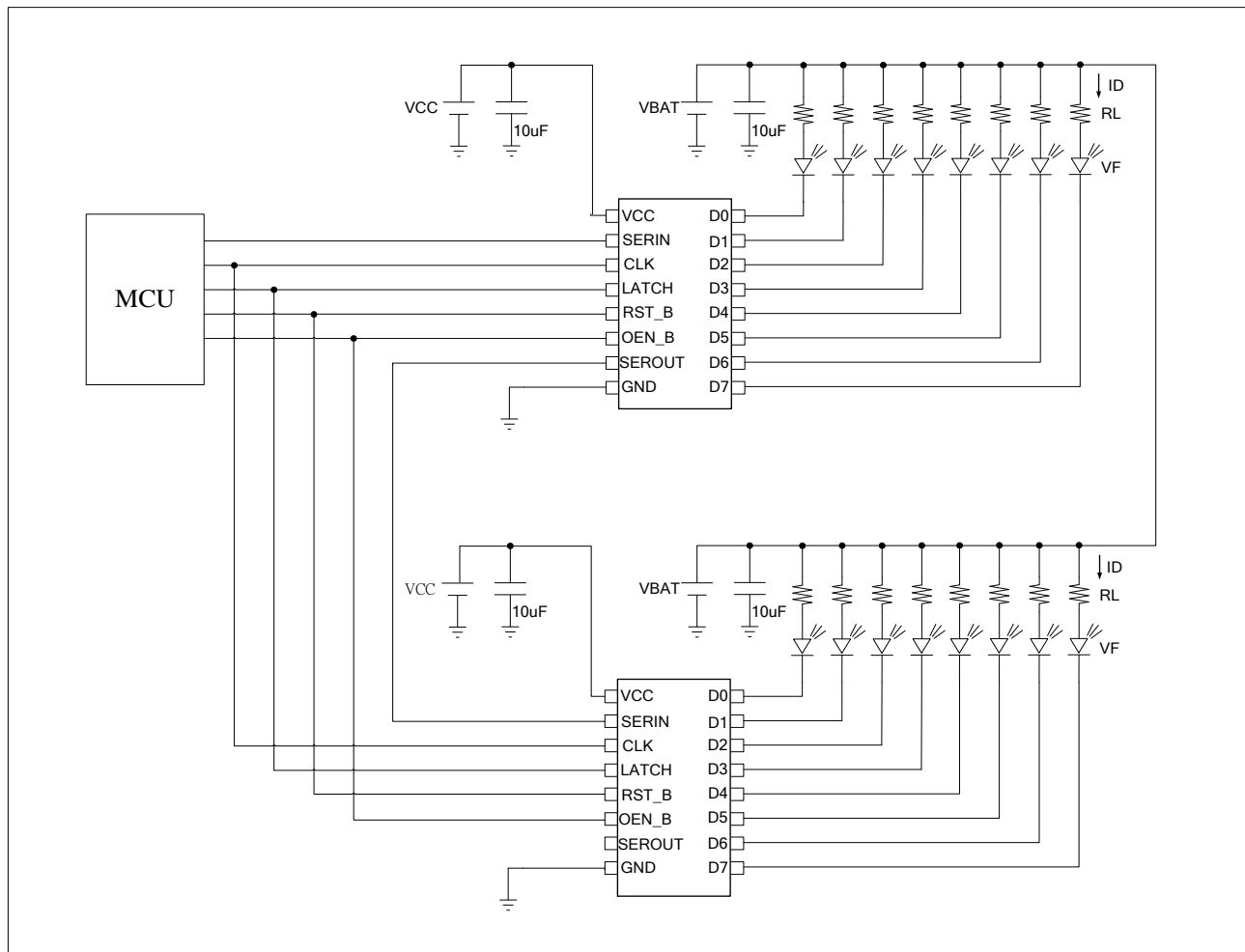


Figure 2. Application Circuit

ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT16941-TX	TSSOP, 16 Pins	PT16941-TX
PT16941-S	SOP, 16 Pins	PT16941-S

PIN CONFIGURATION

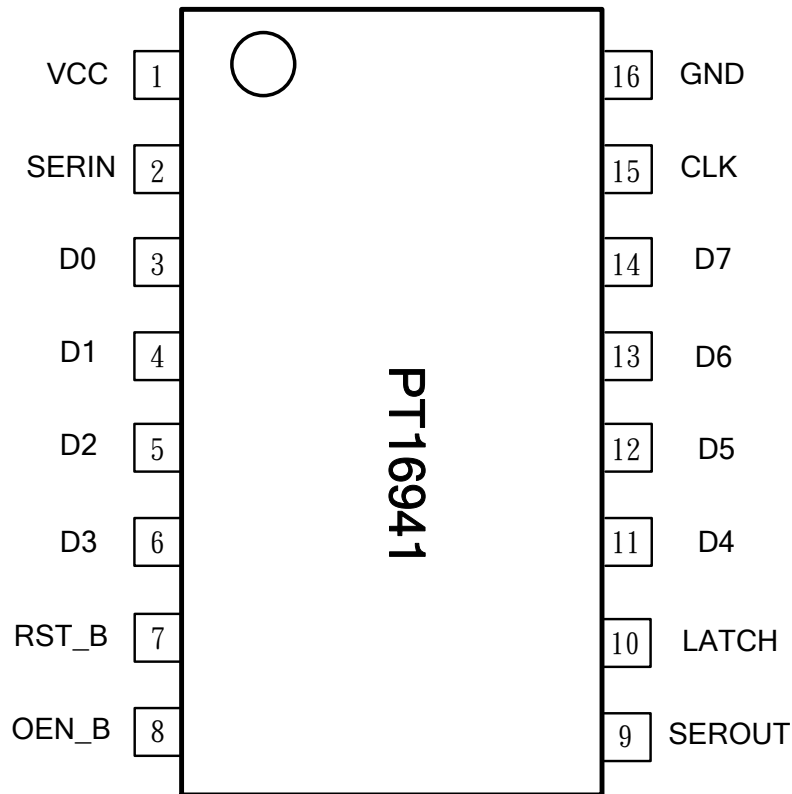


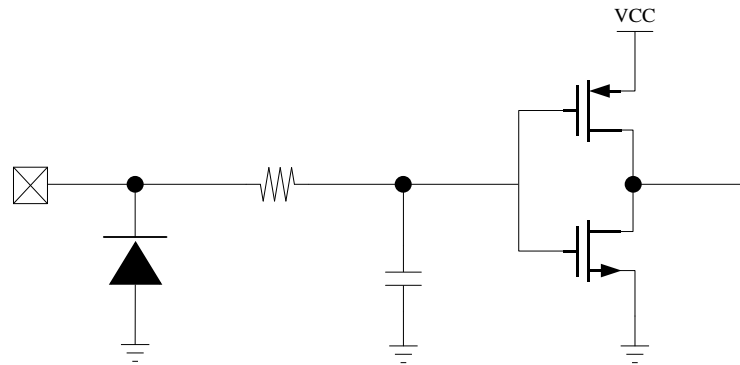
Figure 3. Pin Configuration

PIN DESCRIPTION

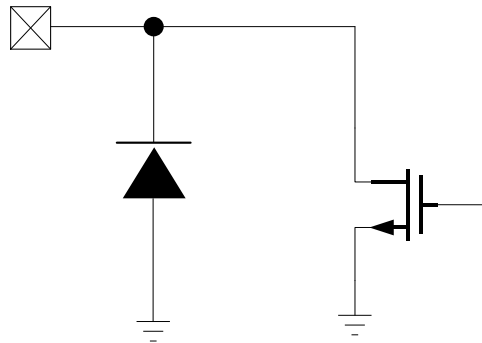
Pin Name	Description	Pin No.
VCC	Power supply voltage input	1
SERIN	Serial data input	2
D0	Drain output 0	3
D1	Drain output 1	4
D2	Drain output 2	5
D3	Drain output 3	6
RST_B	Reset invert input (Low: FF data 0)	7
OEN_B	Output enable (High: Output OFF)	8
SEROUT	Serial data output	9
LATCH	Latch signal input (High: Data latch)	10
D4	Drain output 4	11
D5	Drain output 5	12
D6	Drain output 6	13
D7	Drain output 7	14
CLK	Clock input	15
GND	GND	16

I/O EQUIVALENCE CIRCUITS

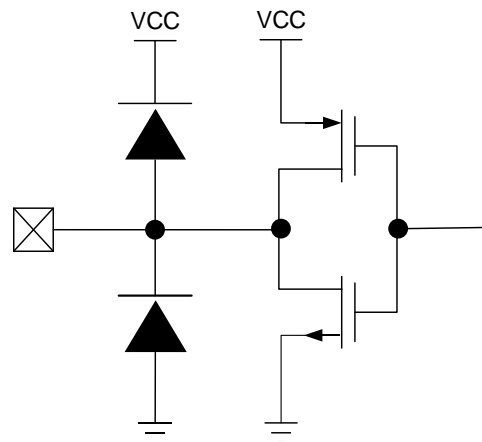
2 PIN (SERIN), 7 PIN (RST_B), 8 PIN (OEN_B), 10 PIN (LATCH), 15 PIN (CLK)



3 PIN (D0), 4 PIN (D1), 5 PIN (D2), 6 PIN (D3), 11 PIN (D4), 12 PIN (D5), 13 PIN (D6), 14 PIN (D7)



9 PIN (SEROUT)



FUNCTION DESCRIPTION

SERIAL COMMUNICATION

The serial I/F is composed of a shift register which changes the CLK and SERIN serial signals to parallel signals, and a register to store those signals with a LATCH signal. The registers are reset by applying a voltage below VTL to the RST_B terminal, and D7 to D0 become open. To prevent erroneous LED lighting, please apply voltage below VTL to RST_B during start-up.

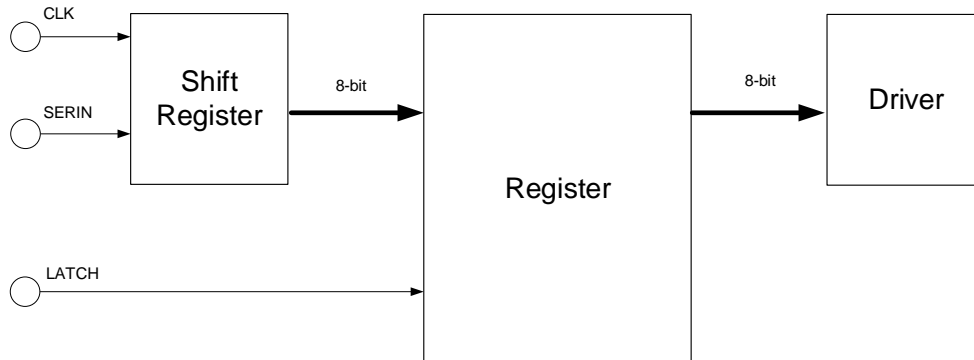


Figure 4. Block Diagram of Serial Communication

SERIAL COMMUNICATION TIMING

The 8-bit serial data input from SERIN is taken into the shift register by the rising edge of the CLK signal, and is recorded in the register by the rising edge of the LATCH signal. The recorded data is valid until the next rising edge of the LATCH signal.

SERIAL COMMUNICATION DATA

The serial data input configuration of SERIN terminal is shown below:

d7	d6	d5	d4	d3	d2	d1	d0
data							

Terminal	Output Condition	data							
		d7	d6	d5	d4	d3	d2	d1	d0
D7	ON	1	*	*	*	*	*	*	*
	OFF	0	*	*	*	*	*	*	*
D6	ON	*	1	*	*	*	*	*	*
	OFF	*	0	*	*	*	*	*	*
D5	ON	*	*	1	*	*	*	*	*
	OFF	*	*	0	*	*	*	*	*
D4	ON	*	*	*	1	*	*	*	*
	OFF	*	*	*	0	*	*	*	*
D3	ON	*	*	*	*	1	*	*	*
	OFF	*	*	*	*	0	*	*	*
D2	ON	*	*	*	*	*	1	*	*
	OFF	*	*	*	*	*	0	*	*
D1	ON	*	*	*	*	*	*	1	*
	OFF	*	*	*	*	*	*	0	*
D0	ON	*	*	*	*	*	*	*	1
	OFF	*	*	*	*	*	*	*	0

* indicate Don't care

ENABLE SIGNAL

By applying voltage at least V_{TH} or more to the OEN_B terminal, D7 to D0 become open forcibly.
 D7 to D0 become PWM operation by having the PWM signal to the OEN_B terminal.

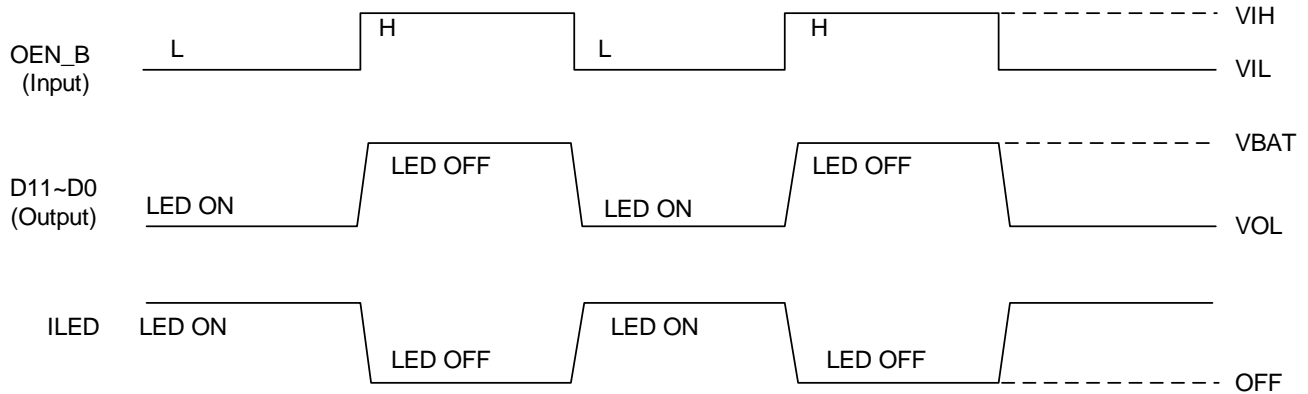


Figure 5. PWM Signal

SEROUT

A cascade connection can be made (connecting at least 2 or more IC's in serial).
 Serial signal input from SERIN is transferred into receiver IC by the falling edge of the CLK signal.
 Since this functionality gives enough margins for the setup time prior to the rising edge of the CLK signal on the receiver IC (using the exact same CLK signal of sender IC), the application reliability can be improved as cascade connection functionality.

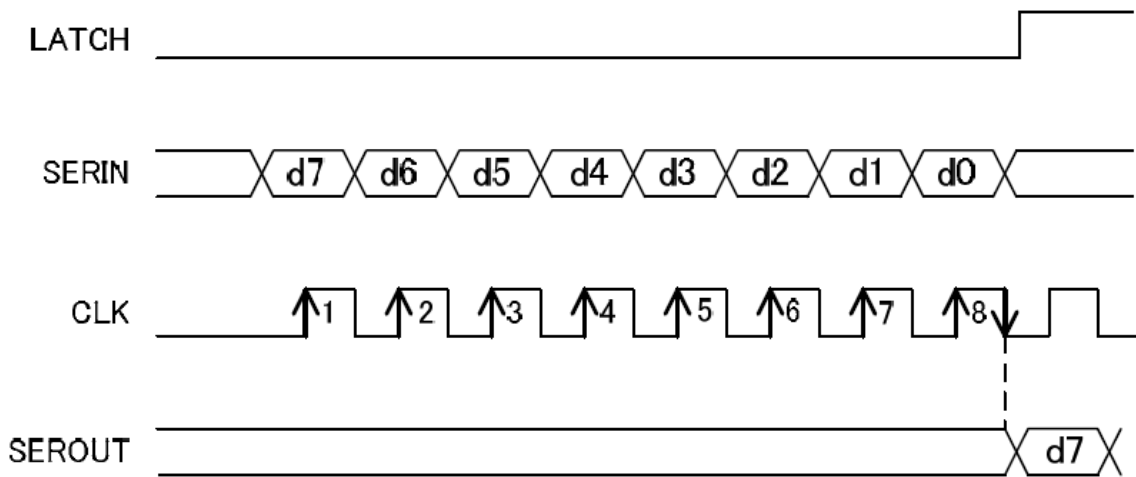


Figure 6. SEROUT Output Signal

CASCADE CONNECTION

By using (at least) 2 ICs, each IC's D7 to D0, at (at least) 8ch, can be controlled by the 16-bit SERIN signal. The serial data input to the sender IC can be transferred to the receiver IC by inputting 8 CLK to the CLK terminal.

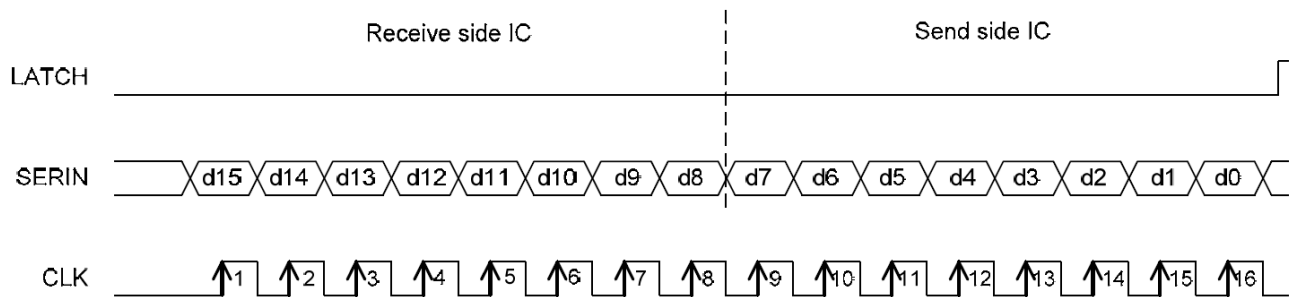


Figure 7. Cascade Connection

INPUT SIGNAL TIMMING CHART

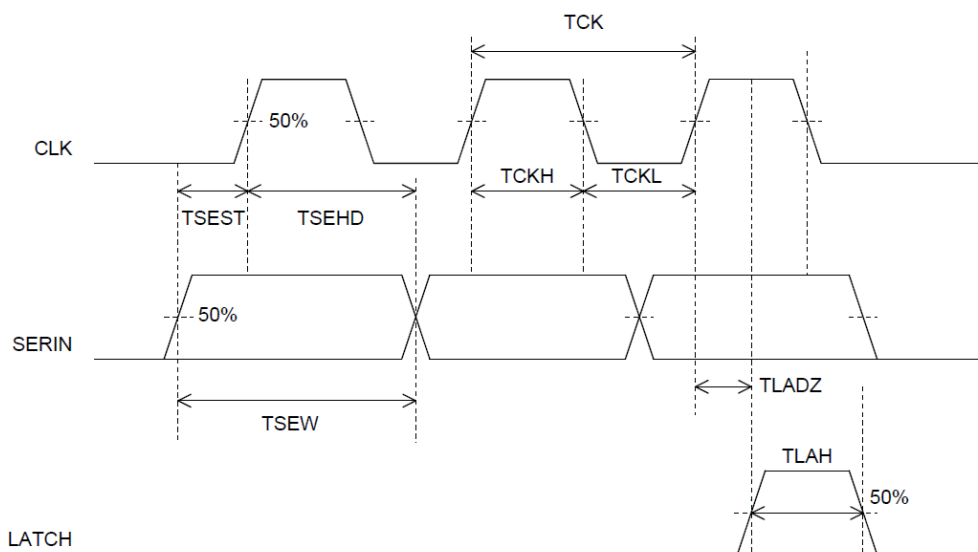


Figure 8. Timing Chart of Input Signal

Input Signal's Timing Rule (Ta=-40 to 105°C VCC=3.0 to 5.5V)

Parameter	Symbol	Min	Unit
CLK period	TCK	800	ns
CLK high pulse width	TCKH	380	ns
CLK low pulse width	TCKL	380	ns
SERIN high and low pulse width	TSEW	780	ns
SERIN setup time prior to CLK rise	TSEST	150	ns
SERIN hold time after CLK rise	TSEHD	150	ns
LATCH high pulse time	TLAH	380	ns
Last CLK rise to LATCH rise	TLADZ	200	ns

OUTPUT SIGNAL DELAY CHART

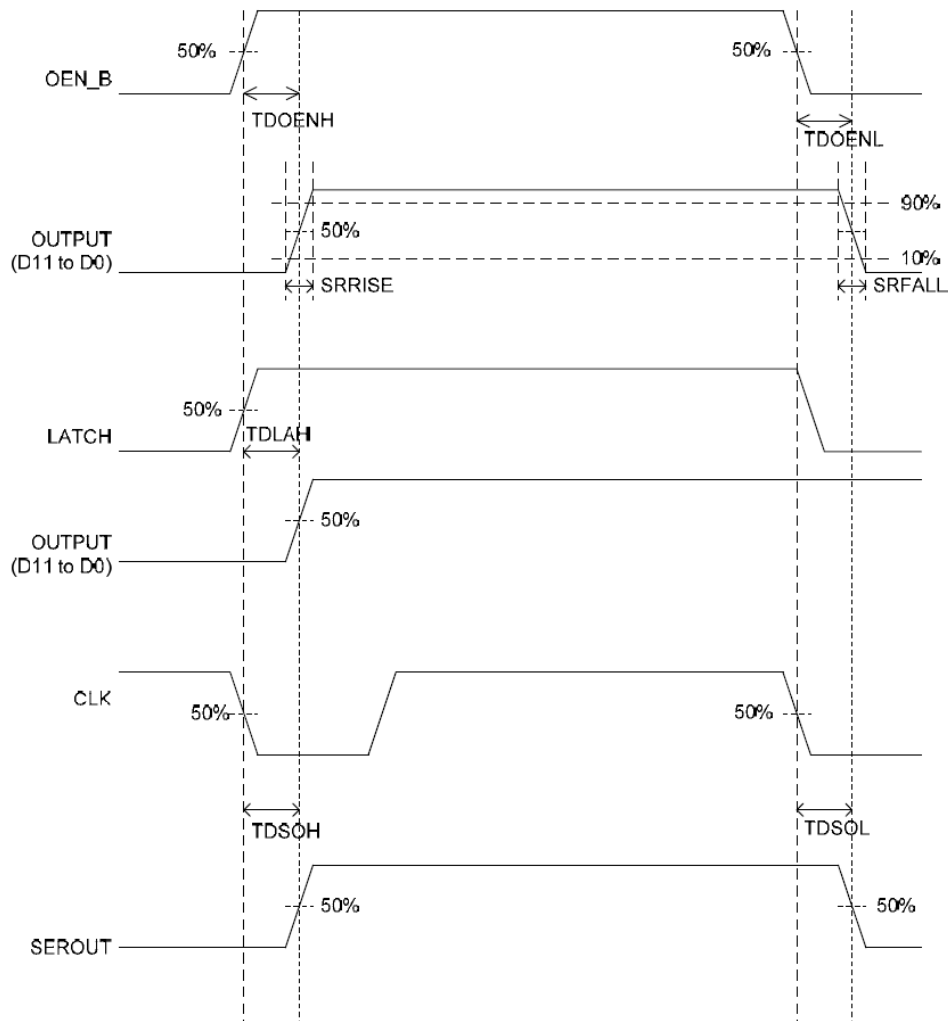


Figure 9. Delay Chart of Output Signal

Output Signal's Delay Time (Ta=-40 to 105°C VCC=3.0 to 5.5V)

Parameter	Symbol	Condition	Min	Typ.	Max.	Unit
OEN_B Switching Time (L→H)	TDOENH		-		3000	ns
OEN_B Switching Time (H→L)	TDOENL		-		3000	ns
LATCH Switching Delay Time	TDLAH		-	-	3000	ns
SEROUT Propagation Delay Time (L→H)	TDSOH		-	-	350	ns
SEROUT Propagation Delay Time (H→L)	TDSOL		-		350	ns
Rising Slew Rate	SRRISE	Ta=25°C, VCC=5V, RL=500Ω, VBAT=10V	-	20	-	V/μs
Falling Slew Rate	SRFALL	Ta=25°C, VCC=5V, RL=500Ω, VBAT=10V	-	20	-	V/μs

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Power Supply Voltage	VCC	5.5	V
Output Voltage	VDmax	36	V
Input Voltage	VIN	-0.3 to VCC	V
Power Dissipation	Pd	TBD	mW
Operating Temperature Range	Topr	-40 to +105	°C
Storage Temperature Range	Tstg	-40 to +150	°C

RECOMMENDED OPERATING RATINGS

Parameter	Symbol	Value	Unit
Power Supply Voltage	VCC	3.0 to 5.5	V
Operational Temperature	Topr	-40 to 105	°C

ELECTRICAL CHARACTERISTICS

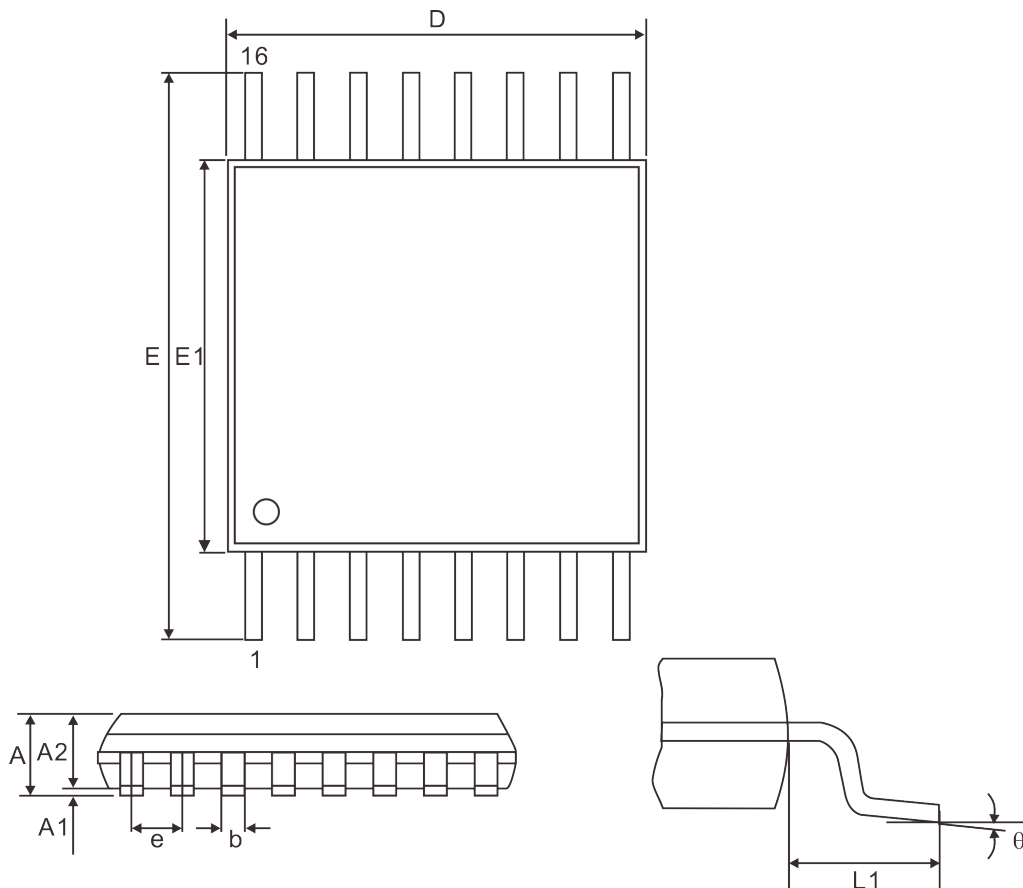
(Unless specified, Ta=-40 to 105°C VCC=3.0 to 5.5V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
【Output D0~D11】 (Pin 3~6, Pin 11~14)						
ON Resistor1	RON1	ID=20mA, VCC=4.5 to 5.5V	-	6	12	Ω
ON Resistor2	RON2	ID=20mA, VCC=3.0 to 4.5V	-	9	18	Ω
Output Leakage Current1	IDL1	VD=34V	-	-	1	μA
Output Leakage Current2	IDL2	VD=16V, Ta=25°C	-	-	0.5	μA
【Logic input】 (Pin 2,7,8,10,15)						
Upper Limit Threshold Voltage1	VTH1	VCC=4.5 to 5.5V	VCC*0.5	-	-	V
Upper Limit Threshold Voltage2	VTH2	VCC=3.0 to 4.5V	VCC*0.6	-	-	V
Bottom Limit Threshold Voltage1	VTL1	VCC=4.5 to 5.5V	-	-	VCC*0.2	V
Bottom Limit Threshold Voltage2	VTL2	VCC=3.0 to 4.5V	-	-	VCC*0.3	V
OEN-B Hysteresis Width	VHYS	VCC=5.0, OEN-B Pin	0.15	0.30	0.50	V
Serial Clock Frequency	FCLK		-	-	1.25	MHz
Input Leakage Current L	IINLL	VIN=0V	-5	0	-	μA
Input Leakage Current H	IINLH	VIN=5V	-	0	5	μA
【WHOLE】						
Circuit Current	ICC	Serial Data Input, VCC=5V, CLK=500KHz, VTH=VCC, VTL=0V, SEROUT=OPEN	-	0.05	1	mA
Static Current	ISTN	SEROUT=OPEN	-	0	50	μA
【SEROUT】 (Pin 9)						
Output Voltage High1	VOH1		4.6	4.8	-	V
Output Voltage Low1	VOL1		-	0.2	0.4	V
Output Voltage High2	VOH2		2.7	3.0	-	V
Output Voltage Low2	VOL2		-	0.3	0.6	V

* This product is not designed for protection against radioactive rays.

PACKAGE INFORMATION

16 Pins, TSSOP



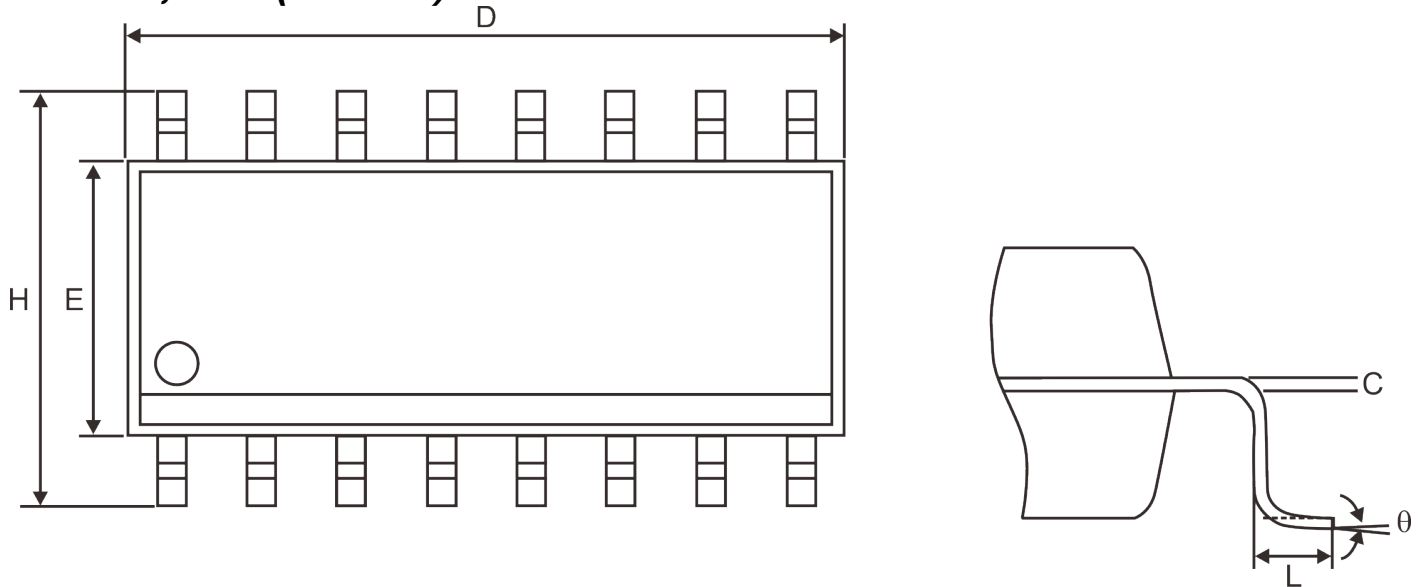
Symbol	Dimensions (mm)		
	Min.	Nom.	Max.
A	-	-	1.20
A1	0.00	-	0.15
A2	0.80	1.00	1.05
b	0.19	-	0.30
e	0.65 BSC		
D	4.90	5.00	5.10
E	6.40 BSC		
E1	4.30	4.40	4.50
L1	1.00 REF		
θ	0°	-	8°

Notes:

1. Refer to JEDEC MO-153 AB/ABT(Thermally Enhanced Variations)

PACKAGE INFORMATION

16 Pins, SOP(150MIL)



Symbol	Dimensions (mm)		
	Min.	Nom.	Max.
A	1.35	-	1.75
A1	0.10	-	0.25
b	0.31	-	0.51
c	0.10	-	0.25
e	1.27 BSC		
D	9.90 BSC		
H	6.00 BSC		
E	3.90 BSC		
L	0.40	-	1.27
θ	0°	-	8°

Notes:

1. Refer to JEDEC MS-012AC

IMPORTANT NOTICE

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