DESCRIPTION

PT16974 is a linear LED driver for automotive exterior lighting. It incorporates linear regulation and multiple logic control for use in Rear Combination Lamps. There are eight linear programmable constant current sources, so that provides various sequencing turn signals.

PT16974 allows to set the STOP (DC value) and TAIL illumination (PWM duty cycle) via tow single resistors, the TAIL illumination can be controlled by external PWM input also.

Sequencing functionality is activated, controlled, and programmed by individual pins. In addition to programming of the sequence interval, the device can sequence 8 individual output channels, 4 pairs of output channels, 2 quad output channels, or all 8 at once.

An optional external ballast FET helps distribute the system power for high current application. Regulates the voltage at the top (anode) of the LED strings， to reduce the power dissipation of the device. Set back power limit reduces the drive current during overvoltage conditions. This is most useful for low power applications when no external FET is used.

A global enable function helps to active the device by external signal.

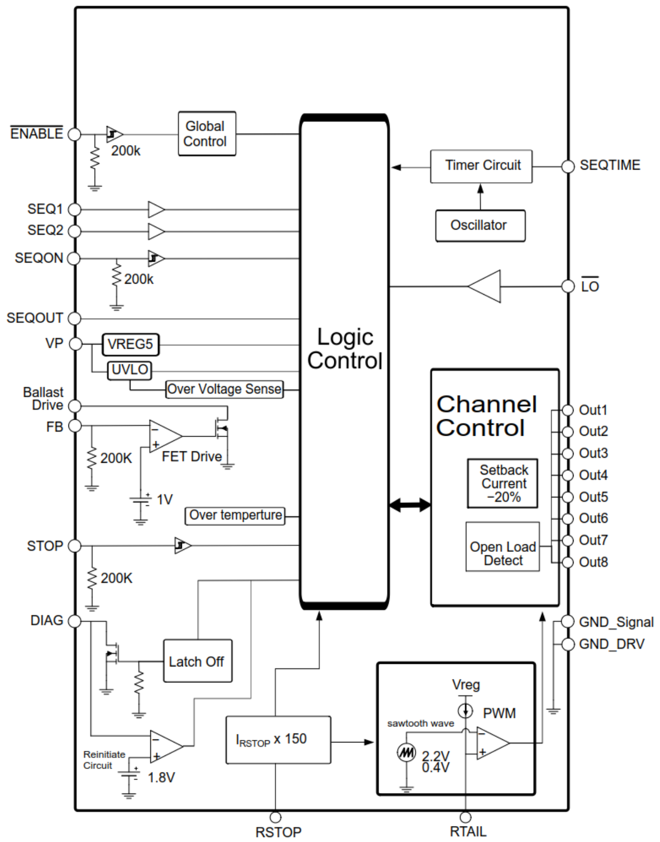
APPLICATION

- Rear Combination Lamps (RCL)
- Turn Signal
- Center High Mounted Stop Lamps (CHMSL) Arrays
- Daytime Running Lights (DRL)
- Fog Lights
- Signature Lamp

FEATURE

- Automotive AEC-Q100, Grade 1 (-40℃~+125℃) Qualified.
- Programmable LED current outputs for LED string
- LED current up to 800mA
- Single resistor set for the STOP current
- Single resistor set for the TAIL dimming
- Single resistor set for programming of the sequence interval
- Global enable control
- Various display sequencing
- Open LED string diagnostic with open−drain output in all modes
- Integrated 800Hz PWM dimming
- External PWM modulation input
- Low dropout operation for pre−regulator applications Overvoltage set back power limitation
- Programmable latch−off function on open string
- Over temperature protection
- HSSOP24 package

BLOCK DIAGRAM

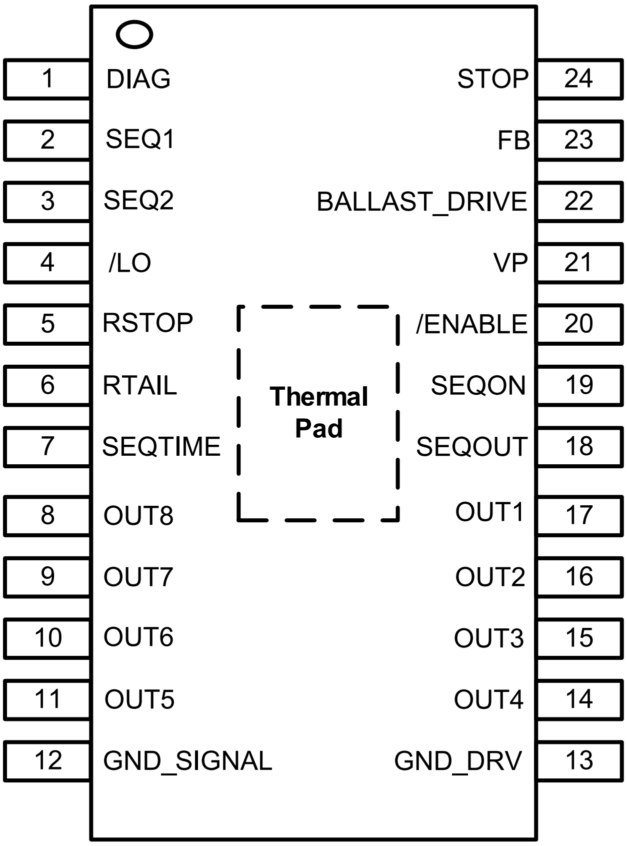


ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT16974-HX	24 Pins, HSSOP	PT16974-HX

PIN CONFIGURATION

Top View



PIN DESCRIPTION

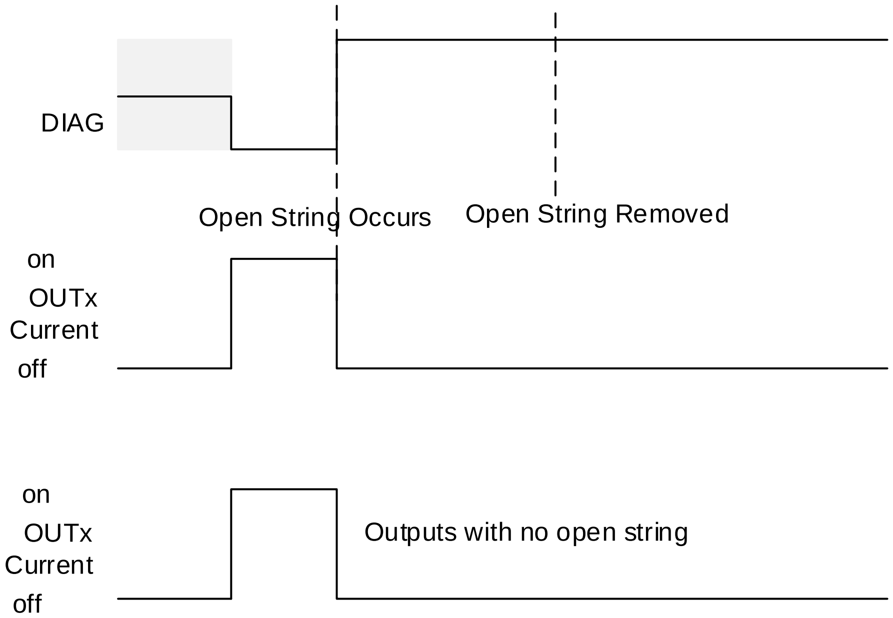
Pin Name	Description	Pin No.
DIAG	Diagnostic output. Requires a pull−up resistor. Normal operation in logic low, and indicate fault status in logic high. Fault status includes LED open circuit, RSTOP current limit, set back current Limit down 20%, and thermal shutdown. Forcing this pin below 1.8V (typ) to reinitiate the device. Ground this pin if not used.	1
SEQ1	Output sequencing setting. Ground or leave this pin floating for sequencing programming.	2
SEQ2	Output sequencing setting. Ground or leave this pin floating for sequencing programming.	3
LO	Ground this pin for latch off function.	4
RSTOP	STOP current programming pin. Connect a resistor to GND_Signal to set the output current of STOP mode.	5
RTAIL	TAIL current PWM duty cycle programming pin. Connect a resistor to GND_Signal to set the dimming duty cycle. Ground pin if using external modulation.	6
SEQTIME	Sequence Time programming pin. Connect a resistor to GND_Signal to set the sequence time.	7
OUT8	Channel 8 constant current output to LED. Ground this pin to GND_DRV is not used.	8
OUT7	Channel 7 constant current output to LED. Ground this pin to GND_DRV is not used.	9
OUT6	Channel 6 constant current output to LED. Ground this pin to GND_DRV is not used.	10
OUT5	Channel 5 constant current output to LED. Ground this pin to GND_DRV is not used.	11
GND_Signal	Analog ground. Return for the internal reference voltage and analog circuit. Connect to circuit ground, GND, to complete return path.	12
GND_DRV	Power ground. Return for high current (8 channels). Connect to circuit ground, GND, to complete return path.	13
OUT4	Channel 4 constant current output to LED. Ground this pin to GND_DRV is not used.	14
OUT3	Channel 3 constant current output to LED. Ground this pin to GND_DRV is not used.	15
OUT2	Channel 2 constant current output to LED. Ground this pin to GND_DRV is not used.	16
OUT1	Channel 1 constant current output to LED. Ground this pin to GND_DRV is not used.	17
SEQOUT	Sequence status reporting, open−drain output, requires a pull−up resistor. Follows $\overline{\text{ENABLE}}$ pin after delay of OUT8 with SEQON high.	18
SEQON	Sequence mode enable. Requires a pull−up resistor, tie this pin to logic high， turns on 1−8 output sequencing.	19
$\overline{\text{ENABLE}}$	Global enable input. Ground this pin to turn device on.	20
VP	Supply voltage input.	21
Ballast Drive	Gate drive for external power distribution PFET. Ground if not used.	22
FB	Feedback Sense reference, connect resistor divider from the top (anode) of the LED strings (Vstring) to set the regulation voltage. Connect to GND if not use.	23
STOP	Stop Logic Input. External Modulation Input when VP is high.	24
Thermal pad	Ground. Do not connect to PCB traces other than GND.	Thermal pad

TABLE 1. APPLICATION I/O TRUTH TABLE

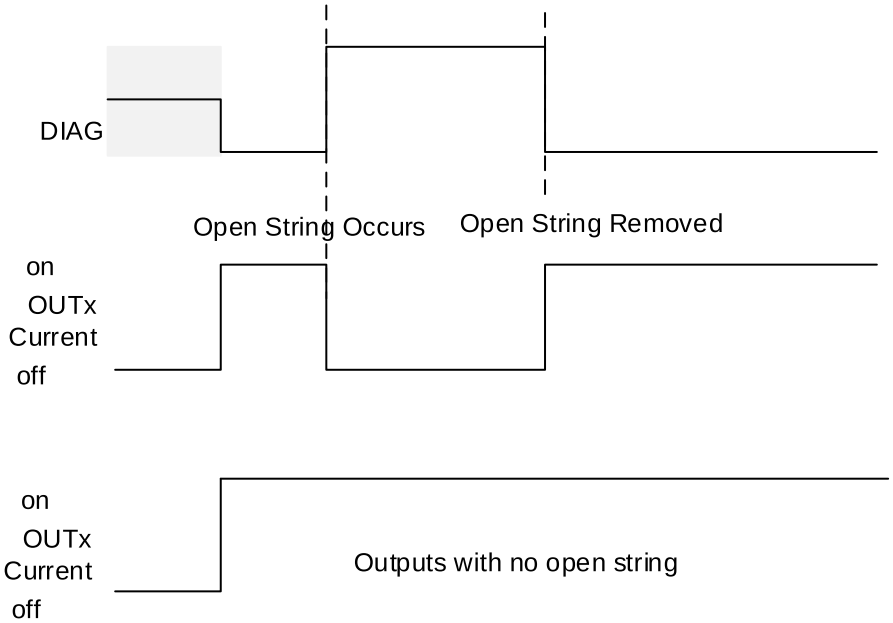
$\overline{EN}$	SEQON	STOP INPUT	TAIL MODE	OUTx LATCH OFF ($\overline{LO}$ = GND)	OUTX CURRENT	FAULT STATE[1]	DIAG STATE[2]
1	X	X	X	no	OFF	−	1
0	0	0	0	no	OFF	−	1
0	0	1	X	no	I_{STOP}	NORMAL	0
0	0	1	X	no	I_{STOP}	OPEN CIRCUIT[3]	1
0	0	1	X	yes	OFF	OPEN CIRCUIT[3]	1
0	0	0	1	no	PWM	NORMAL	0
0	0	0	1	no	PWM	OPEN CIRCUIT[3]	PWM
0	1	X	X	no	I_{STOP}	NORMAL	0
0	1	X	X	no	I_{STOP}	OPEN CIRCUIT[3]	1
0	1	X	X	yes	OFF	OPEN CIRCUIT[3]	1

Reference Figures below.
X = Don’t care
0 = Logic LOW
1 = Logic HIGH
NOTE: （1）Open Circuit, RSTOP Current Limit, set Back Current Limit down 20%, and thermal shutdown
（2）Pull−up resistor to DIAG and SEQOUT required.
（3）Any string or SEQOUT open.

DIAG TIMING DIAGRAM WITH OPEN STRING LATCH ACTIVE ALL OUTPUTS LATCH OFF.

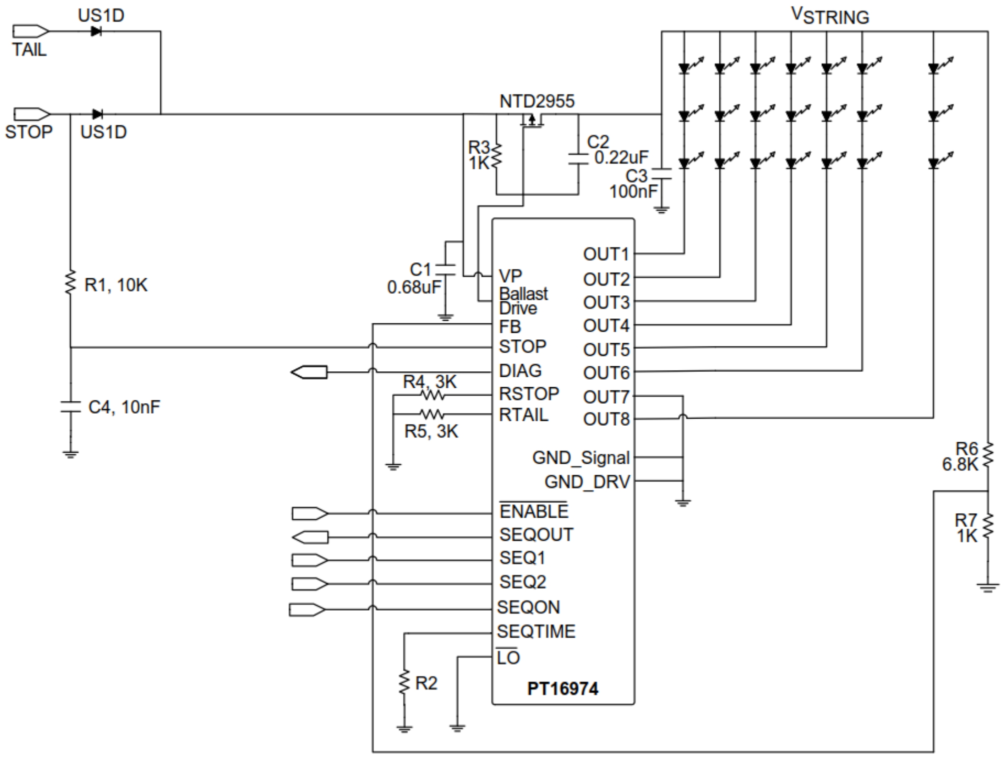


DIAG TIMING DIAGRAM WITHOUT OPEN STRING LATCH ACTIVE NO OUTPUTS ARE TURNED OFF. DIAG WILL REPORT THE STATE.



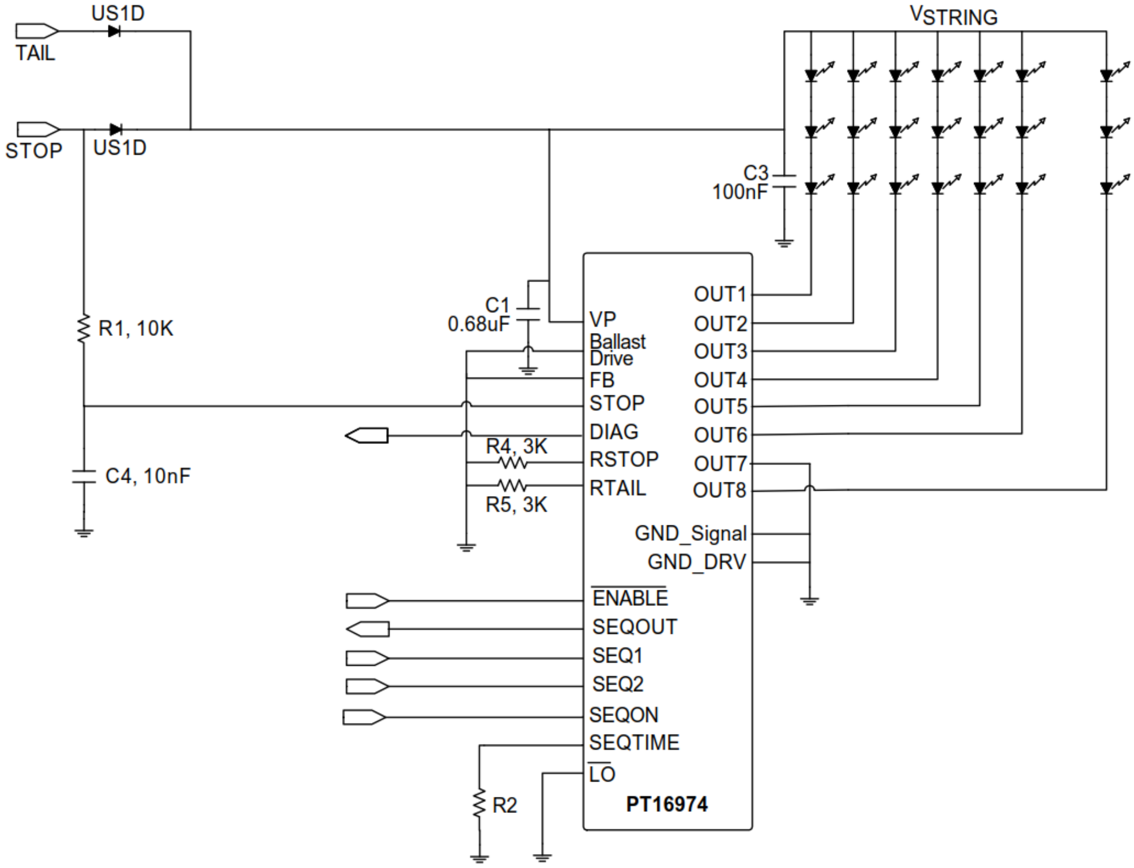
APPLICATION CIRCUITS

WITH EXTERNAL FET BALLAST TRANSISTOR



R6 and R7 set regulated voltage on V_{STRING}, V_{STRING}=7.8V.
C1 is eliminate input noise and stable VP supply. C3 is improve EMC Performance
Unused OUT pins should be shorted to ground.

WITHOUT THE FET BALLAST TRANSISTOR



When using the device without the FET ballast transistor, ground FB pin and Ballast Drive pin.

OPERATING DESCRIPTION

GENERAL

PT16974 is a linear LED driver for automotive exterior lighting. It incorporates STOP, TAIL and Turn signal functions which used in automotive Rear Combination Lighting systems and blinking functions. The driver provides 8 LED current channels and the output current up to 100mA per channel. The current setting is easily programmed by an external resistor. An optional external control for a ballast FET helps distribute the system power.
Stop and Tail mode can be switched via STOP pin logic input. When STOP is high, it's in the STOP mode, and the duty cycle of the outputs is at 100%; When STOP is low, the duty cycle of the outputs is programmed via an external resistor on the RTAIL pin. Various sequencing functionality is available using the SEQ1, and SEQ2 pins. Sequencing options include individual channels 1−8, 4 paired combinations, 2 quad combinations, and an all on delay.
A logic output (DIAG) communicates open circuit of the LED driver outputs and SEQOUT back to the microprocessor. Both DIAG and SEQOUT require a pull−up resistor for proper operation.

DIAG

DIAG pin reports fault status in logic high (requires a pull−up resistor). Fault status includes LED open circuit, RSTOP current limit, set back current Limit down 20%, and thermal shutdown. This pin can be connected to an external microcontroller or comparator to facilitate fault detection. DIAG is in logic low when normal operating. Reference Table 1 for details on logic performance.
Open circuit conditions are reported when the outputs are actively driven. When operating in STOP mode the DIAG signal is a DC signal. When operating in TAIL the DIAG signal is a PWM signal reporting open circuit when the output drive is active.

OPEN LOAD DETECTION

PT16974 incorporates open load detection function, the internal current is monitored when normal operating, and an open load is flagged when the current is 1/2 of the targeted output current. Also open load detection has an under voltage lockout feature to remove the possibility of turning off the device while it is powering up. The open load disable threshold is 7.7 V.
In order to implement the open load detection and preservation of the latch off feature for multiple IC, multiple ballast transistors in series must be used as shown in Figure 1.
Interruption of any of the series devices will provide an all off occurrence. The Vstring voltage (anode of the LED strings) is set up by the feedback in just the first device. Any subsequent devices should connect their FB pin to ground. This will remove competition of voltage regulation points of Vstring.

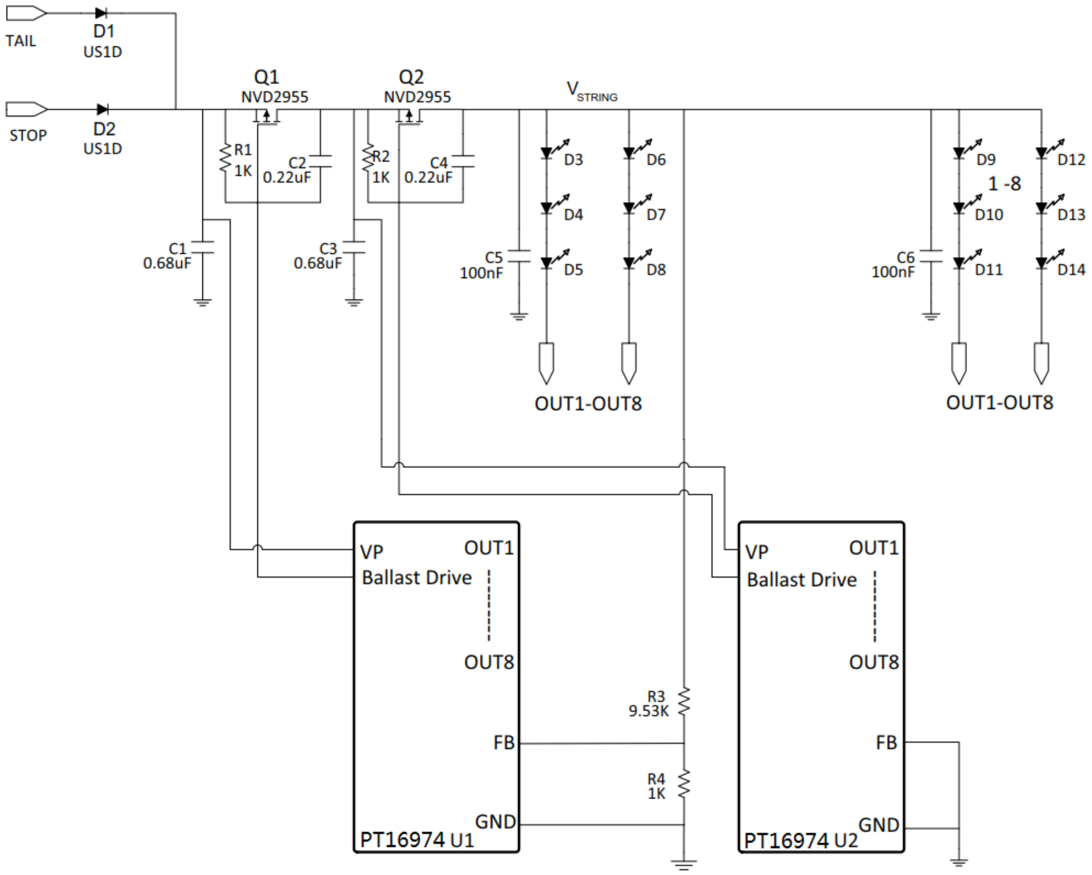


Figure1. For multiple IC application

SEQUENCING

In Turn mode, there are 4 kinds of output sequencing. Output sequencing is controlled by the SEQON, SEQTIME, SEQ1, and SEQ2 pins. The SEQON pin requires a pull-up resistor and tie this pin to logic high to enable any of the sequencing functions. With the SEQON pin in a low state, all 8 outputs turn on at the same time and SEQOUT remains high all the time (via the external pull−up resistor). The SEQ1 and SEQ2 programming pins are utilized by grounding them or leaving them floating. They follow Table 2(reference timing diagrams in Page 19 to 22). The sequence interval is defined by the delay of the ENABLE pin going low to OUT2 turning on (OUT1 turns on coincident with ENABLE). The same sequence time interval is present for each additional sequential turn−on output of the IC. When the device is operating in the sequence mode, force the ENABLE high or SEQON low to leave the sequence mode.

ENABLE going from low to high (Figure 4) will turn off all outputs. When SEQON going high to low (Figure 5 and Figure 6), the device will leave the sequence mode, and continue to operate in STOP or TAIL mode. A device which was previously in TAIL mode (STOP=0) (Figure 5) will revert to TAIL mode. A device which was previously in STOP mode (STOP=1) Figure 6 will revert to STOP mode.

Before a sequence event, SEQOUT is high impedance. After a sequence event, SEQOUT is high impedance.

Table 2. SEQUENCING COMBINATIONS

SEQ1	SEQ2	Sequencing Functionality
1	1	All on
1	0	Dual Output Combination
0	1	Quad Combination
0	0	Full 8 Channel Sequencing

0= ground; 1= floating (Internal pull-up to the internal power supply)

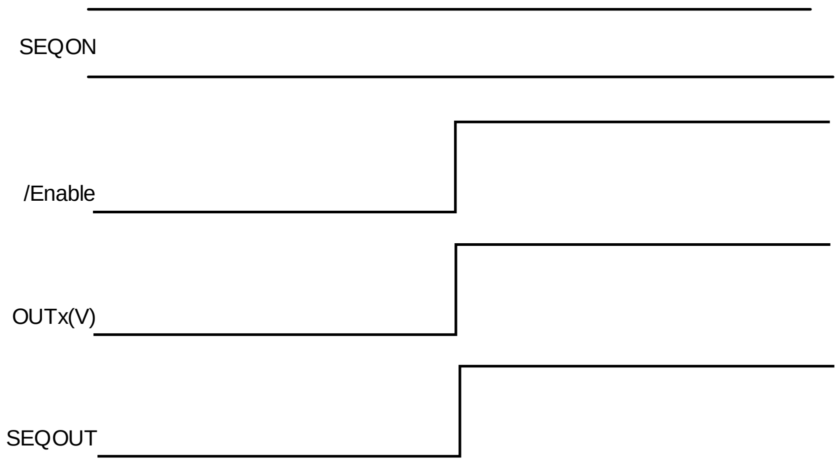


Figure 4. Sequence Interrupt from ENABLE

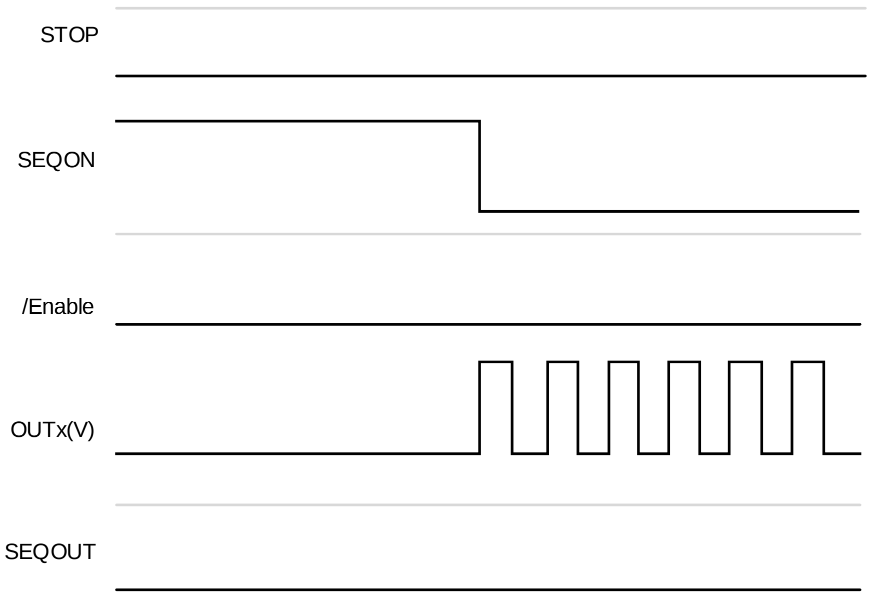


Figure 5. Sequence Interrupt from SEQON (STOP = 0)

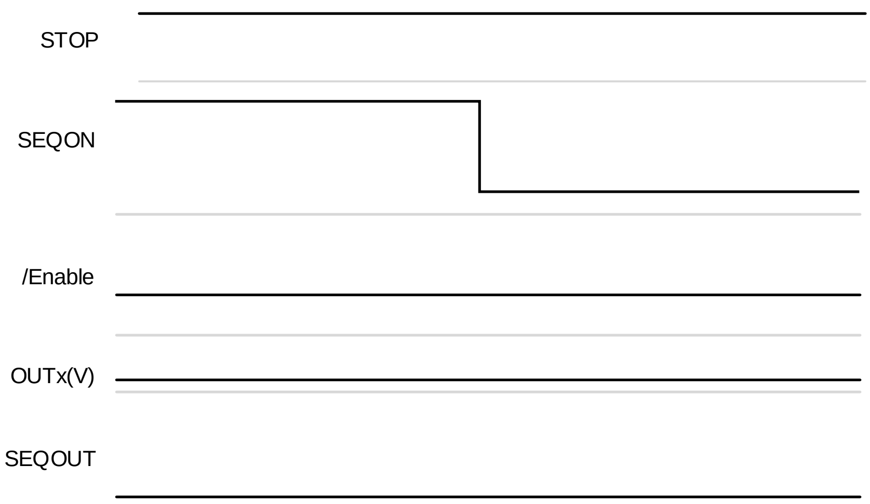


Figure 6. Sequence Interrupt from SEQON (STOP = 1)

$\overline{\text{LO}}$ (LATCH OFF) AND DIAG

Sometimes, the automotive requirements dictate that if one of the lighting outputs is an open circuit, all outputs will be turned off. This eliminates driving with partial illuminated lights. The lighting device will either display all LED strings or no LED strings at all. The option to turn all LED strings off with an open circuit detect on any of the 8 outputs is programmed by grounding the LO pin. Left this pin floating to disable this feature.
Each output has its own sensing circuitry. When an open circuit occurs on any output, latches off all 8 outputs ($\overline{\text{LO}}$ = low). There are two means to reinitiate the IC drivers in condition of keeping input mains.

1. Forcing the DIAG pin below the Open Circuit Reset Voltage (1.8 V typical).
2. Toggling the $\overline{\text{ENABLE}}$ input.

PROGRAMMABILITY

At present, using LED Strings for Rear Combination Lamps applications is a common configuration. PT16974 provides 8 matched outputs allowing individual LED string drive with current set by a single resistor. Output currents are matched within ±4% at high temperature.
When STOP=1, set the output current using equation 1. When STOP=0, modulates the output currents at a duty cycle programmed using equation 2.
Current limiting on RSTOP limits the output current which can be referenced from the RSTOP Pin. If the setting value of the output current exceeds 100mA, the RSTOP Current Limit will set the actual output current to less than 100mA, and the DIAG Pin will go high. This helps limit output current for this type of fault.
The modulated output currents provide the dimmed tail illumination function and assure a fixed brightness level for tail lamps. The typical fixed PWM frequency is 800Hz, it allows flicker−free illumination. PWM control is the preferred method for dimming LEDs.
The diagnostic function allows to detect an open circuit in any one of the output circuits. The active−low diagnostic output (DIAG) is coincident with the STOP input and the ON state in the tail mode. DIAG goes high if an open load is detected in any LED string when STOP is high.

OUTPUT CURRENT PROGRAMMING

For quick design of the stop current, refer Figure 7 to choose programming resistor (RSTOP) value. Refer Figure 8 Performance Graph (Duty Cycle vs. RTAIL) to choose a typical value programming resistor for output duty cycle (with a typical RSTOP value of 3KΩ). The duty cycle is dependent on both RSTOP and RTAIL values. RSTOP should be the first consideration because the stop current is only dependent on this value.

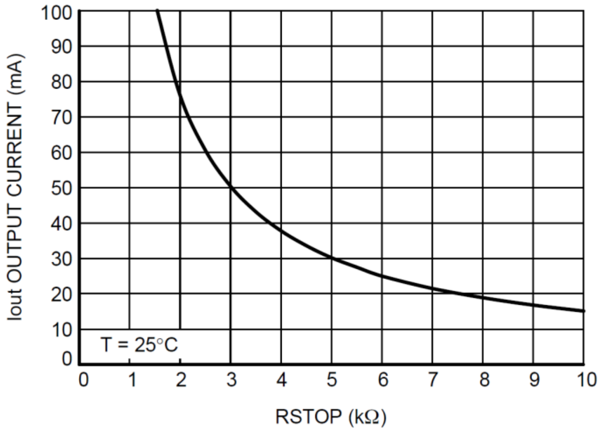


Figure 7.Iout vs. RSTOP

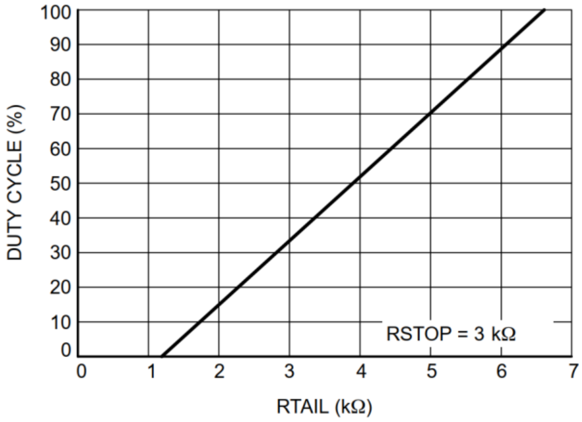


Figure 8.Duty Cycle vs. RTAIL

Equation 1 can be used to calculate a typical value of STOP current and used for worst case analysis. Output Current is directly tested per the electrical parameter table to be ±10% at room and high temperature.

$$I_{OUTX} = 150\ \mathrm{X}\ \frac{\mathrm{RSTOP\_Bias\_Voltage}}{\mathrm{RSTOP}}\ (\mathrm{mA})$$ Equation 1

RSTOP Bias Voltage = 1 V (typ)

SET THE DUTY CYCLE (DC) USING RTAIL

The equation below can be used to calculate a typical value of PWM duty cycle.

RTAIL = 1.8   RSTOP(DC + 0.22) Equation 2

DC = duty cycle expressed in fractional form. (e.g. 0.50 is equivalent to 50% duty cycle) (ground RTAIL when using external modulation)
Duty Cycle will be varied by changing the RTAIL Voltage and RTAIL Bias Current (generated from the current through RSTOP).
Voltage errors encompass generator errors (0.4 V to 2.2 V) and comparator errors and are included in testing as the Duty Cycle. Typical duty cycle measurements are 5% with RTAIL = 0.49 V and 70% with RTAIL = 1.66 V.
RTAIL Bias Current errors are measured as RTAIL Bias Current and vary as 290 μA (min), 330 μA (typ), and 370 μA (max) with RSTOP = 3 KΩ.
The error duality originating from both the internal current source generated on the RSTOP pin and the comparator voltage thresholds of the RTAIL pin combined with the choice of duty cycle levels make it difficult to specify duty cycle minimum and maximum limits, but worst case conditions can be calculated when considering the variation in the voltage threshold and current source. Duty Cycle variation must include the direct duty cycle as specified in the electrical parameter table plus an additional error due to the Irstop current which generates this voltage in the system.

SEQUENCE AND RE−ENABLE TIME PROGRAMMING

Using a resistor from the SEQTIME pin to ground to program the Sequence time. Refer Figure 9 to choose programming resistor for the expected time. Acceptable values for the resistor are between 1 K and 10 K. These provide 50 msec and 500 msec times respectively.
The program resistor used can be calculated by using the electrical parameters

1. Sequence Time / $R_{SEQTIME}$

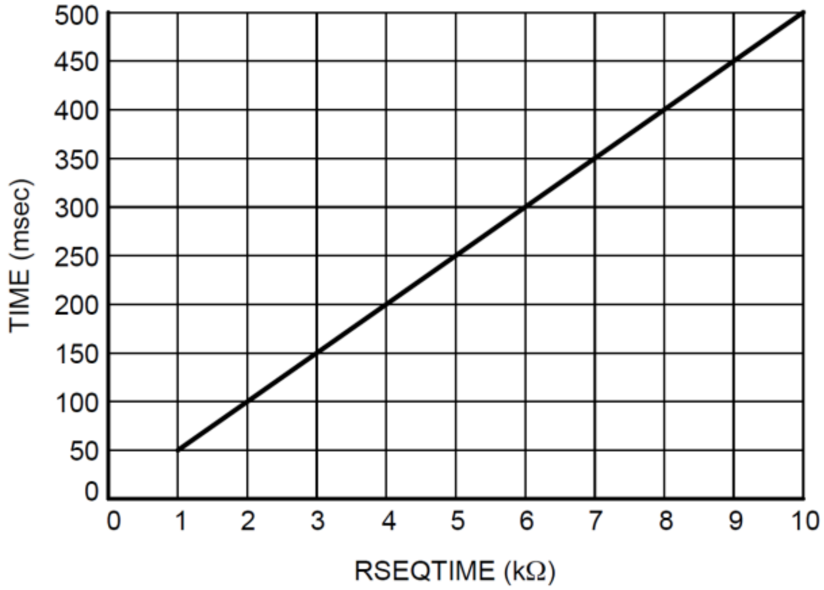


Figure 9. Sequence Time. vs. $R_{SEQTIME}$

$$\text{Sequence Time} = \frac{\text{Sequence\_Time}}{R_{SEQTIME}} \text{ X } R_{SEQTIME}$$

Example:
Electrical Parameter (typ) Sequence Time / $R_{SEQTIME}$ = 50 msec/kΩ
$R_{SEQTIME}$ = 10 kΩ
Sequence Time = 50 * 10 = 500 msec

The Sequence Re−Enable Time uses the same internal timer as the Sequence interval Time. The Sequence Re−Enable Time is provided to prevent an immediate feedback triggering in a daisy chain setup. Reference Figure 14, Figure 15 and Figure 16 for details.
PT16974 has a variable sequence interval time according to different setting of SEQ1 and SEQ2.

$$\text{Sequence Re} - \text{Enable Time} = \text{Sequence Interval Time} = \frac{\text{Sequence Re} - \text{Enable Time}}{R_{SEQTIME}} \text{ X } R_{SEQTIME} \Big/ \text{Output Cluster}$$

**Output Cluster = 1/2/4/8*

Example:
Electrical Parameter (typ) Sequence Re−Enable Time / $R_{SEQTIME}$ = 50 msec/kΩ
$R_{SEQTIME}$ = 10 kΩ
SEQ1=0,SEQ2=0 (Page 20), individual 8 output channel, Output Cluster= 8, Sequence interval time= 500/8=62.5ms
SEQ1=1,SEQ2=0 (Page 21), dual output combination, Output Cluster= 4, Sequence interval time= 500/4=125ms

PARALLEL OUTPUTS

Each output provides 100mA current for LED string. In order to meet the current of single LED string, the device allow to parallel combine any number of outputs. Combining all 8 outputs will allow for a maximum system level string current design of 800mA.

UNUSED OUTPUTS

If there are unused output channels, connect the unused outputs to ground. PT16974 detects the condition during power−up using the open load disable threshold and disables the open circuit detection circuitry. Refer the Figure10 and Figure 11，the diagrams highlight the impacts on the sequencing function when an output is not used. For example, shown as Figures 10, set SEQ1=0 and SEQ2=0, and OUT7 is not used (connect to ground). The subsequent output (OUT8) has been pulled in (in time) as shown by the 1st arrow. Accordingly, the SEQOUT signal has also been pulled in (in time) as shown by the 2nd arrow. For instances which are coupled with others (in time) (e.g. SEQ1=1 and SEQ2=0, OUT7 is grounded), there is no change in the ensuing waveforms. Figure 11 shows there is no impact for channel 8 when OUT7 is not used.

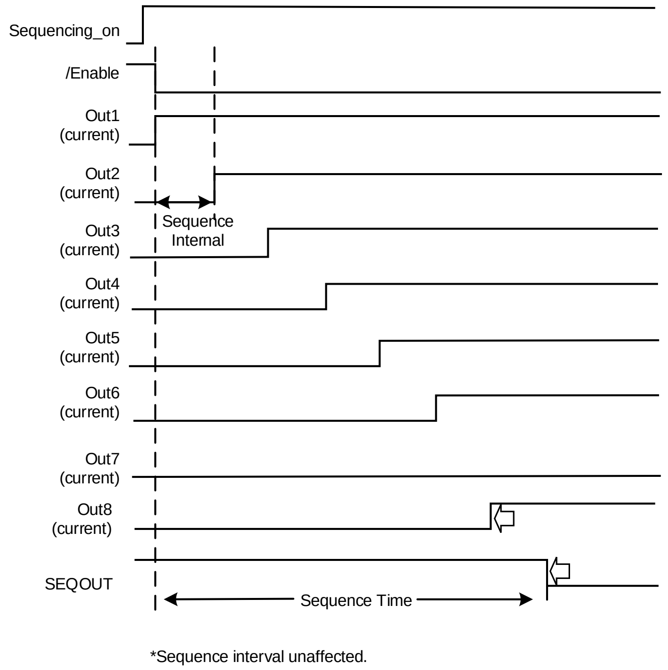


Figure 10. Unused Output time shift (SEQ1 = 0, SEQ2 = 0)

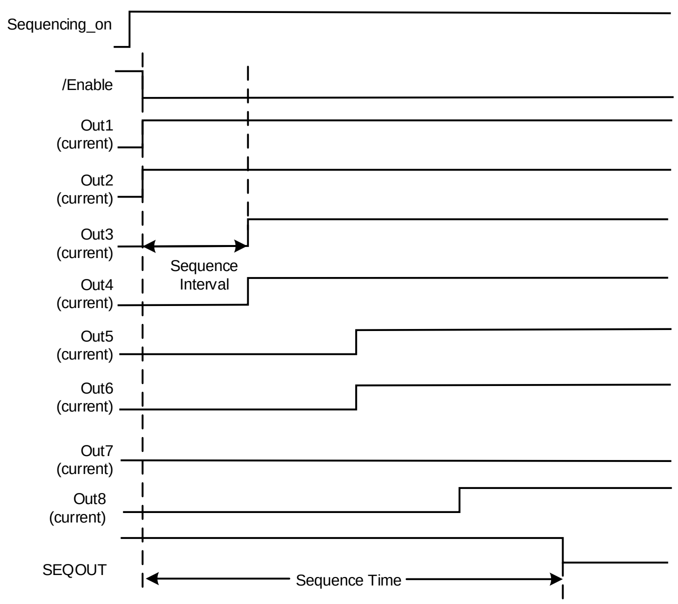


Figure 11. Unused Output No Time Shift (SEQ1 = 1, SEQ2 = 0)

DAISY CHAIN

To obtain better sequencing display, using multiple devices to design a daisy−chain in TURN mode as shown in Figure 12. Connections allow for a continuous stream of devices including all delays attributed to the previous sequence timing events from the previous integrated circuits. This setup ripples the signal through all devices until all devices are on. The example shows 3 devices, but as many devices as desired may be used.
Once the SEQOUT signal reaches the end of the daisy chain string, all devices turn off. The sequence starts again via the retriggerable function, shown as Figure 14 and Figure 15. PT16974 device utilizes a Sequence Re−Enable time whereby a device turned off via the ENABLE pin will not turn back on until the Sequence Re−Enable time has passed. This allows all devices to turn off for a discernible time before reinitiating the sequence. Using a capacitor to extend the time at the end of the sequence.
Figure 16 shows the timing diagram associated with the setup shown in Figure 14. When each PT16974 device receives a turn on signal through its ENABLE pin, the output turns on the LED. The SEQOUT pin goes low with an internal delay response, delays the turn-on of the next sequential device. Figure 15 shows an alternative setup using NFET transistors instead of PFET transistors.
SEQOUT pin incorporates an open circuit detection, shown as Figure 13, implement the detection of open circuit condition, report the condition back to the controller via the DIAG pin, and turn off all driver ICs in the daisy-chain eliminating any spurious lighting events. SEQOUT is not active during STOP/TAIL modes (SEQOUT=0).

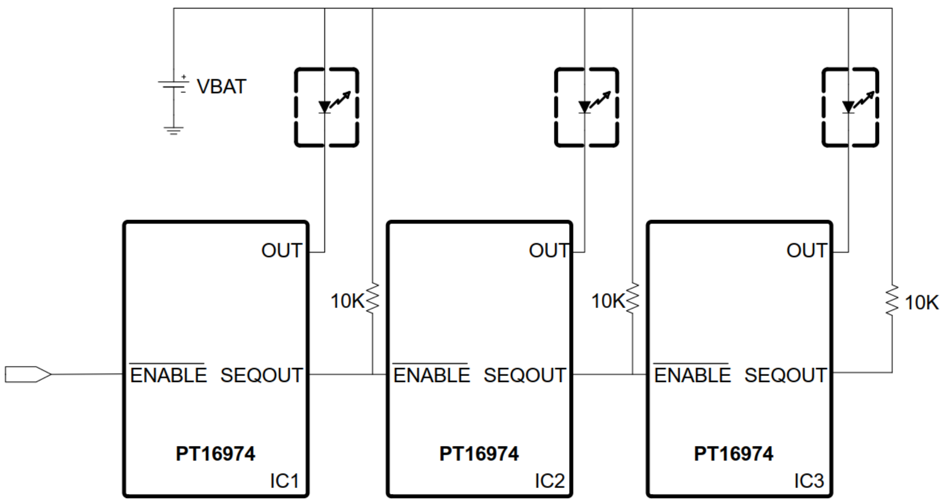


Figure 12. Daisy Chain Sequencing

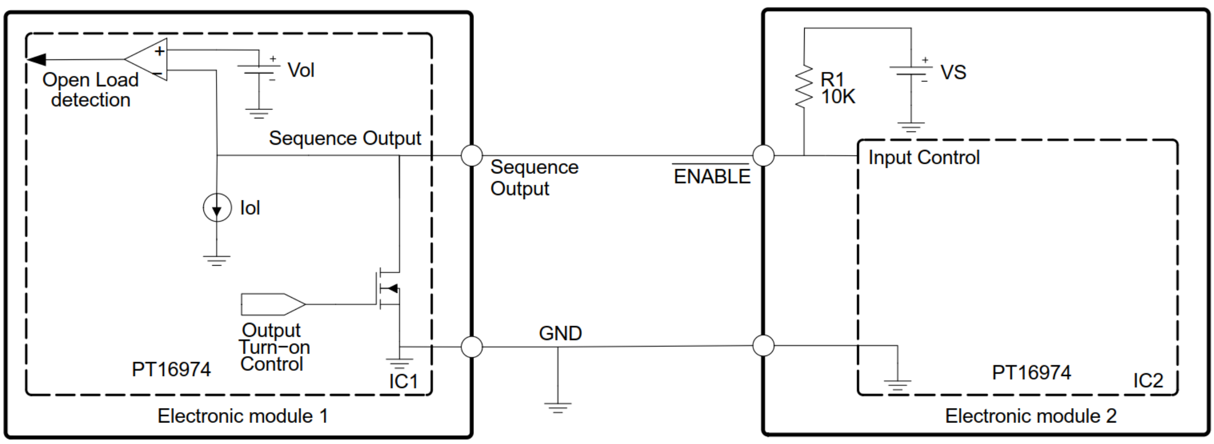


Figure 13. Daisy Chain Interface between Multiple ICs

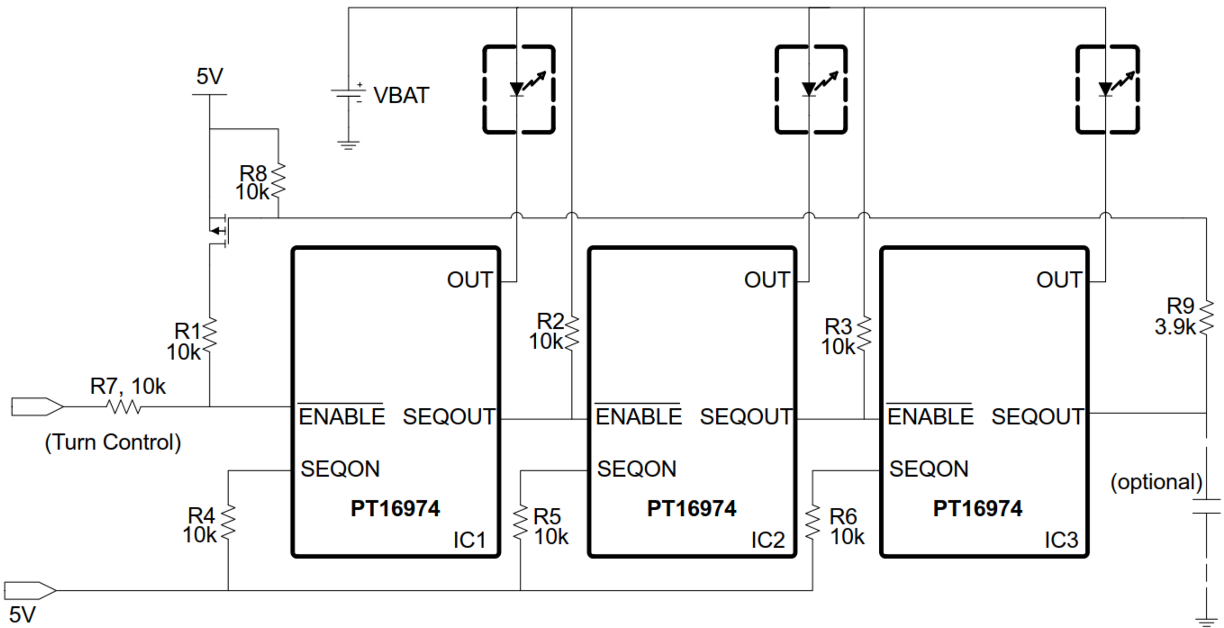


Figure 14. Retriggerable Daisy Chain Sequencing using the Sequence Re−Enable Time

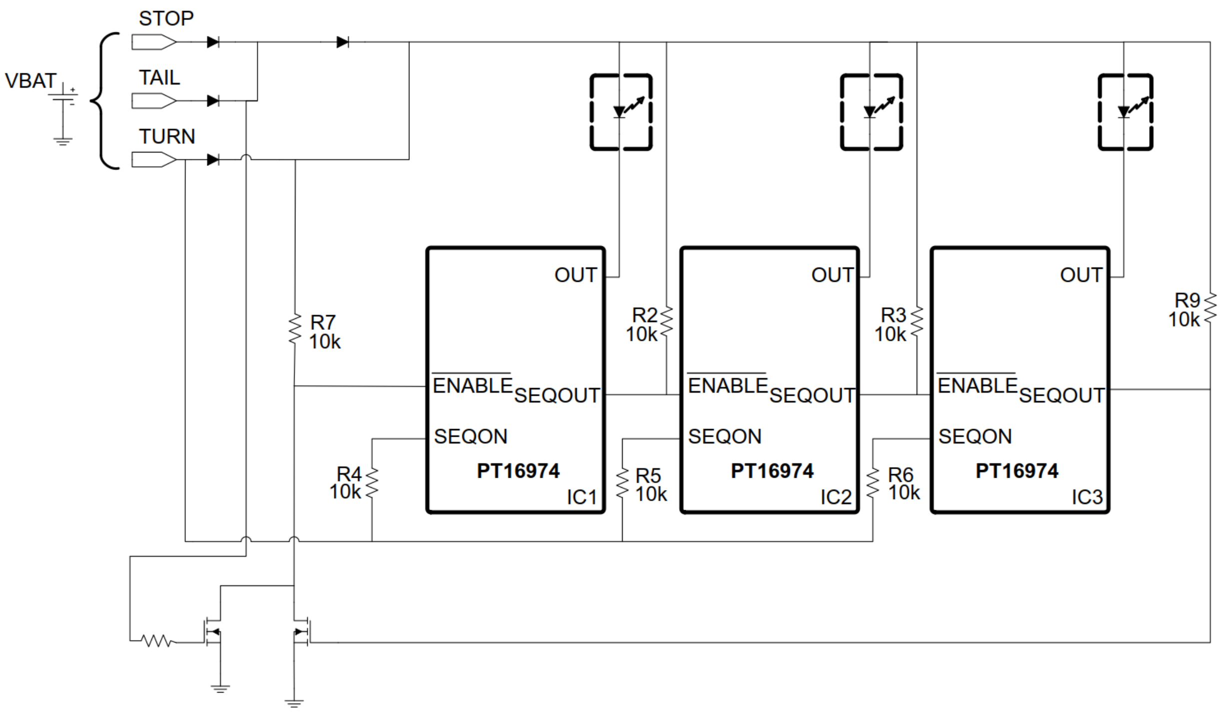


Figure 15. Alternate Retriggerable Daisy Chain Sequencing using Sequence Re−Enable Time

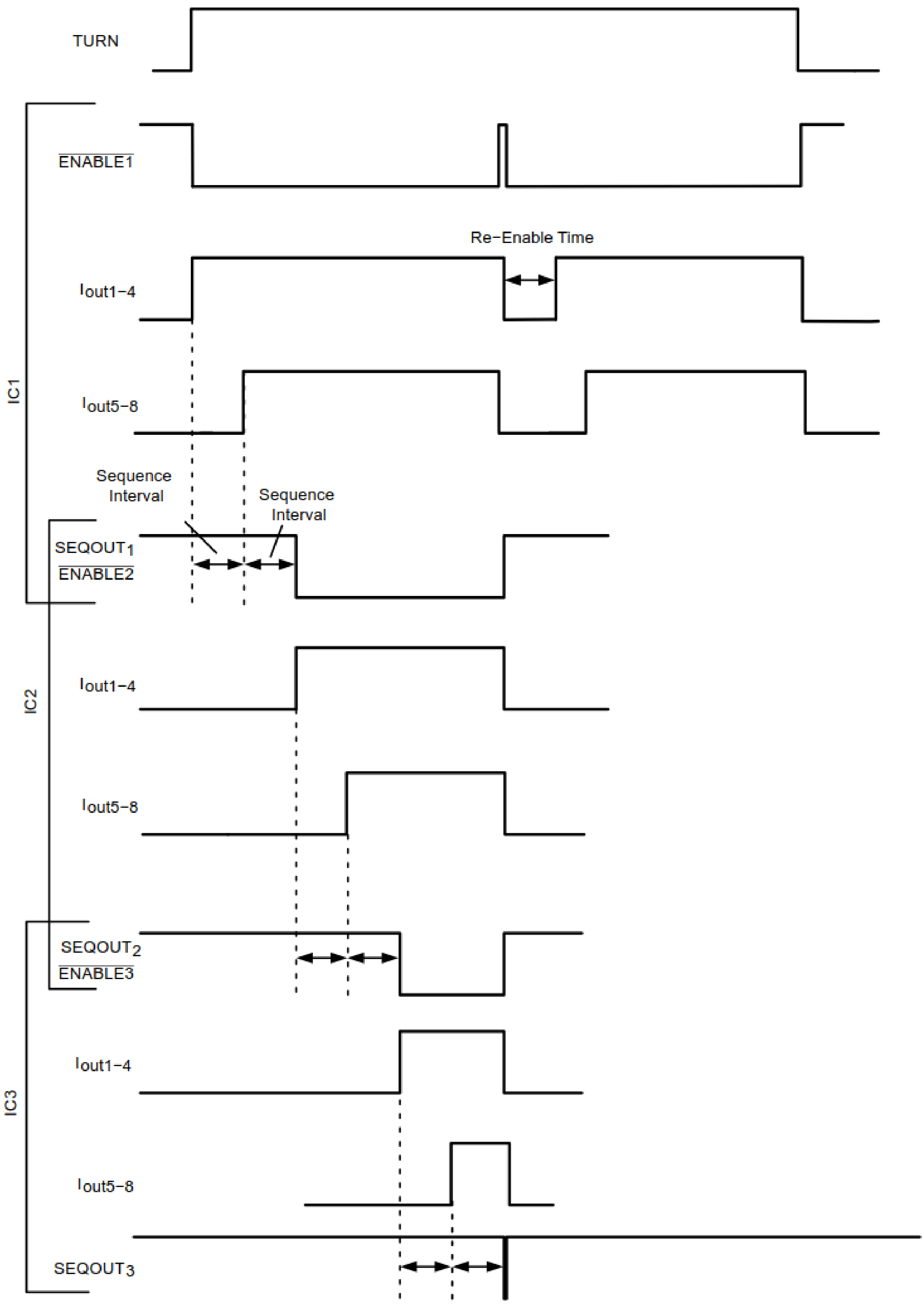


Figure 16. Sequencing Timing Diagram with Re−Enable Time Delay

BALLAST DRIVE

Using an external FET device helps distribute the system power. The voltage at the top (anode) of the LED strings (Vstring) is regulated by a DC voltage regulation system. This helps to limit the power in the PT16974 by setting the voltage on the OUTx pins specific to each customer application. The Ballast Drive pin provides the drive in the feedback loop from the FB pin. In steady state, the voltage is regulated at the feedback voltage (FB). The voltage of FB pin is sourced from voltage divider of the Vsting voltage. Unlike other systems, the ballast drive current does not turn off in a leakage state when turned off (FB high), but instead provides 1mA of current, to provide a faster response of the system loop.

RSTOP OVER CURRENT PROTECTION

The RSTOP pin incorporates Over Current Protection. The device performance could cause excessive high current if without protection, and potential damage to the external LEDs. Detection of the RSTOP over current event (RSTOP to ground) is 1mA and is current limited to 2.2mA. Output drive currents will limit to typically 65 mA.
PT16974 still works during a short circuit of RSTOP pin. I_{OUT} is decreased by reducing the voltage on the RTAIL pin to 2/3 of normal operation during the STOP short condition and the TAIL duty cycle is reduced to less than 40%.

SET BACK CURRENT

For providing consistent LED light output at low line voltage, the low dropout is a key attribute, because automotive battery systems have wide variations in line supply voltage. The set point resistor of PT16974 lies outside the LED load path and aids in the low dropout capability, unlike adjustable regulator based constant current source schemes where the set point resistor resides in the load path.
PT16974 incorporates Setback Current Limit function, this function is enabled during the high input voltage. When VP > 17.2V(typ), the OUTx current is reduced resulting in lower power dissipation on the IC during a setback current limit event. In this way the PT16974 can operate in extreme conditions and still provide a controlled level of light output. This abnormal condition is reported on the DIAG Pin when the drive current is reduced to 80% of the rated current.
Activation of the set back current feature provides a roll−off rate of −8%/V.

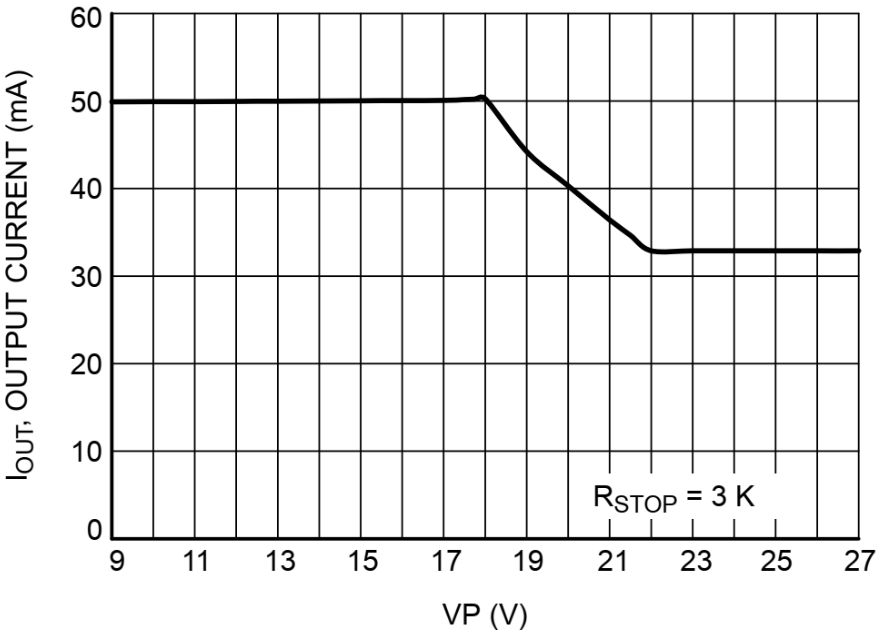


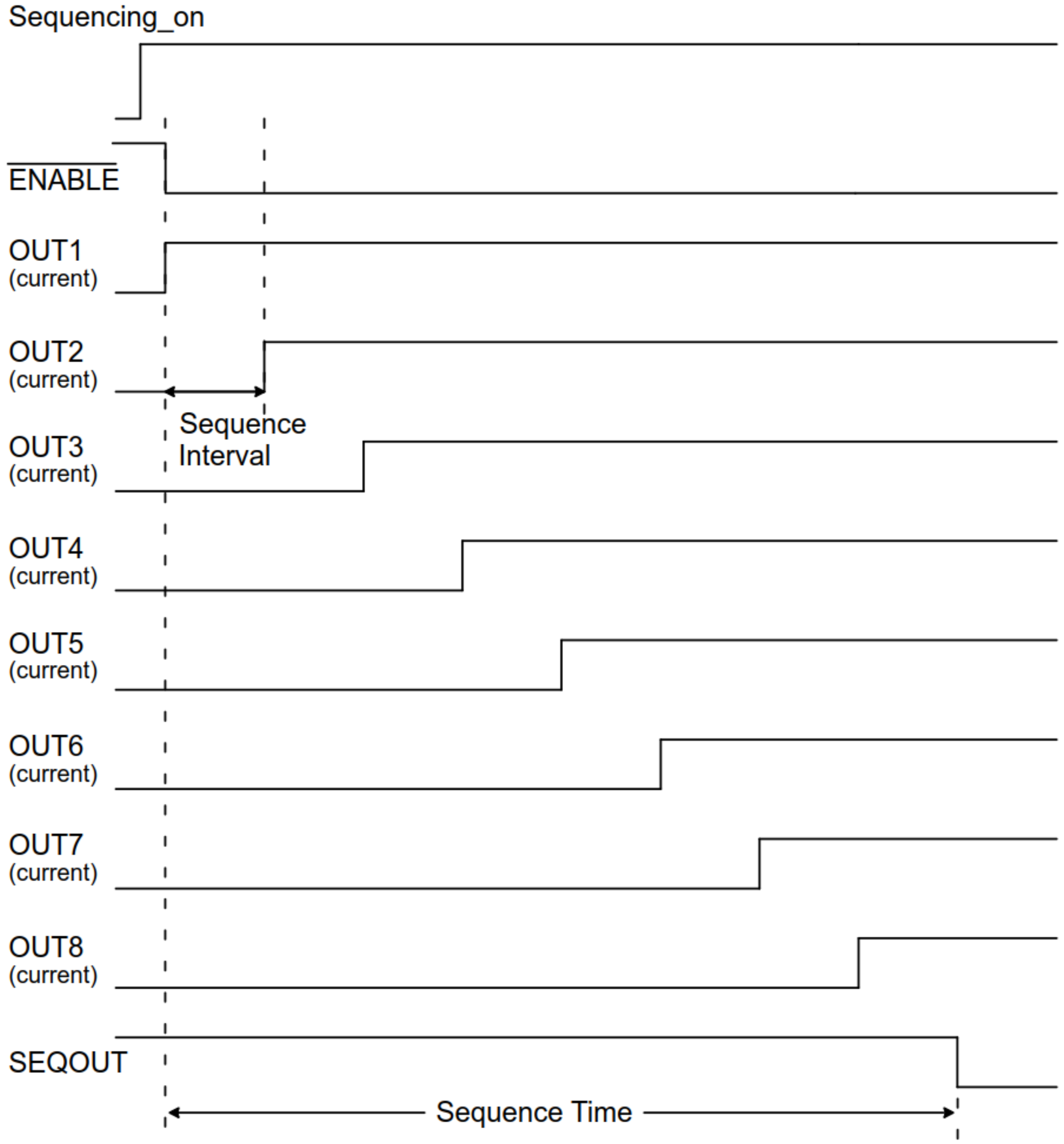
Figure 17. I_{OUT} vs. VP

SEQUENCE PROGRAMMING TIMING DIAGRAMS

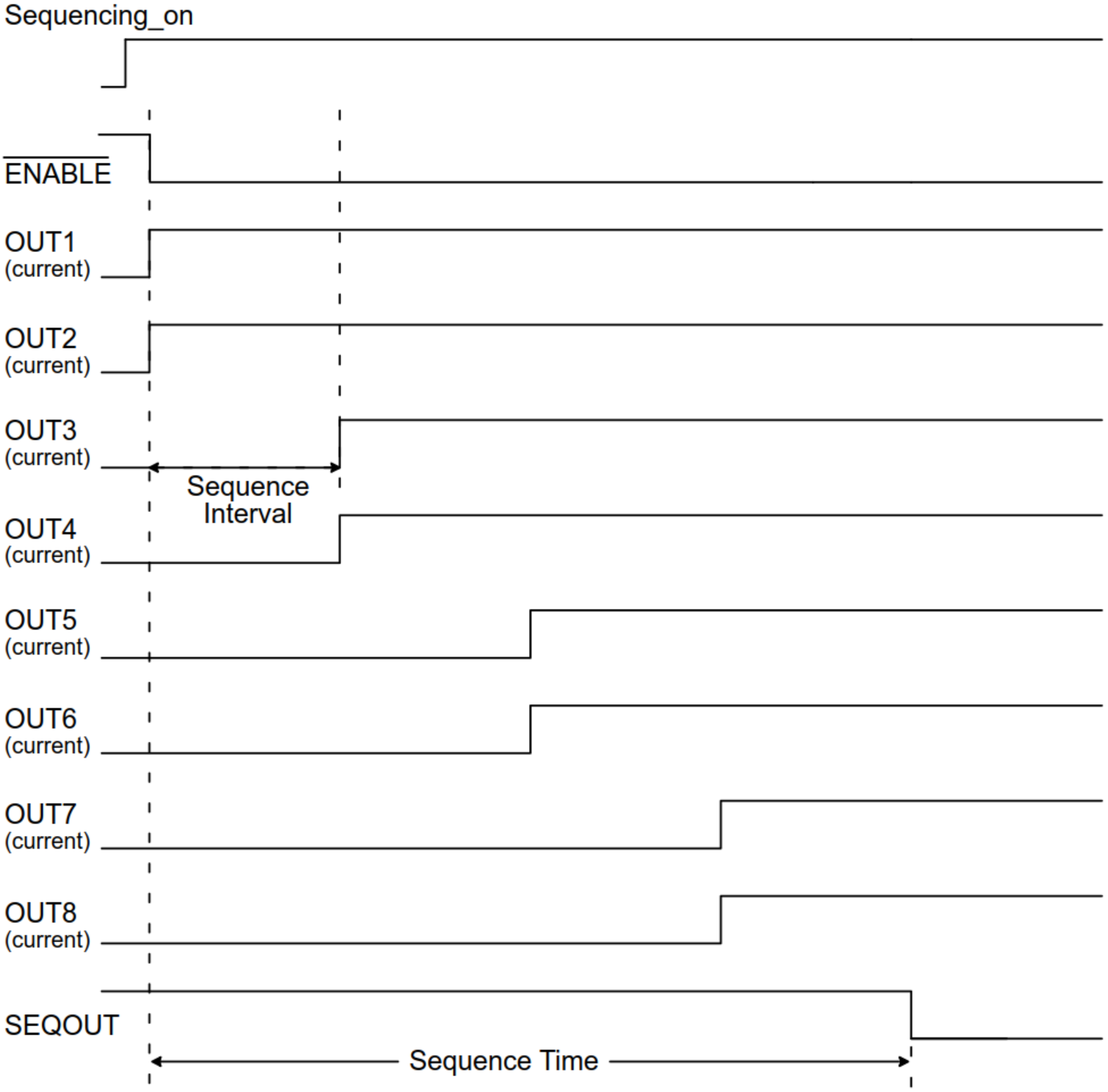
The four timing diagrams show the options available for sequencing of the 8 outputs dependent on the state of SEQ1 and SEQ2.

- 8 individual sequence intervals.
- 4 pairs of sequence intervals.
- 2 quads of sequence intervals.
- 1 single sequence interval.

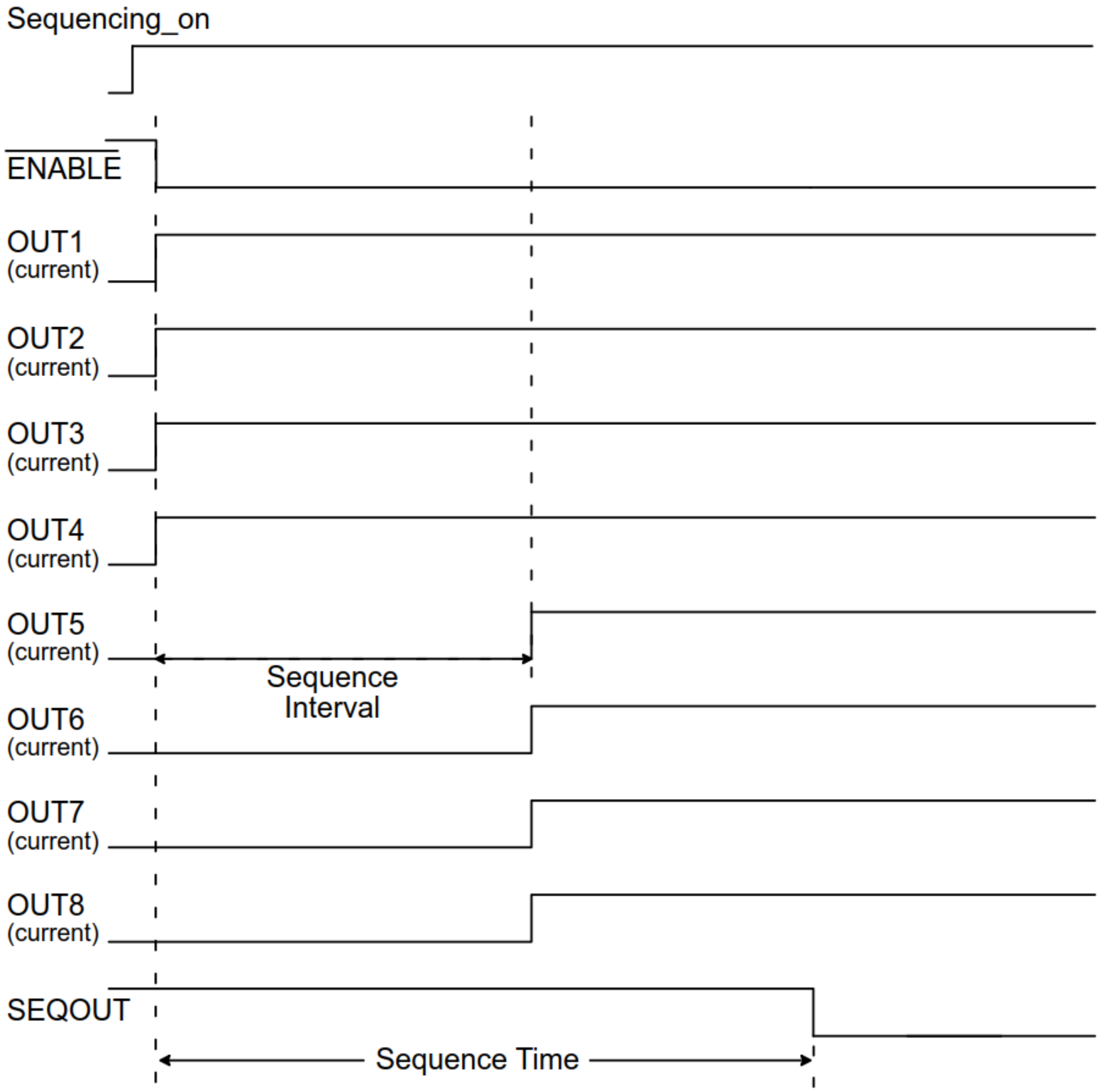
SEQUENCING TIMING DIAGRAM (SEQ1 = 0, SEQ2 = 0)



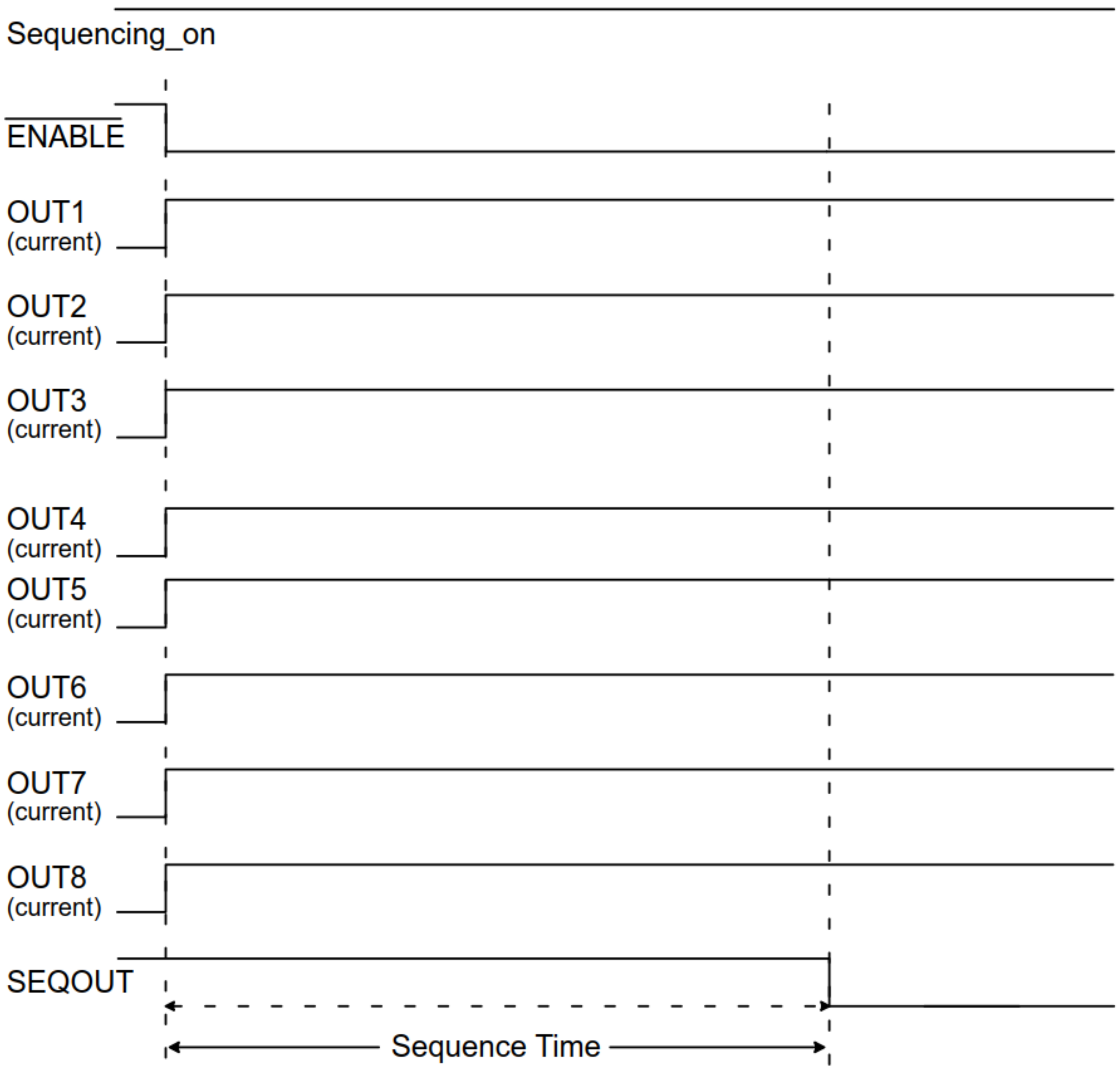
SEQUENCING TIMING DIAGRAM (SEQ1 = 1, SEQ2 = 0)



EQUENCING TIMING DIAGRAM (SEQ1 = 0, SEQ2 = 1)



SEQUENCING TIMING DIAGRAM (SEQ1 = 1, SEQ2 = 1)



The sequencing function is triggered by a logic level high to low signal on the ENABLE pin.
0=ground
1=floating

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Supply Voltage	VP, Ballast Drive, STOP, DIAG, ENABLE, SEQON, SEQOUT	-0.3 ~ 45	V
Input Voltage	RTAIL, RSTOP, FB, SEQTIME, SEQ1, SEQ2, LO	-0.3 ~ 5.5	V
Output Pin Voltage	OUTX	-0.3 ~ 45	V
Output Pin Current	OUTX	200	mA
DIAG Pin Current	DIAG	10	mA
Operating Temperature	Tj	-40 ~ +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ATTRIBUTES

Characteristic		Value
ESD Capability		
Human Body Model (HBM)		± 2000V
Charge Device Mode (CDM)		± 600 V
Storage Temperature		−55 to 150°C
Moisture Sensitivity		MSL3
Package Thermal Resistance (Note1)		
HSSOP24	Junction–to–Board, $R_{\theta JB}$	9.4°C/W
	Junction–to–Ambient, $R_{\theta JA}$	28°C/W
	Junction–to–Case, $R_{\theta JC}$	15°C/W

Note1: Test condition: Refer to JESD51 regulation

1) Board Laver=4 Lavers, Material=FR-4, Board thickness=1.6mm

2) Board area=76.2mm X114.3mm, metal coverage area=74.2mmX74.2mm

3)Copper layer thickness: top/bottom layer=70um, 2nd and 3rd layer=35um

4) Copper coverage ratio: top/bottom layer=20%, 2nd and 3rd layer=90%

ELECTRICAL CHARACTERISTICS

(6V < VP < 16 V, STOP = VP, RSTOP = 3 kΩ, RTAIL = 1.6 kΩ, RSEQTIME = 5.1 kΩ, −40°C ≤ TJ ≤ 150°C, unless otherwise specified.)

Parameter	Test Condition	Min	Typ	Max	Unit
GENERAL PARAMETERS					
Quiescent Current (IOUTx = 50 mA)					
STOP Mode	VP = 16 V		7	12	mA
Tail Mode	VP = 16 V		7	12	
Fault Mode	VP = 16 V, STOP = 0 V, OUTx = 0 mA, Disconnected output			8.0	
Driver Ground Pin Current (pin13)	IOUT1 to IOUT8 = 50 mA		400	500	mA
Open Load Disable Threshold		7.2	7.7	8.2	V
Open Load Disable Hysteresis			200		mV
Output Under Voltage Lockout		4.5	4.9	5.3	V
Output Under Voltage Lockout Hysteresis			100		mV
CURRENT SOURCE OUTPUTS					
Output Current	OUTX = 0.5 V	45	50	55	mA
	OUTX = 1 V, RSTOP = 1.5 K	90	100	110	
Maximum Regulated Output Current	0.5V to 16V	100			mA
Current Matching	$\left[\frac{2IOUTx(min)}{IOUTx(min)+IOUTx(max)}-1\right]x\,100$ $\left[\frac{2IOUTx(max)}{IOUTx(min)+IOUTx(max)}-1\right]x\,100$	-4	0	4	%
Line Regulation	9 V ≤ VP ≤ 16 V		1.2	6.0	mA
Open Circuit Detection Threshold	25 mA	25	50	75	% of Output Current
	50 mA	35	50	65	
Current Slew Rate	Iout = 44 mA, 10% to 90% points		15	20	mA/μs
Overvoltage Set Back Threshold	@ 99% Iout	16.0	17.2	18.4	V
Overvoltage Set Back Current	VP = 20 V (Note 2)		78		%Iout
Diag Reporting of Set Back Current			80		%Iout
Output Off Leakage	$\overline{\text{ENABLE}}$ =high			1	μA
FET DRIVER					
Ballast Drive DC Bias	FB = 1.5 V, Ballast Drive = 3 V		1.0	2.4	mA
Ballast Drive Sink Current	FB = 0.5 V, Ballast Drive = 3 V	4	15	20	
Ballast Drive Reference Voltage		0.92	1.00	1.08	V
STOP / $\overline{\text{ENABLE}}$ / SEQON LOGIC					
Input High Threshold		0.75	1.4	1.75	V
Input Low Threshold		0.70	1.2	1.44	V
V_{IN} Hysteresis		100	250	400	mV
Input Impedance	Vin = 14 V	120	200	300	KΩ
SEQ1 / SEQ2 / $\overline{\text{LO}}$ LOGIC					
Input High Threshold		0.75	1.4	1.75	V
Input Low Threshold		0.70	1.2	1.44	V
V_{IN} Hysteresis		100	250	400	mV
Input Pull−up Current	SEQx = 0 V	5	10	20	μA
CURRENT PROGRAMMING					
RSTOP Bias Voltage	Stop current programming voltage	0.94	1.00	1.06	V
RSTOP K multiplier I_{OUTX}/I_{RSTOP}			150		-

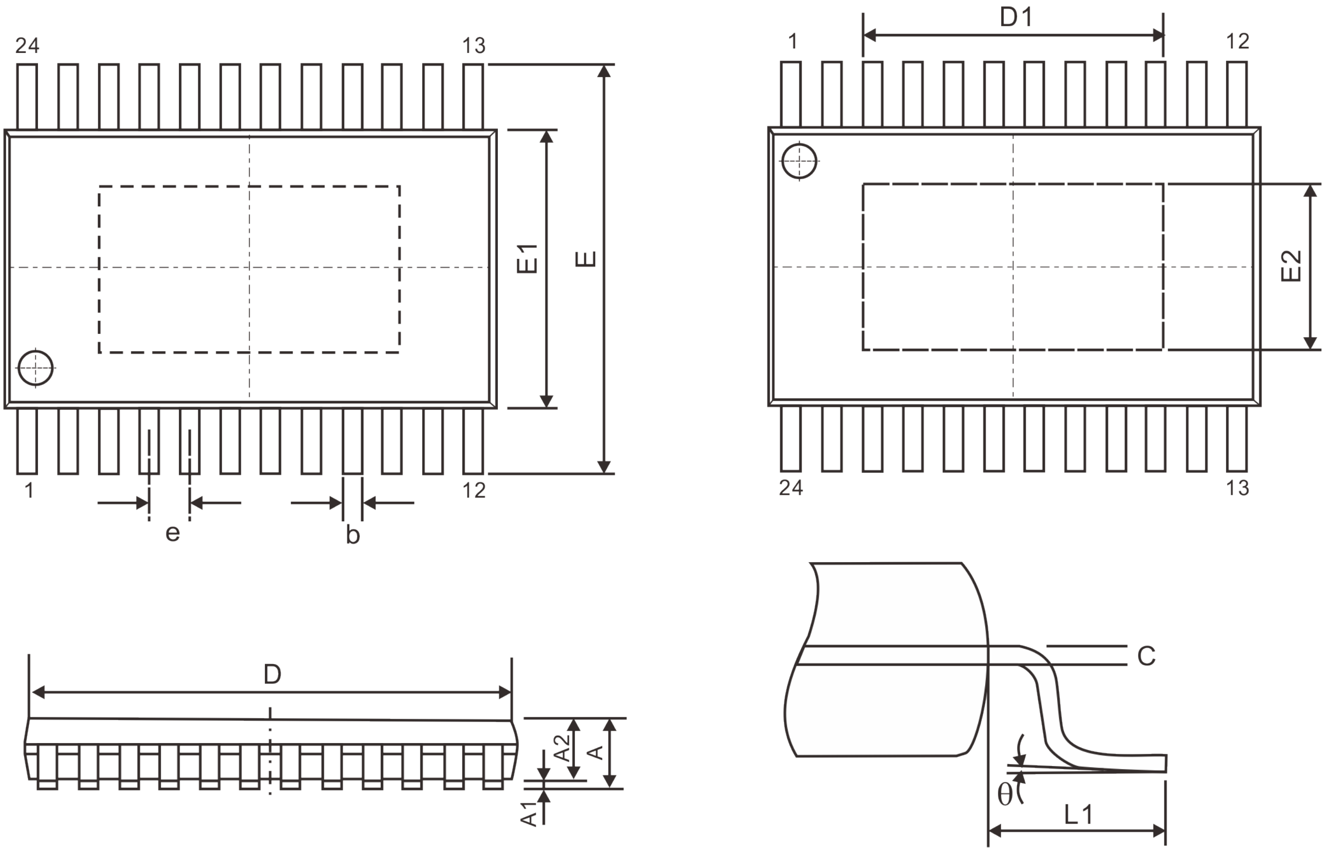
Parameter	Test Condition	Min	Typ	Max	Unit
RSTOP Over Current Detection	RSTOP = 0 V	0.70	2.00	4.00	mA
RTAIL Bias Current	Tail duty cycle programming current	290	330	370	μA
Tail Duty Cycle		5		100	%
SEQTIME Voltage		0.94	1.00	1.06	V
DIAG / SEQOUT OUTPUT					
Output Low Voltage	Output Active, I_{DIAG} = 1 mA		0.1	0.40	V
DIAG Output Leakage	V_{DIAG} = 5 V			10	μA
Open Load Reset Voltage on DIAG		1.6	1.8	2.0	V
SEQOUT Open Load Detection Threshold Voltage		0.70	0.80	0.90	V
SEQOUT Open Load Detection Sink Current		10	20	35	μA
AC CHARACTERISTICS					
Stop Turn−on Delay Time	V(STOP) > 1.75 V to I(OUTx) = 90%		14	45	μS
Stop Turn−off Delay Time	V(STOP) < 0.75 V to I(OUTx) = 10%		14	45	μS
PWM Frequency	STOP = 0 V	400	800	1200	Hz
Open Circuit to DIAG Reporting	4.8 mA pull−up to VP, V(DIAG) >1.5 V	1	2	4	μS
Sequence Time / $R_{SEQTIME}$	SEQTIME = 1K to 10K	44	50	52.5	ms/KΩ
Sequence Re−Enable Time / $R_{SEQTIME}$	SEQTIME = 1K to 10K	44	50	52.5	ms/KΩ
VP Turn−on Time		0.55	0.80	1.20	ms
THERMAL LIMIT					
Thermal Shutdown	Note 1	150	175		°C
Thermal Hysteresis	Note 1		25		°C

Notes:

1. Designed to meet these characteristics over the stated voltage and temperature recommended operating ranges, though may not be 100% parametrically tested in production.
2. The output current degrades at a rate of 8%/V.

PACKAGE INFORMATION

HSSOP24



Symbol	Dimensions(mm)		
	Min.	Nom.	Max.
A	1.346	1.626	1.753
A1	0.102	-	0.250
A2	-	-	1.500
D	8.560	8.661	8.738
D1	3.023	-	3.708
E	5.791	5.994	6.198
E1	3.810	3.912	3.988
E2	2.057	-	2.591
b	0.203	-	0.305
c	0.178	-	0.254
e	0.635 BSC		
L	0.406	0.635	1.270
L1	1.041 (BSC)		
θ	0°	-	8°

Notes:

1. Refer to JEDEC MO-137 AE
2. Unit: mm

IMPORTANT NOTICE

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