

DESCRIPTION

The PT2475 is a quad DMOS full-bridge driver capable of driving up to two stepper motors or four DC motors. Each full-bridge output is rated up to 1.2A and 36V. The PT2475 includes fixed off-time pulse width modulation (PWM) current regulators, along with 2-bit nonlinear DACs (digital-to-analog converters) that allow stepper motors to be controlled in full, half, and quarter steps, and DC motors in forward, reverse, and coast modes. The PWM current regulator uses mixed decay mode for reduced audible motor noise, increased step accuracy, and reduced power dissipation.

Internal synchronous rectification control circuitry is provided to improve power dissipation during PWM operation.

Protection features include thermal shutdown with hysteresis, under-voltage lockout (UVLO) and crossover current protection. Special power up sequencing is not required.

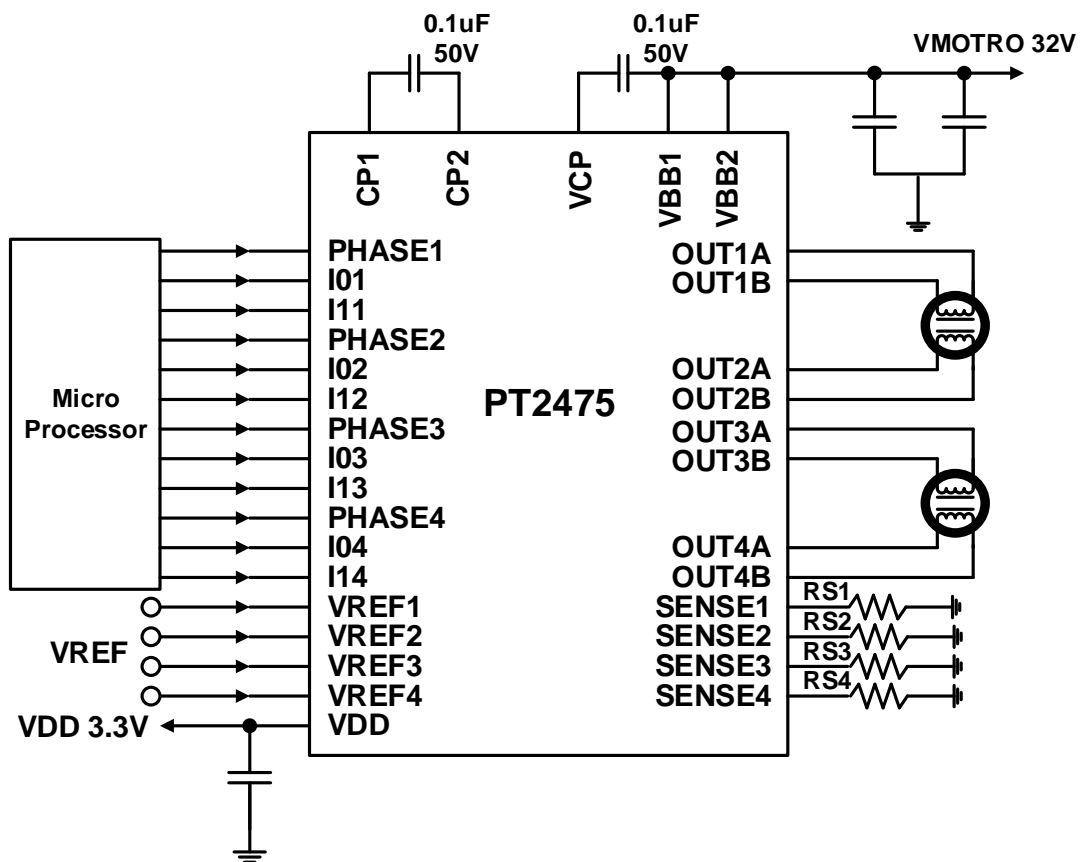
FEATURE

- 36V output rating
- 4 full bridges
- Dual stepper motor driver
- High current outputs
- 3.3 and 5V compatible logic supply
- Synchronous rectification
- Internal under-voltage lockout (UVLO)
- Thermal shutdown circuitry
- Crossover-current protection
- Low profile QFN package

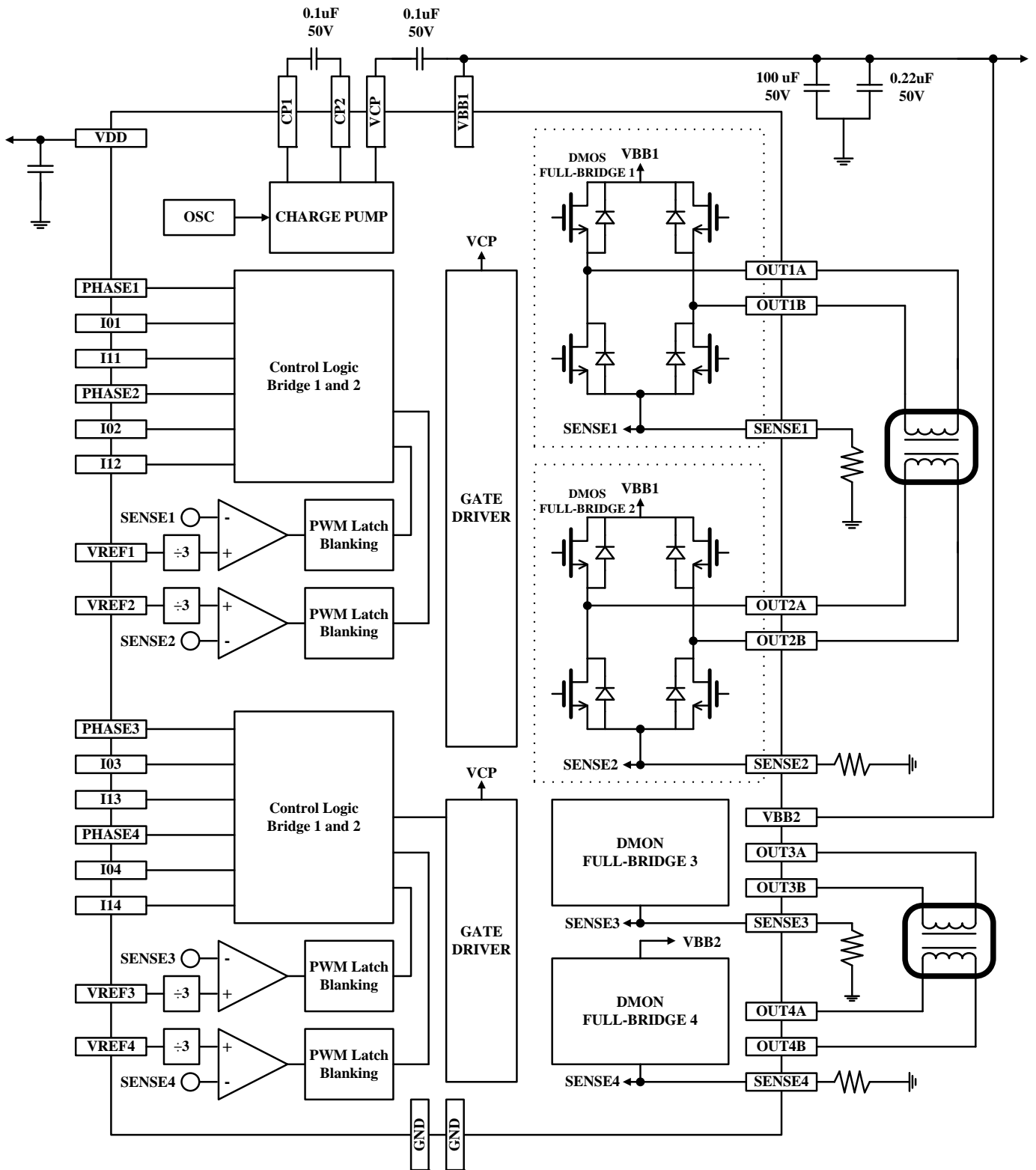
APPLICATION

- Robotics
- Security monitoring, high-speed ball
- Engraving machine, laser cutting machine
- Scanner, copier

BLOCK DIAGRAM



APPLICATION CIRCUIT



PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.	
			QFN36	ELQFP48
OUT1A	O	DMOS Full-Bridge 1 Output A	2	3
SENSE1	O	Sense Resistor Terminal for Bridge 1	3	4
OUT1B	O	DMOS Full-Bridge 1 Output B	4	5
VBB1	Power	Load Supply Voltage	5	6
OUT2B	O	DMOS Full-Bridge 2 Output B	6	8
SENSE2	O	Sense Resistor Terminal for Bridge 2	7	9
OUT2A	O	DMOS Full-Bridge 2 Output A	8	10
PHASE4	I	Control input	9	13
PHASE3	I	Control input	10	14
VDD	Power	Logic Supply Voltage	11	15
VREF1	I	Analog Input	12	16
VREF2	I	Analog Input	13	17
VREF3	I	Analog Input	14	18
VREF4	I	Analog Input	15	19
GND	Power	Ground	16	20
PHASE2	I	Control input	17	21
PHASE1	I	Control input	18	22
I14	I	Control input	19	24
OUT4A	O	DMOS Full-Bridge 4 Output A	20	27
SENSE4	O	Sense Resistor Terminal for Bridge 4	21	28
OUT4B	O	DMOS Full-Bridge 4 Output B	22	29
VBB2	Power	Load Supply Voltage	23	31
OUT3B	O	DMOS Full-Bridge 3 Output A	24	32
SENSE3	O	Sense Resistor Terminal for Bridge 3	25	33
OUT3A	O	DMOS Full-Bridge 3 Output B	26	34
I13	I	Control input	27	37
I12	I	Control input	28	38
I11	I	Control input	29	39
GND	Power	Ground	30	40
VCP	O	Reservoir Capacitor Terminal	31	42
CP1	O	Charge Pump Capacitor Terminal	32	43
CP2	O	Charge Pump Capacitor Terminal	33	44
I01	I	Control input	34	45
I02	I	Control input	35	46
I03	I	Control input	36	47
I04	I	Control input	1	48
NC	-	NC pin	-	1, 2, 7, 11, 12, 23, 25, 26, 30, 35, 36, 41
-	-	Exposed pad for enhanced thermal performance. Should be soldered to the PCB.	-	-

FUNCTION DESCRIPTION

DEVICE OPERATION

The PT2475 is designed to operate two stepper motors, four DC motors, or one stepper and two DC motors. The currents in each of the output full-bridges, all N-channel DMOS, are regulated with fixed off-time pulse width modulated (PWM) control circuitry. Each full-bridge peak current is set by the value of an external current sense resistor, R_{Sx} , and a reference voltage, V_{REFx} .

If the logic inputs are pulled up to VDD, it is good practice to use a high value pull-up resistor in order to limit current to the logic inputs, should an overvoltage event occur. Logic inputs include: PHASEx, I0x, and I1x.

INTERNAL PWM CURRENT CONTROL

Each full-bridge is controlled by a fixed off-time PWM current control circuit that limits the load current to a desired value, I_{TRIP} . Initially, a diagonal pair of source and sink DMOS outputs are enabled and current flows through the motor winding and R_{Sx} . When the voltage across the current sense resistor equals the voltage on the V_{REFx} pin, the current sense comparator resets the PWM latch, which turns off the source driver. In normal operation, PHASEx are signals of step by step, the maximum value of current limiting is set by the selection of R_{Sx} and the voltage at the VREF input with a trans-conductance function approximated by:

$$I_{TripMax} = V_{REF} / (3 \times R_S)$$

Each current step is a percentage of the maximum current, $I_{TripMax}$. The actual current at each step I_{Trip} is approximated by:

$$I_{Trip} = (\% I_{TripMax} / 100) I_{TripMax}$$

where % $I_{TripMax}$ is given in the Step Sequencing table.

Note: It is critical to ensure that the maximum rating of $\pm 500\text{mV}$ on each SENSEx pin is not exceeded.

FIXED OFF-TIME

The internal PWM current control circuitry uses a one shot circuit to control the time the drivers remain off. The one shot off-time, t_{off} , is internally set to $8\mu\text{s}$.

BLANKING

This function blanks the output of the current sense comparator when the outputs are switched by the internal current control circuitry. The comparator output is blanked to prevent false detections of overcurrent conditions, due to reverse recovery currents of the clamp diodes, or to switching transients related to the capacitance of the load. The stepper blank time, t_{BLANK} , is approximately $3\mu\text{s}$.

CONTROL LOGIC

Communication is implemented via the industry standard I0x, I1x, and PHASEx interface. This communication logic allows for full, half, and quarter step modes. Each bridge also has an independent VREF input so higher resolution step modes can be programmed by dynamically changing the voltage on the V_{REFx} pins.

CHARGE PUMP (CP1 AND CP2)

The charge pump is used to generate a gate supply greater than the VBB in order to drive the source-side DMOS gates. A $0.1\mu\text{F}$ ceramic capacitor should be connected between CP1 and CP2 for pumping purposes. A $0.1\mu\text{F}$ ceramic capacitor is required between VCP and VBBx to act as a reservoir to operate the high-side DMOS devices.

SHUTDOWN

In the event of a fault (excessive junction temperature, or low voltage on VCP), the outputs of the device are disabled until the fault condition is removed. At power-up, the under voltage lockout (UVLO) circuit disables the drivers.

SYNCHRONOUS RECTIFICATION

When a PWM-off cycle is triggered by an internal fixed off-time cycle, load current will recirculate. The PT2475 synchronous rectification feature will turn on the appropriate MOSFETs during the current decay, and effectively short out the body diodes with the low $R_{DS(on)}$ driver. This significantly lowers power dissipation. When a zero current level is detected, synchronous rectification is turned off to prevent reversal of the load current.

MIXED DECAY OPERATION

The bridges operate in mixed decay mode. Referring to figure 1, as the trip point is reached, the device goes into fast decay mode for 30.1% of the fixed off-time period. After this fast decay portion, t_{FD} , the device switches to slow decay mode for the remainder of the off-time. During transitions from fast decay to slow decay, the drivers are forced off for approximately 400ns. This feature is added to prevent shoot-through in the bridge. As shown in figure 1, during this "dead time" portion, synchronous rectification is not active, and the device operates in fast decay and slow decay only.

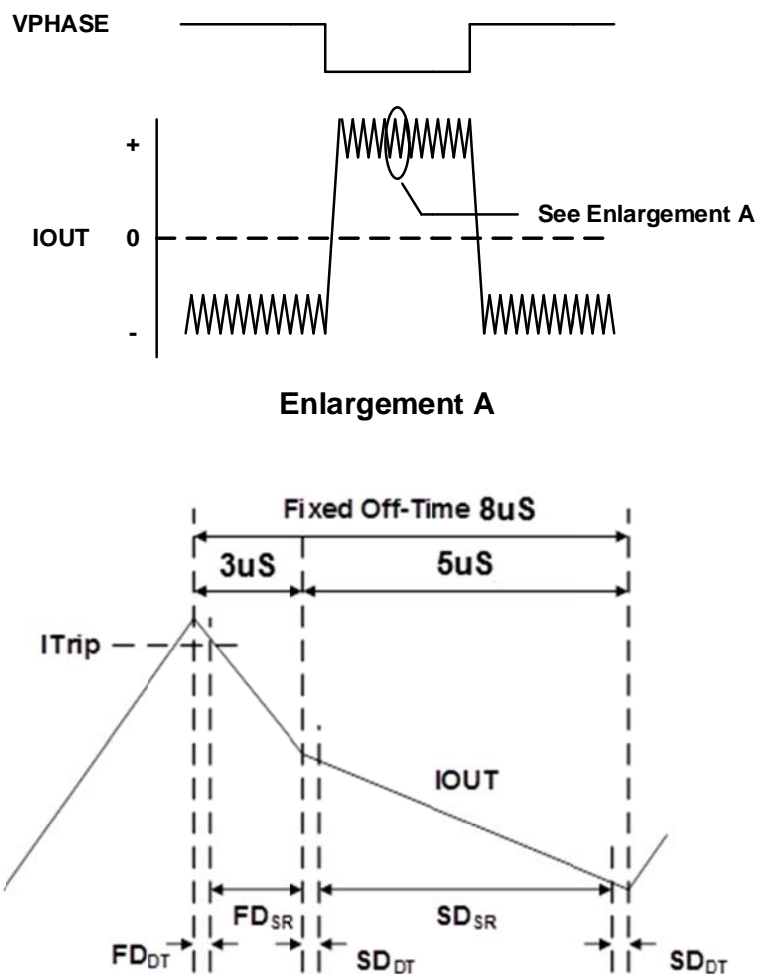
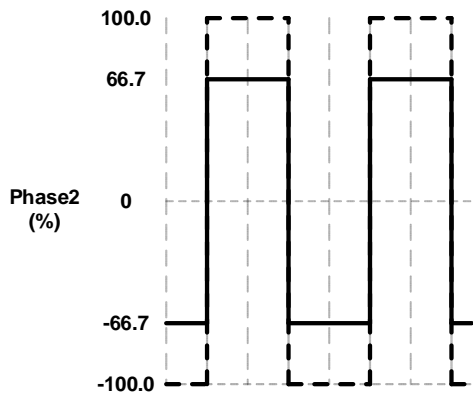
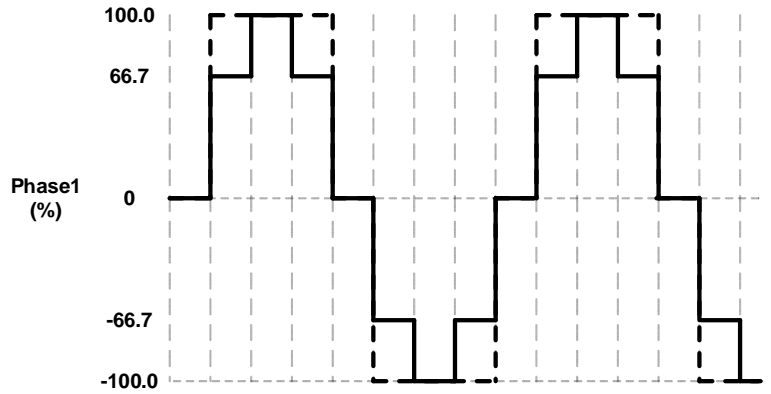
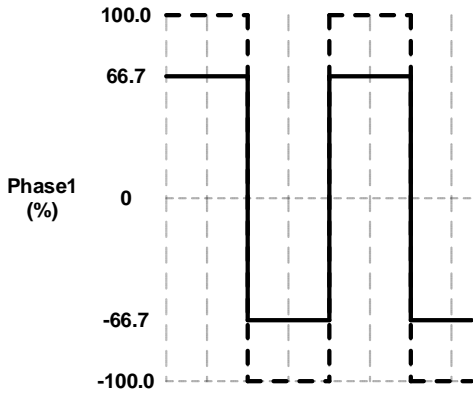
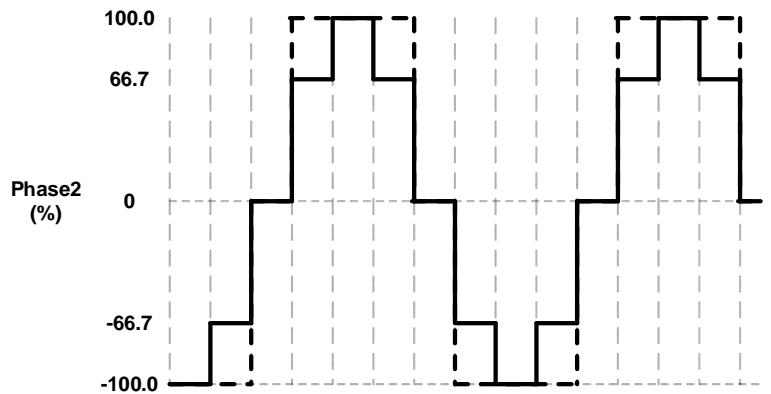


Figure 1. Mixed Decay Mode Operation

STEP SEQUENCING DIAGRAM



- - - Full step 2 phase
 — Modified step 2 phase



- - - Full step 2 phase
 — Modified step 2 phase

Figure 2: Step Sequencing for Full-Step Increments

Figure 3: Step Sequencing for Half-Step Increments

STEP SEQUENCING DIAGRAM

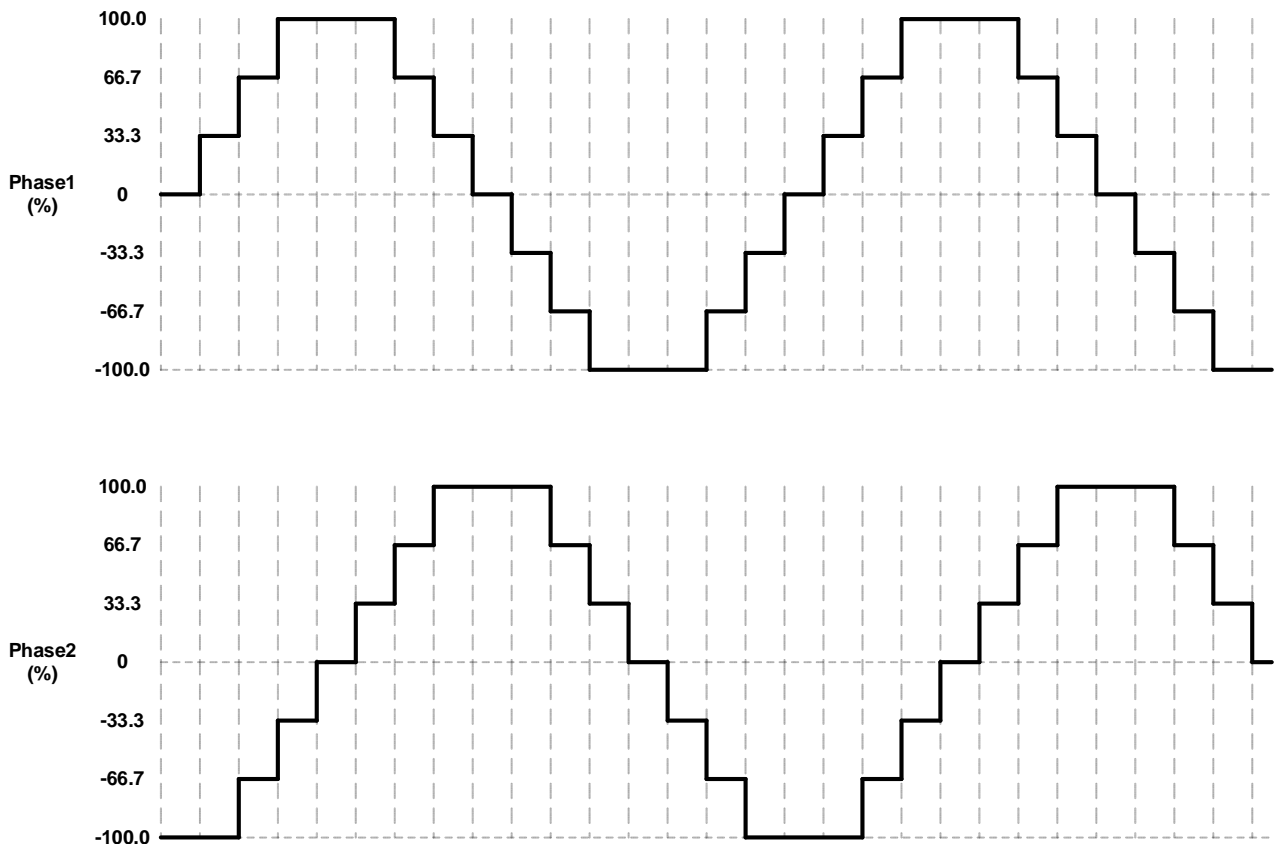


Figure 4: Step Sequencing for Quarter-Step Increments.

Table 1: Step Sequencing Setting

Full	1/2	1/4	Phase 1 (%I _{TripMax})	I0x	I1x	PHASE	Phase 2 (%I _{TripMax})	I0x	I1x	PHASE
	1	1	0	H	H	X	100	L	L	0
		2	33	L	H	1	100	L	L	0
1	2	3	100/66*	L/H*	L	1	100/66*	L/H*	L	0
		4	100	L	L	1	33	L	H	0
	3	5	100	L	L	1	0	H	H	X
		6	100	L	L	1	33	L	H	1
2	4	7	100/66*	L/H*	L	1	100/66*	L/H*	L	1
		8	33	L	H	1	100	L	L	1
	5	9	0	H	H	X	100	L	L	1
		10	33	L	H	0	100	L	L	1
3	6	11	100/66*	L/H*	L	0	100/66*	L/H*	L	1
		12	100	L	L	0	33	L	H	1
	7	13	100	L	L	0	0	H	H	X
		14	100	L	L	0	33	L	H	0
4	8	15	100/66*	L/H*	L	0	100/66*	L/H*	L	0
		16	33	L	H	0	100	L	L	0

*Denotes modified step mode

APPLICATION INFORMATION

MOTOR CONFIGURATIONS

PT2475 is for applications that require either two stepper motor drivers or four DC motor drivers. Commutation is done with a standard phase/enable logic interface.

DC MOTOR CONTROL

Each of the 4 full bridges has independent PWM current control circuitry that makes the PT2475 capable of driving up to four DC motors at currents up to 1.2A. Control of the DC motors is accomplished by tying the I0x and I1x pins together creating an equivalent ENABLE function with maximum current defined by the voltage on the corresponding V_{REFx} pin. The DC motors can be driven via a PWM signal on this enable signal, or on the corresponding PHASEx pin. Motor control includes forward, reverse, and coast.

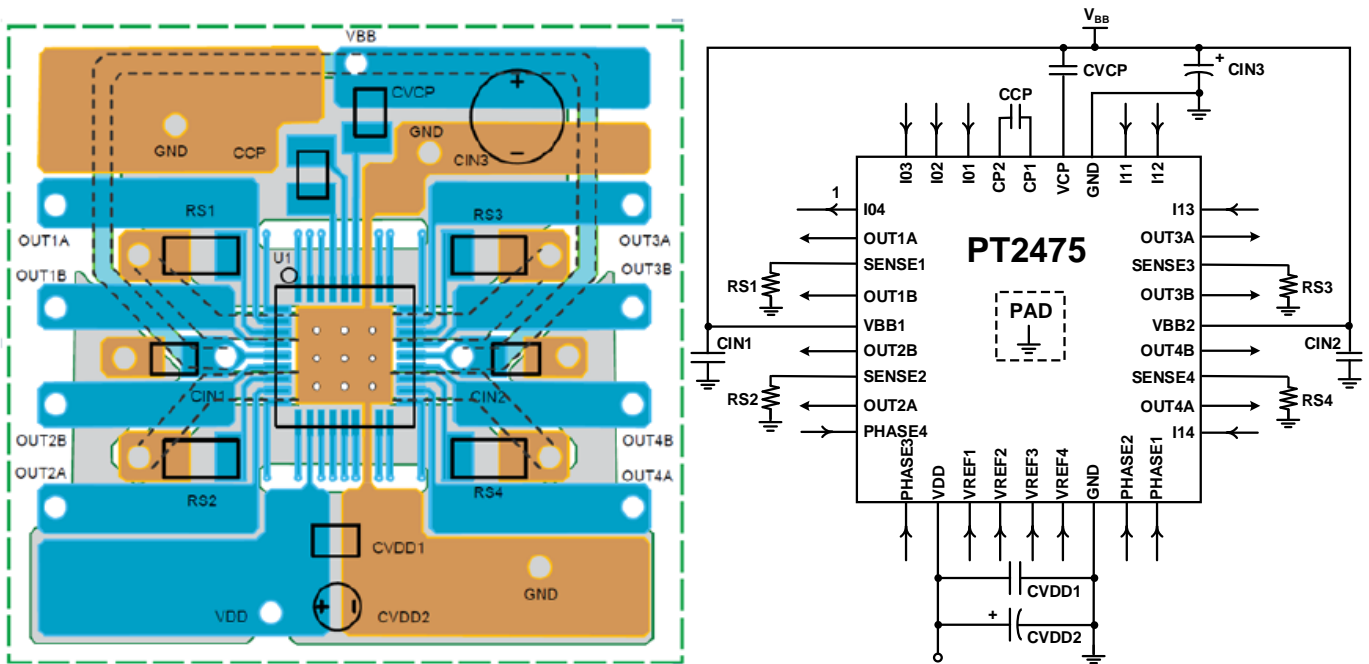
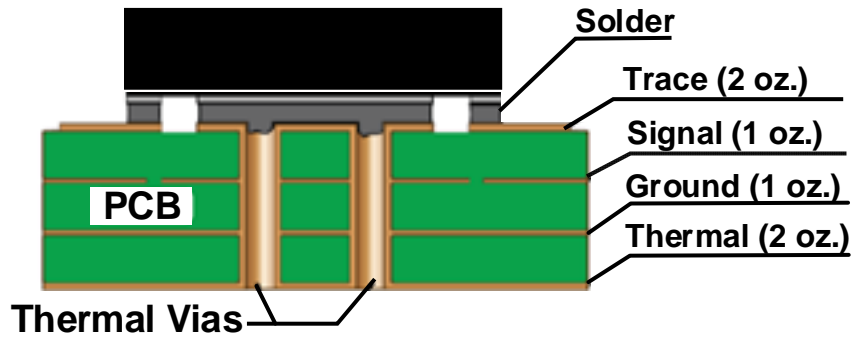
LAYOUT

The printed circuit board should use a heavy ground-plane. For optimum electrical and thermal performance, the PT2475 must be soldered directly onto the board. On the underside of the PT2475 package is an exposed pad, which provides a path for enhanced thermal dissipation. The thermal pad should be soldered directly to an exposed surface on the PCB. Thermal vias are used to transfer heat to other layers of the PCB.

GROUNDING

In order to minimize the effects of ground bounce and offset issues, it is important to have a low impedance single-point ground, known as a star ground, located very close to the device. By making the connection between the exposed thermal pad and the ground-plane directly under the PT2475, that area becomes an ideal location for a star ground point.

A low impedance ground will prevent ground bounce during high current operation and ensure that the supply voltage remains stable at the input terminal. The recommended PCB layout shown in the diagram below, illustrates how to create a star ground under the device, to serve both as low impedance ground point and thermal path.



QFN36 package layout shown

SENSE PINS

The sense resistors, R_{Sx} , should have a very low impedance path to ground, because they must carry a large current while supporting very accurate voltage measurements by the current sense comparators. Long ground traces will cause additional voltage drops, adversely affecting the ability of the comparators to accurately measure the current in the windings. As shown in the layout below, the SENSE x pins have very short traces to the R_{Sx} resistors and very thick, low impedance traces directly to the star ground underneath the device. If possible, there should be no other components on the sense circuits.

Note: When selecting a value for the sense resistors, be sure not to exceed the maximum voltage on the SENSE x pins of $\pm 500\text{mV}$.

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Max	Unit	
Motor power supply voltage		VBB	-0.3	38	V	
Logic power supply voltage		VCC	-0.3	5.5	V	
Operating Junction Temperature		T _j	-40	150	°C	
SENSEx Pin Voltage		VSENSE	-0.3	0.5	V	
VREFx Pin Voltage		VREFX	-0.3	2.5	V	
Storage Temperature		T _{STG}	-40	150	°C	
Operation Humidity		-	20	85	%	
Storage Humidity		-	20	90	%	
ESD	-	HBM	-	±4	-	KV
		MM	-	±0.4	-	KV
		CDM*	-	±0.5	-	KV

*CDM test is based on ANSI/ESDA/JEDEC JS-002-2014

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Min	Max	Unit
Motor power supply voltage		VBB	8	36	V
Logic power supply voltage		VCC	3	5	V
Motor continuous current		I _{OUT}	0	1.2	A
Motor peak current (t < 1μs)		I _{PEAK}	Internal Limited		A
Logic level input voltage		V _{LOGIC}	0	5	V
Operating ambient temperature		T _A	-40	85	°C

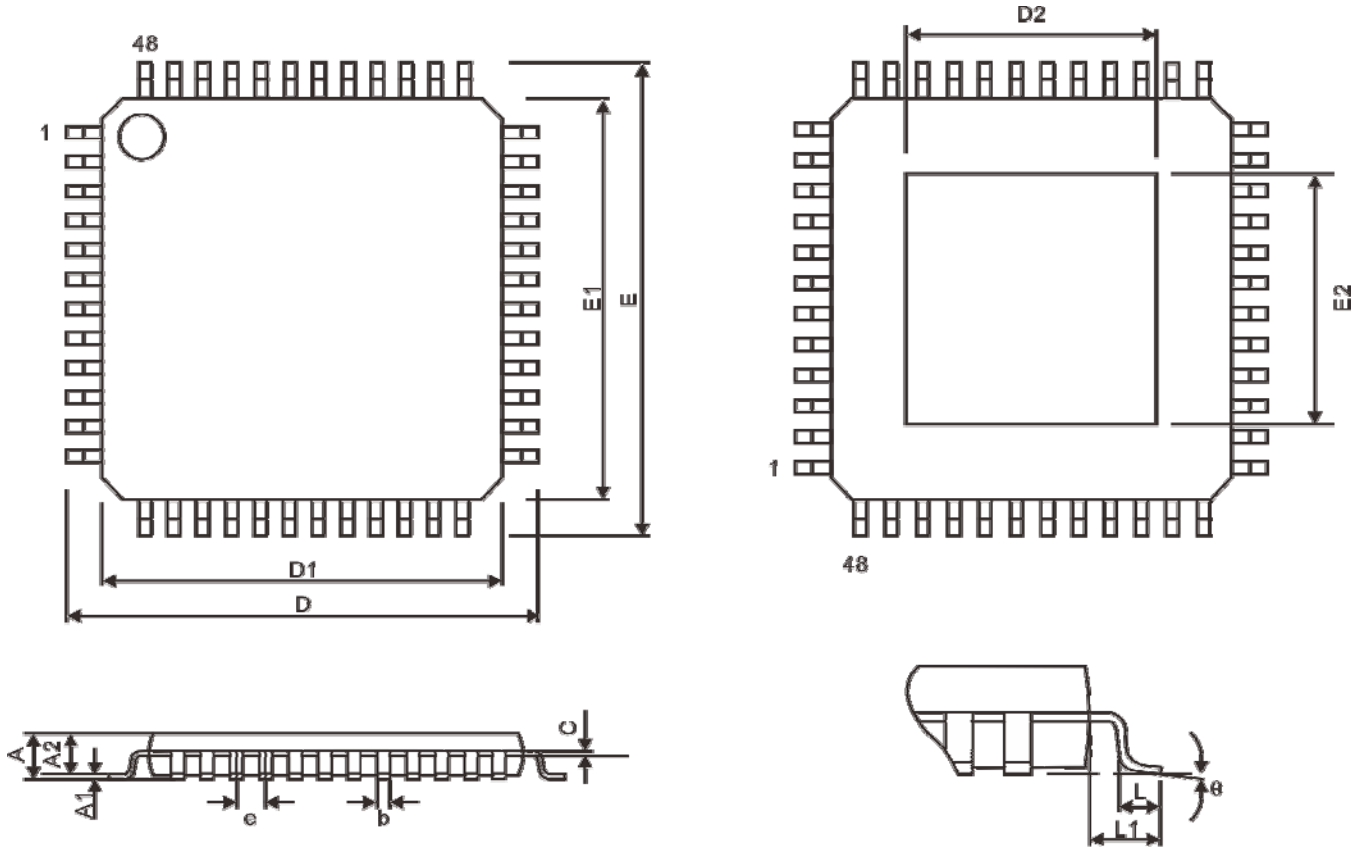
ELECTRICAL CHARACTERISTICS

TA=25°C , VBB=36V , over recommended operating conditions unless otherwise noted

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Motor Supply Voltage	VBB		8	-	36	V
Logic Supply Voltage	VDD		3	-	5	V
VBB Supply Current	IBB		-	5	8	mA
VDD Supply Current	IDD		-	-	10	mA
Output Resistance	RDS(ON)	Source Driver, IO _{UT} =-1.2A, T _J =25°C	-	700	800	mΩ
		Sink Driver, IO _{UT} =1.2A, T _J =25°C	-	700	800	mΩ
Off-state leakage current	IOFF		-20	-	20	μA
Control Logic						
Input High Voltage	VIH		2.5	-	-	V
Input Low Voltage	VIL		-	-	1	V
Input Hysteresis	VHYS		-	1	-	V
Input Current	IIN	Input High = 5V	-	50	-	μA
Motor Driver						
Rise Time	tR		-	170	-	ns
Fall Time	tF		-	80	-	ns
Dead Time	tDEAD		-	700	-	ns
Blanking Time	TBLANK		-	3	-	μs
Current Control						
VREFx Pin Input Range	VREFx		0	-	1.5	V
VREFx Pin Input Current	IREF	VREF=1.5V	-1	-	1	μA
Current Trip-Level Error	VERR	VREF=1.5V, Phase Current=100%	-5	-	5	%
		VREF=1.5V, Phase Current=67%	-5	-	5	%
		VREF=1.5V, Phase Current=33%	-15	-	15	%
Protection Circuit						
VBB UVLO Threshold	VUV(VBB)	VBB Rising	7	-	-	V
VBB Hysteresis	VHYS(VBB)		-	300	-	mV
VDD UVLO Threshold	VUV(VDD)	VDD Rising	2.65	-	-	V
VDD Hysteresis	VHYS(VDD)		-	200	-	mV
Thermal Shutdown Temp	TSD		-	160	-	°C
Thermal Shutdown Hys	TSD,HYS		-	60	-	°C

PACKAGE INFORMATION

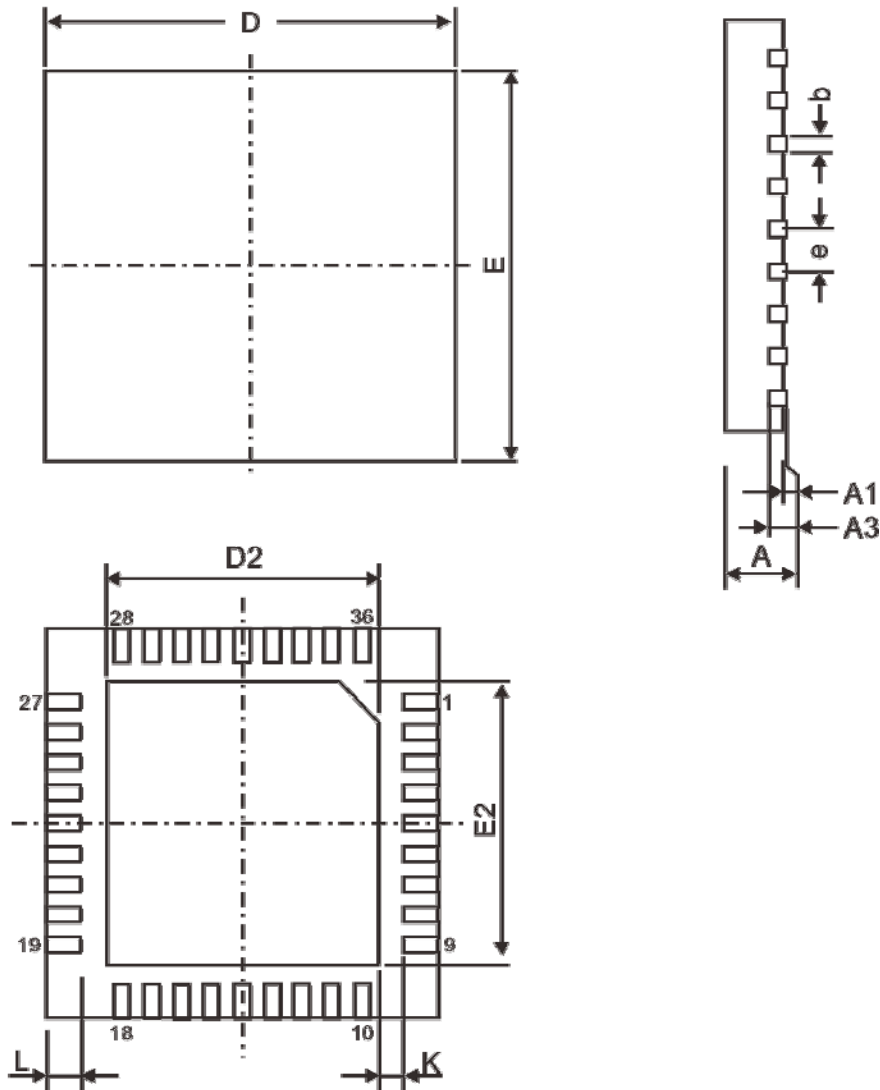
48-PIN, ELQFP, 7X7



Symbol	Dimensions(mm)		
	Min.	Nom.	Max.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	-	0.20
D	9.00 BSC		
D1	7.00 BSC		
D2	4.31	-	5.21
E	9.00 BSC		
E1	7.00 BSC		
E2	4.31	-	5.21
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

Note: Refer to JEDEC MS-026 BBC

36-PIN, QFN, 6X6



Symbol	Dimensions(mm)		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20 REF		
b	0.18	0.25	0.30
D	6.00 BSC		
D2	4.47	4.57	4.62
E	6.00 BSC		
E2	4.47	4.57	4.62
e	0.50 BSC.		
L	0.35	0.40	0.45
K	0.2	-	-

Note: Refer to JEDEC MO-220 VJJD

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