

DESCRIPTION

The PT2483L is a monolithic integrated motor driver designed for printer, scanner or home appliance. The built-in two channel H-bridges designs for driving a bipolar stepping motor or two DC-brushed motors. The H-bridge driver is consists by all of N-channel MOSFET allows delivering up to 2.5A maximum output current ($V_M=24\text{ V}$, $T_a=25^\circ\text{C}$).

The Phase/Enable input interface is a common configuration for the motor driver; it is very versatile to control the H-bridge switches to determinate motor winding current and phase. The motor current decay mode is programmable by a tri-states input pin.

The PT2483L is available in a 28-pin HTSSOP package with thermal pad

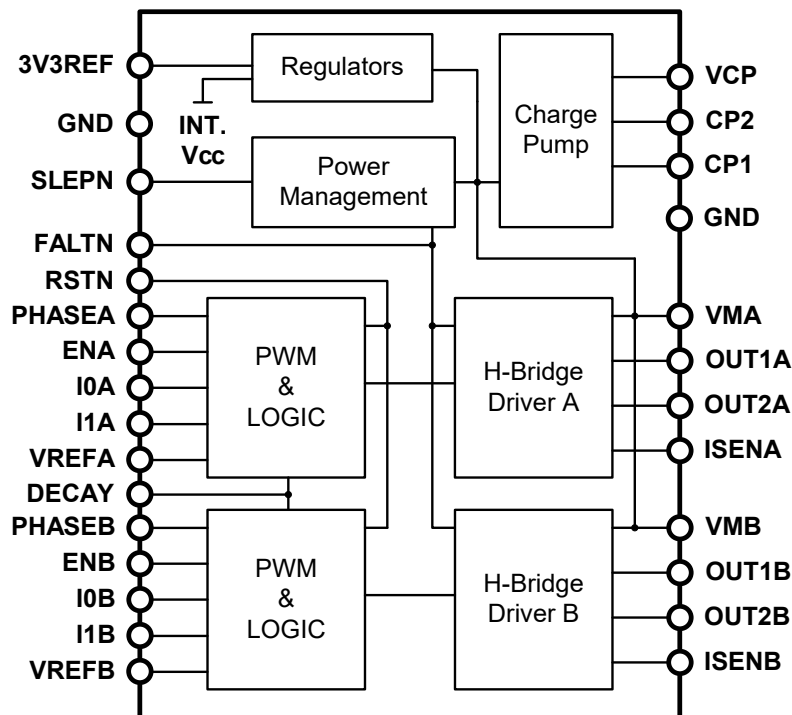
APPLICATIONS

- Automatic teller machines
- Video security cameras
- Printers
- Scanners
- Office automation machines
- Amusement machines
- Factory automation
- Robotics

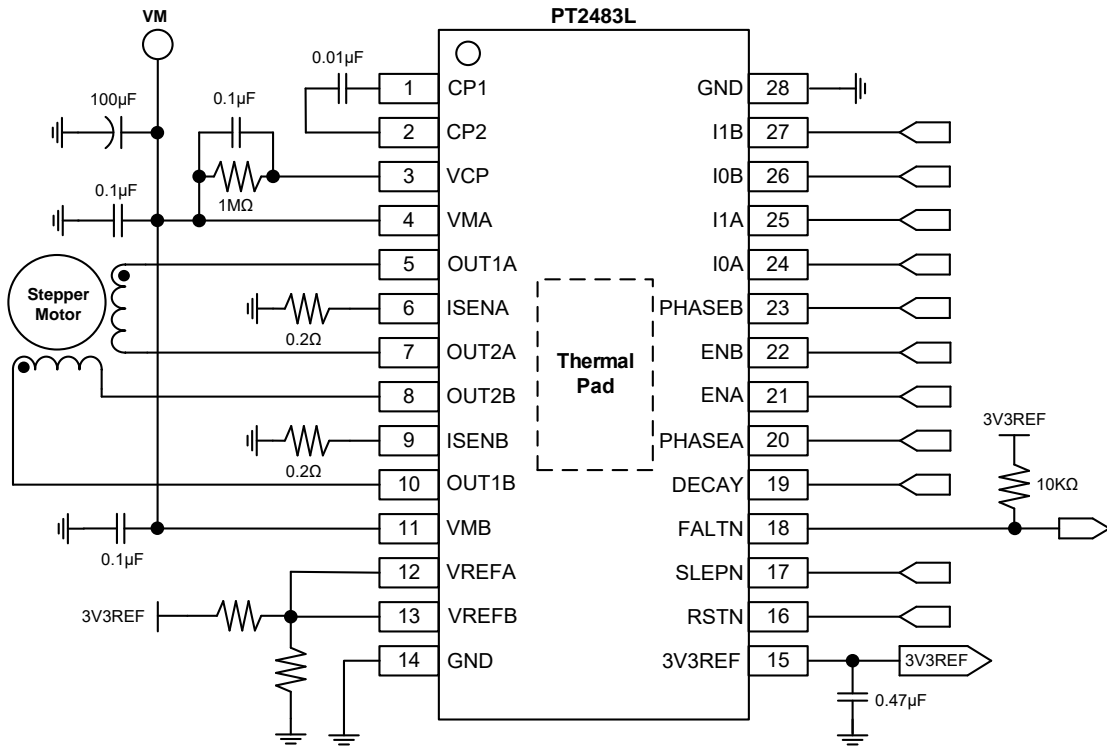
FEATURES

- 8V to 36V maximum supply voltage
- 2.5A maximum driving current at $V_M=24\text{V}$ (with additional heatsink)
- Low switches conduction resistance: $0.4\Omega(\text{typ})$, high side + low side in $T_j=25^\circ\text{C}$.
- Phase and Enable control interface
- H-bridge driver outputs with four levels PWM constant current regulation.
- Winding current decay modes
 - mixed decay
 - slow decay
 - fast decay
- Drives single bipolar stepping motor or dual brushed dc Motors
- Built-in 3.3V reference voltage output
- Low-power sleep mode
- Protection features
 - Over current protection (OCP)
 - Thermal shutdown (TSD)
 - VM under voltage lock out (UVLO)
 - Fault indication output (FALTN)

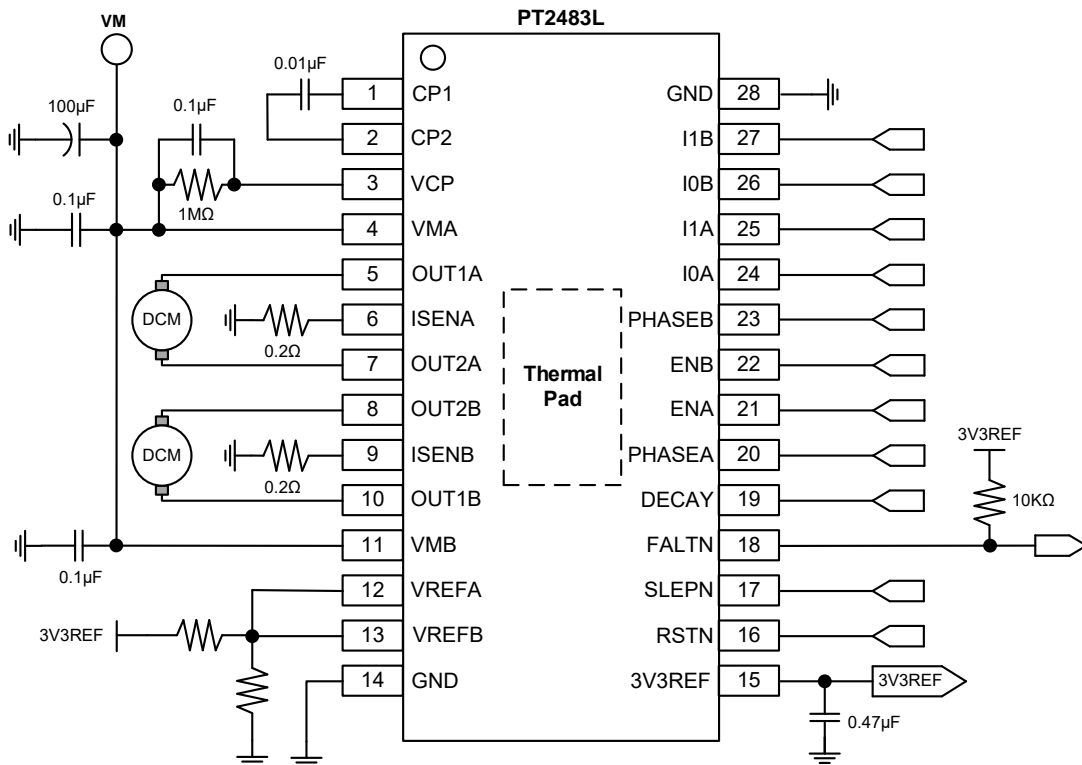
BLOCK DIAGRAM



APPLICATION CIRCUIT



Drives a bipolar stepping motor



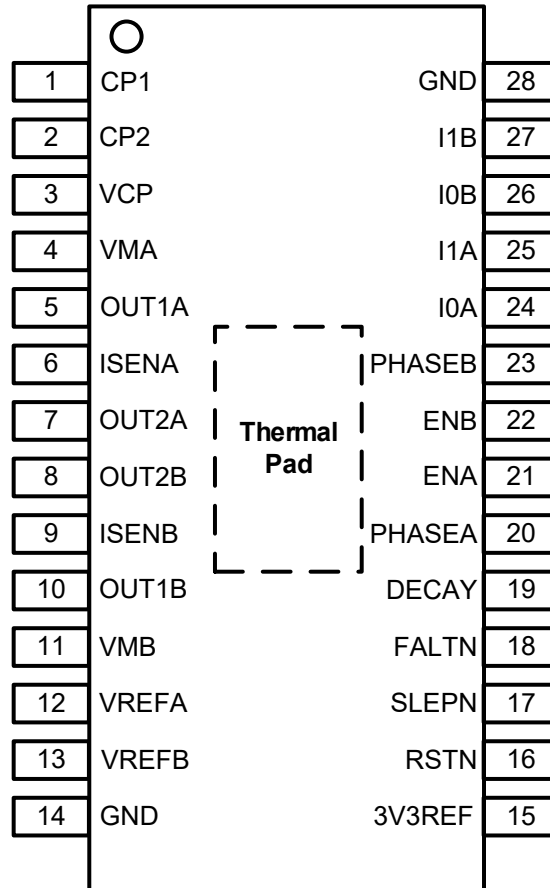
Drives two brushed dc motor

ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT2483L-HT	28 Pins, HTSSOP	PT2483L-HT

PIN CONFIGURATION

Top View



PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
CP1	I	External flying capacitor for charge pump, Connect a 0.01 μ F/50V low-ESR ceramic capacitor between CP1 and CP2.	1
CP2	I		2
VCP	O	High-side gate drive supply voltage (Connect a 0.1 μ F/50V ceramic capacitor and a 1M Ω resistor to VM.)	3
VMA	-	H-Bridge A power supply	4
OUTA1	O	H-Bridge A output 1	5
ISENA	I	H-Bridge A current sense / GND	6
OUTA2	O	H-Bridge A output 2	7
OUTB2	O	H-Bridge B output 2	8
ISENB	I	H-Bridge B current sense / GND	9
OUTB1	O	H-Bridge B output 1	10
VMB	-	H-Bridge B power supply	11
VREFA	I	H-Bridge A current set reference input	12
VREFB	I	H-Bridge B current set reference input	13
GND	-	Device ground	14
3V3REF	O	3.3V reference voltage output	15
RSTN	I	Reset input (L=Initialize all of internal logic registers and disables H-bridge outputs)	16
SLEPN	I	Sleep mode input (H=device enable, L=low-power sleep mode)	17
FALTN	O	Fault, Logic low when fault condition appear (OCP, OTP)	18
DECAY	I	Decay mode (Low = slow decay, open = mixed decay, high = fast decay)	19
PHASEA	I	H-Bridge A phase (H=AOUT1 high, AOUT2 low)	20
ENA	I	H-Bridge A enable (H=H-bridge A output active)	21
ENB	I	H-Bridge B enable (H=H-bridge B output active)	22
PHASEB	I	H-Bridge B phase (H=BOUT1 high, BOUT2 low)	23
I0A	I	H-Bridge A current set (Sets H-bridge A current: 00 = 100%, 01 = 71%, 10 = 38%, 11 = 0%)	24
I1A	I		25
I0B	I	H-Bridge B current set (Sets H-bridge B current: 00 = 100%, 01 = 71%, 10 = 38%, 11 = 0%)	26
I1B	I		27
GND	-	Device ground	28
Thermal Pad	-	Enhance the package heat dissipation, must connecting to the GND plane through the thermal via.	-

FUNCTION DESCRIPTION

PWM MOTOR DRIVERS

The PT2483L includes two H-bridge drivers with PWM current regulation circuitry. The block diagram of system control circuitry shown on Figure 1, the EN/PH input interface is recommend for bipolar stepper motor, but drives two separate brushed dc motors also possible.

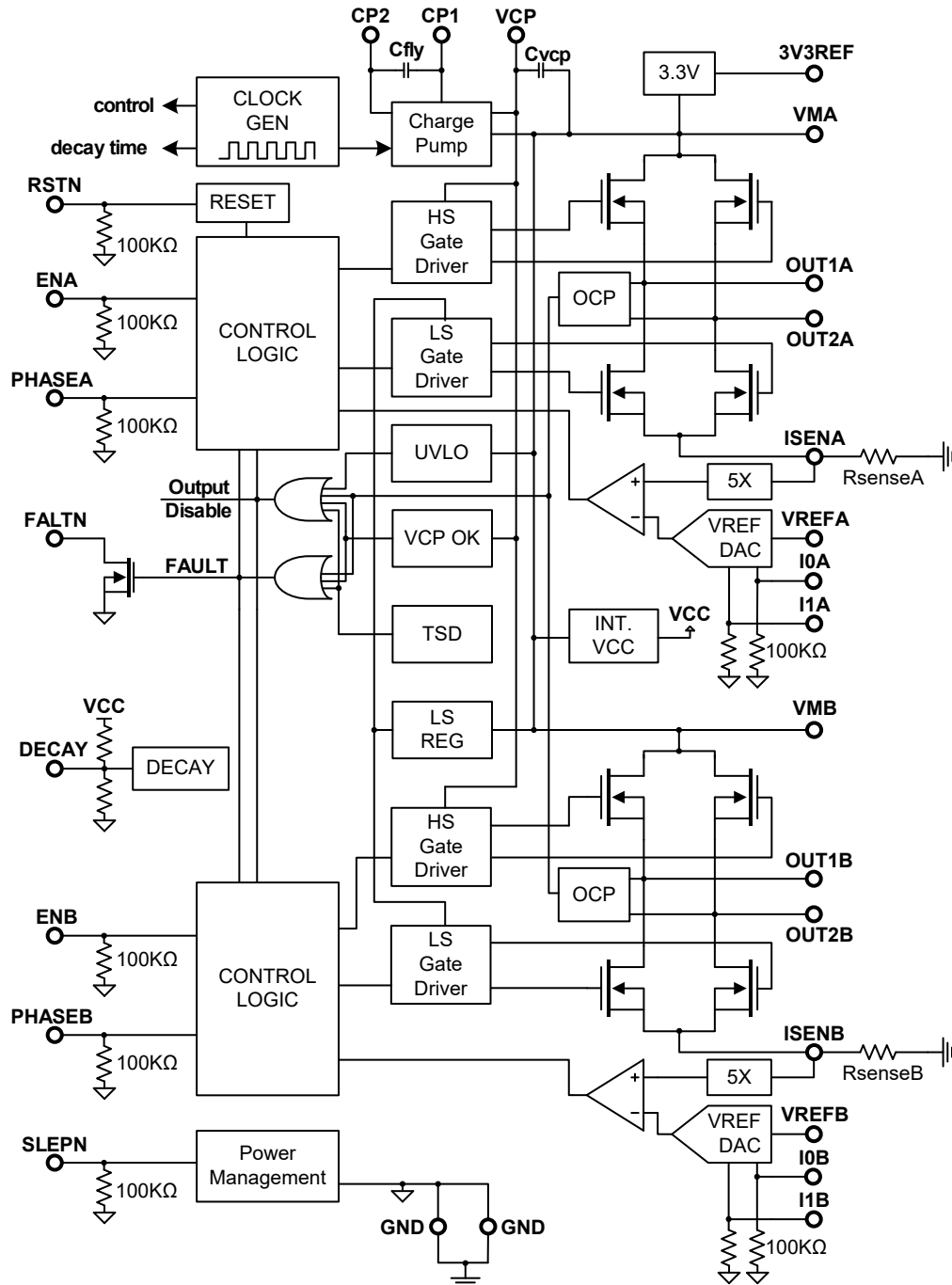


Figure 1. Motor Control Circuitry

The multiple motor power supply pins (VMA and VMB) must be tight together to single supply voltage node on PCB.

H-BRIDGE OUTPUT CONFIGURATION

The output current phase of the H-bridge driver is controls by PHASEx pins logic, and ENx pin is controls the H-bridge driver enable or not. Refer to the Table 1 for the I/O logic corresponds.

ENx	PHASEx	OUTx1	OUTx2
0	X	OPEN	OPEN
1	1	H	L
1	0	L	H

Table 1, H-Bridge Output Configuration

PWM CHOPPING CURRENT REGULATION

The motor windings current regulated by a fixed-frequency PWM chopping, when the H-bridge is enable, the winding current flows through the switches FET of H-bridge and direction determinate by PHASEx setting. The slew rate of winding current is depends on the VM voltage and inductance of the winding. Once the current reaches the current chopping threshold, the H-bridge FET will be disabled and decay mode setting will handles current decay behavior.

For a stepping motor, PWM current regulation often used to maintain the winging current level and helps motor torque steady, and chopping current divider can be use on micro-stepping motor. For DC motors, current regulation is use to limit the start-up and stall current of the motor.

A comparator is used to sets the chopping current level, first the voltage across an external current sense resistor connected to the ISENx pins will multiples by 5, and compare with VREFx voltage input. The VREFx input voltage is scale by a 2-bit DAC that allows current settings from 100%, 71%, 38% of full-scale, and down to zero.

Each H-bridge has own VREFx DAC setting inputs (I0x and I1x). The voltage applied to the PWM current comparator is derives from VREFx DAC output, and VREFx DAC output is scaling from VREFx input and divide ratio determinates by logic states of the I0x and I1x, in Table 2 shows bit definition. The H-bridge will be disabled flows when both I0x and I1x bits in logic Hi state.

I0x	I1x	VREFx DAC Current Ratio (% Full-Scale Chopping Current)
1	1	0% (H-bridge disabled)
0	1	38%
1	0	71%
0	0	100%

Table 2, PWM Chopping Current VS VREFx DAC Bit Definition

The PWM chopping current is calculate in Equation 1.

$$I_{CHOP} = \frac{V_{REFx} \times DAC \text{ ratio}}{5 \times R_{ISENSE}} \quad \text{Eq.(1)}$$

Example 1:

If a 0.5Ω sense resistor is used and the VREFx pin is 2.5 V, and VREFx ratio is sets to 100% of full scale chopping current level (I0x=H, I1x=H) , the output current will be :

$$(2.5 \text{ V} \times 100\%) / (5 \times 0.5 \Omega) = 1.0A.$$

Example 2:

If a 0.2Ω sense resistor is used and the VREFx pin is 1.5V, and VREFx ratio is sets to 38% of full scale chopping current level (I0x=L, I1x=H) , the output current will be :

$$(2.5 \text{ V} \times 38\%) / (5 \times 0.2 \Omega) = 0.95A.$$

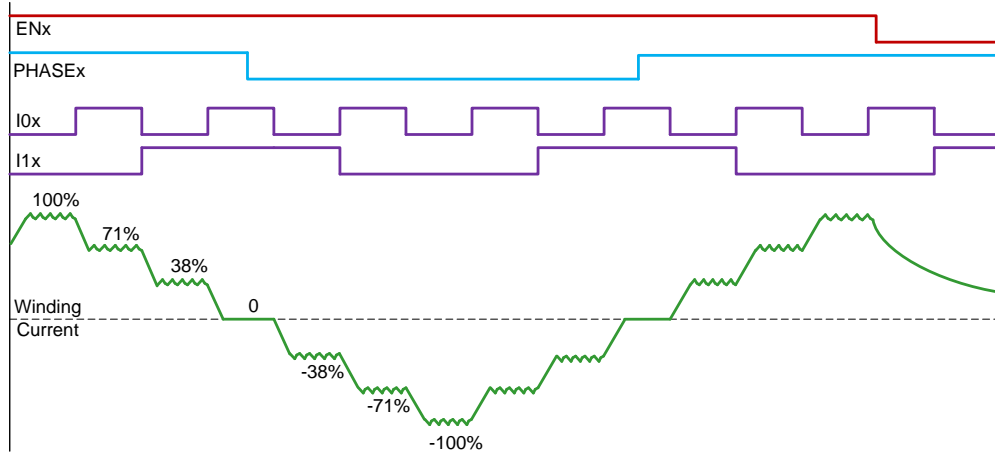


Figure 2, PWM Chopping Current with VREFx DAC Bit Setting

DECAY MODE

The motor winding current in PWM chopping cycle is determined by the voltage on the DECAY pin. In the charge period, the winding excitation by the H-bridge output current. And next the winding current flows through the current sense resistor on the ISENx pin presents a voltage drop and H-bridge will leave charge mode if it reaches the desired comparator threshold, and the next step of H-bridge will go to one of three modes: fast, slow, or mixed decay, depending on the DECAY pin logic status. Please refer to Table 3. The DECAY settings will apply to both H-bridges simultaneously, and Figure 3 shows the current direction in different decay modes and Figure 4 shows the mixed decay sequence waveform.

Decay Pin Level	DECAY Pin Logic	Decay Mode
<0.6V	L	Slow
OPEN	FLOAT	Mixed
>2V	H	Fast

Table 3. DECAY Mode Setting

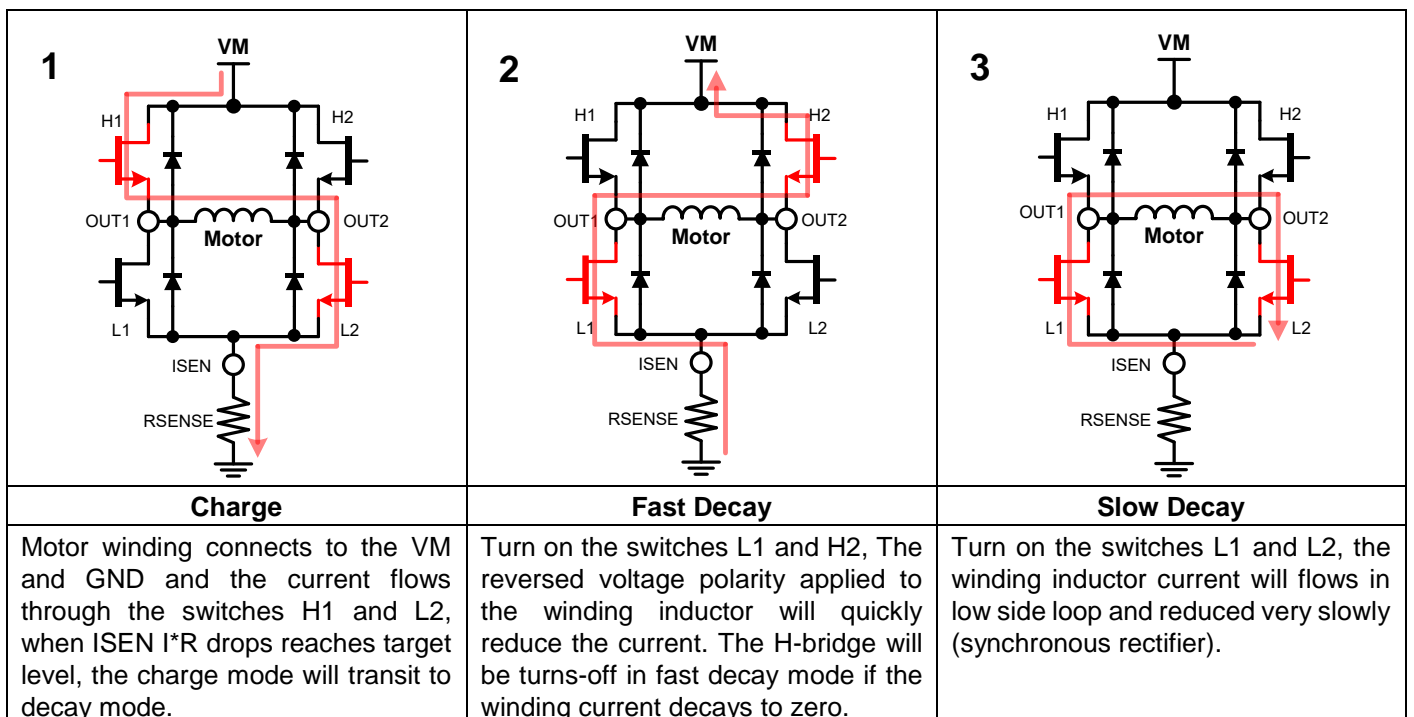
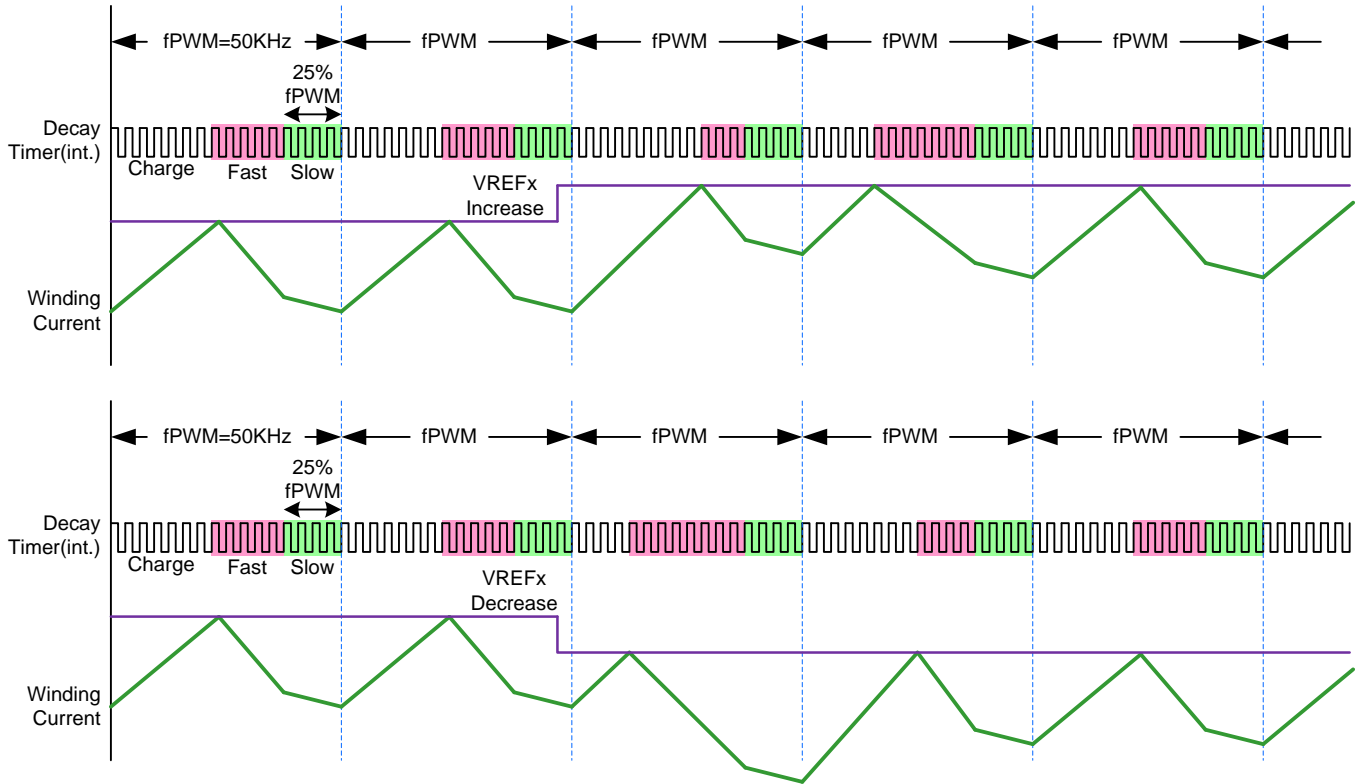


Figure 3. Mixed Decay Mode Switching Sequence (Forward mode only)



(Timer(int) is an internal clock management block uses to drives charge pump and PWM switching cycles, timing clock is only for realize mixed decay operation, not an exactly clock)

Figure 4, Mixed Decay Sequence Waveform

RESET and LOW POWER SLEEP MODE

Pull the RSTN pin to logic low state, the status of all control pins (except SLEPN) will be ignore and internal control circuit will be reset to initial state, the H-bridge output also disabled during RESTN in low state, in the meantime the 3.3V voltage reference and charge pump still works.

Pull the SLEPN pin to logic low will force the chip into a low power sleep mode. During sleep mode is active the H-bridges outputs are disabled, and analog circuit such like charge pump for HS gate driver, 3.3V voltage reference (3V3REF) and internal clocks generator is stop. In the sleep mode, all inputs logic states are ignore until SLEPN returns to logic high state. When chip is wakes up from the low power sleep mode, a short waiting time (less than 1ms) before H-bridge becomes to normal operation is required because of charge pump starting time.

BLANKING TIME

During PWM chopping current is flows after the H-bridge enable, the current signal can be picked-up in the sense resistor connected in ISENx pins, the signal will delivers to comparator after a fixed delay time to avoid noises or current spike causes fault-triggered. The blanking time is fixed at 4μs and it also sets a limit to the duty cycle of PWM in charge period, the minimum on-duty will not less than around 20% in a 50KHz PWM frequency.

PROTECTION CIRCUITS

The PT2483L have fully protection function to against miss-operation events.

OVERCURRENT PROTECTION (OCP)

Overcurrent detection circuit will always monitor all of output pins current during H-bridge is enable, this operation is independent from PWM chopping. If any output pin is connects to VM, GND or across load shorted, the inrush high current will be detected by OCP circuit and immediately turn off both H-bridge outputs after blanking time. The chip will remain disabled until either RSTN pin is toggle once or power down the VM supply and apply again.

If an output pin connects to the VM, the short circuit current will be passing through the low side MOSFET and current sense resistor to GND, to avoid sense resistance interference OCP detects, it should not be higher than a certain range, for example, 0.5Ω or less is recommend.

THERMAL SHUTDOWN (TSD)

If the chip temperature exceeds preset 160°C , all of MOSFET of H-bridge will be turn off and the FALTN pin will be pull down, an external pull up resistor may needed to detects FALTN logic state by MCU I/O pin. Once the chip temperature is cooling down to below hysteresis window, H-bridge outputs will enable again.

UNDERVOLTAGE LOCKOUT (UVLO)

In any time the VM pin voltage drops below the under voltage lockout threshold voltage, all circuitry of the chip will be disabled and reset the internal logic state, operation will resume when VM rises above the UVLO threshold.

FAULT INDICATION (FALTN)

Whatever which condition is happens, the OCP, TSD or charge pump voltage failed, the open-drain FALTN pin will pull down immediately and remains until RSTN pin re-toggled or VM voltage re-applied. FALTN could connect to MCU I/O port for error reporting with a pull high resistor to the 3V3REF or 5V logic supply.

POWER SUPPLY CAPACITOR RECOMMENDATIONS

Consider a real world application scenario; the motor driver is design to drives high inductance load such like motor winding or solenoid coil. If a H-bridge turns-off all of outputs during inductor current still flowing, because the inductor current would not be reset immediately, the rest of free-wheel current would re-directs and passing through the body diode of the output FET and runs into VM supply and final decay to zero after de-magnetization time. This reverse current depends on load inductance, inductor current and re-generates current from the motor due to inertia of rotor. In another case, the parasitic reactance (inductance + resistance) of power wire with the parasitic capacitance of PCB consists a LC resonates tank. During power supply sourcing current to the motor driver board, the VM voltage may drops quickly and parasitic LC resonate will trigged and starts oscillation if the local bypass capacitor is not sufficient.

To prevent unstable bounce or spike appears on VM bus, a high capacitance bounce absorber capacitor ($>100\mu\text{F}$) should be placed on VM bus line, it could absorb re-generates free-wheels current during DC motor brake and stabilize VM voltage during high forward/reverse motor current sources. A small MLCC $0.1\mu\text{F}$ bypass capacitor should be place near the motor driver IC power pin, VM and 3V3REF both, to reduce the spike causes by power line LC resonates.

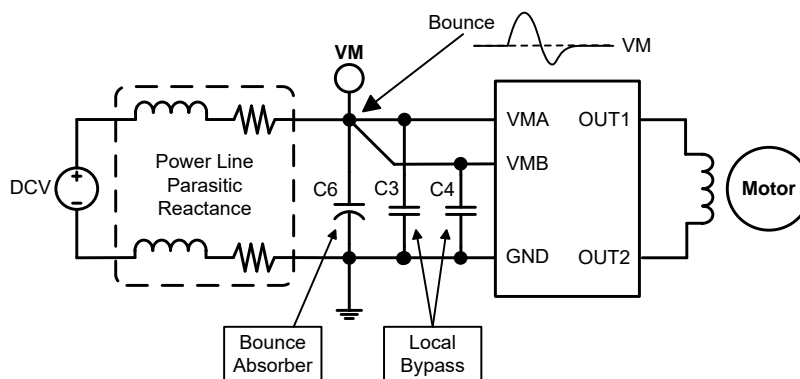


Figure 5, Motor Driver System with External Power Supply

PCB LAYOUT RECOMMENATION

The local bypass capacitor C3 and C4 should be place near the IC power pins, and bounce absorber capacitor C6 should be place on VM bus line. The GND plane should be place on the component side under the chip as a low impedance power trace, and larger area of GND plane and wider cooper trace reduce the thermal resistance (R_{JA}). The thermal pad under HTSSOP package must soldering to the PCB component side and connects to the bottom side through via holes, this arrangement can further enhance the heat dissipation.

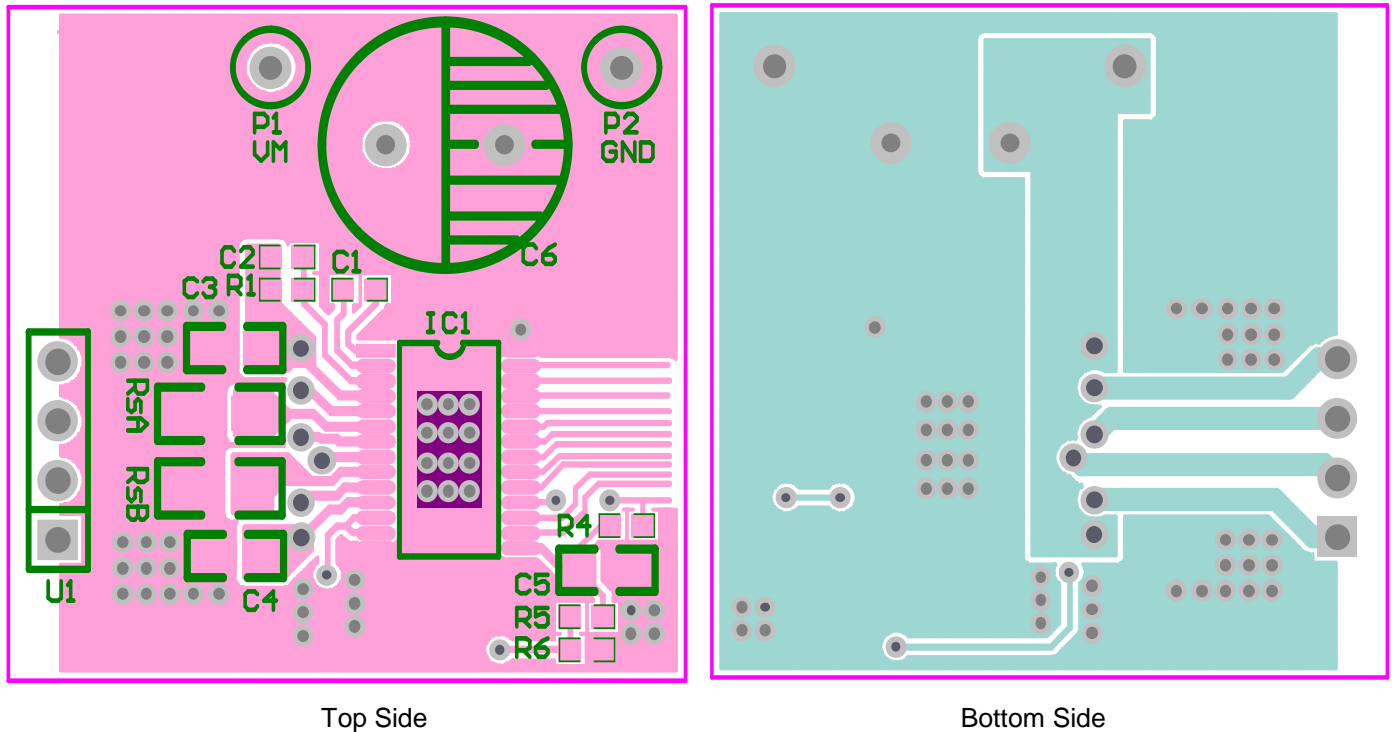


Figure 6, Simplified Layout Example (HTSSOP package)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min.	Max.	Unit
Supply voltage	VMx	-0.2	45	V
Logic pin voltage	ENx/PHASEx/I0x/I1x,DECAY, RESTN,SLEPN,FALTN	-0.2	6	V
VREF input voltage	VREFx	0	4	V
ISENx input voltage	VISENx	-0.6	+0.6	V
Peak motor output current, T<1μS	Ipk	Limited by internal circuit		A
Continue motor output current (note1)	Iout	0	2.5	A
Operating temperature	Topr	-40	85	°C
Storage temperature	Tstg	-40	150	°C
ESD, human body model	HBM	-2000	+2000	V
ESD, charge device model	CDM	+500	-500	V

PACKAGE THERMAL CHARACTERISTIC

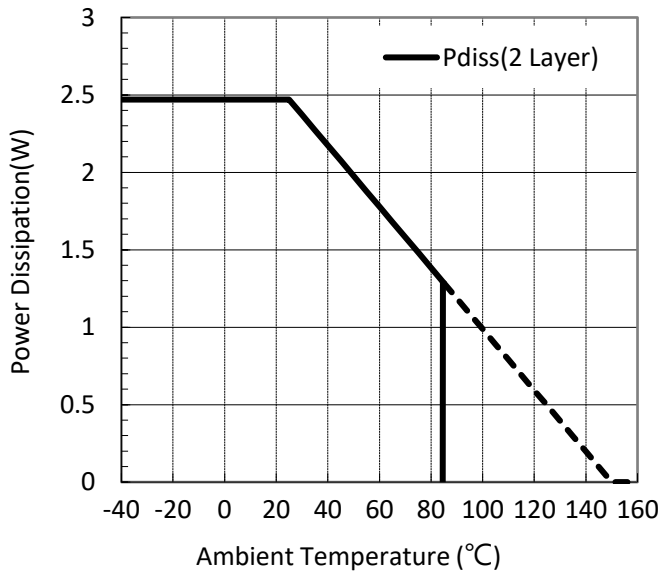
Parameter	Symbol	Condition	Typ	Unit
From chip conjunction dissipation to external environment (note2)	Rja	HTSSOP 28 Pin,	50.6	°C/W
From chip conjunction dissipation to PCB bottom side (note3)	Rjb		29.2	

Note 1: DC output current rating depends on PCB thermal dissipation capability and driving channels.

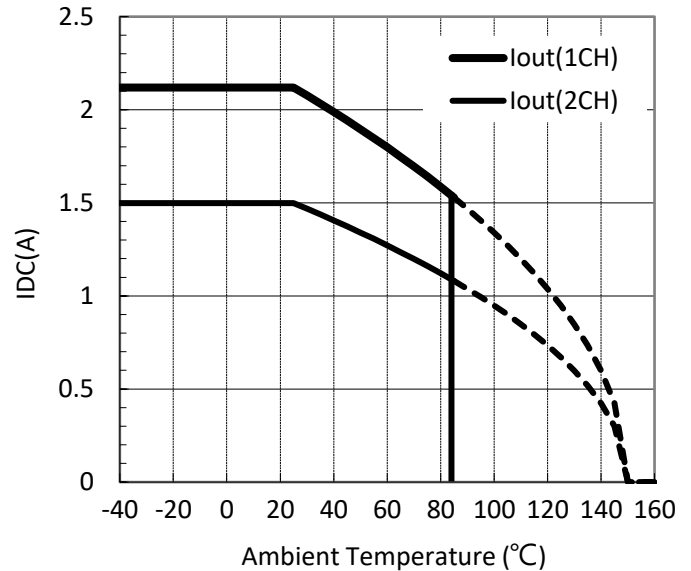
Note 2: The thermal resistance of HTSSOP 28 pin package measured on specified PCB: dimension=70mm x 55mm, FR-4, 2 layers, board thickness=1.6mm, copper thickness=1oz (35μm), GND plane metal coverage>65%, still airflow.

Note 3: The thermal via under the thermal pad: 12 pcs, diameter=0.4mm

PT2483L Thermal Derating



PT2483L DC Output Current



RECOMMENDED OPERATING CONDITION

Parameter	Symbol	Min	Typ	Max	Unit
VM supply voltage	V_M	8	24	36	V
VREF input voltage (note4)	V_{REF}	1	-	3.5	V
3V3REF load current	I_{3V3}	-	-	1	mA
External PWM clock frequency	F_{EXT}	0		100	KHz

Note 4: VREF less than 1V may degrade the Itrip tolerance.

ELECTRICAL CHARACTERISTIC

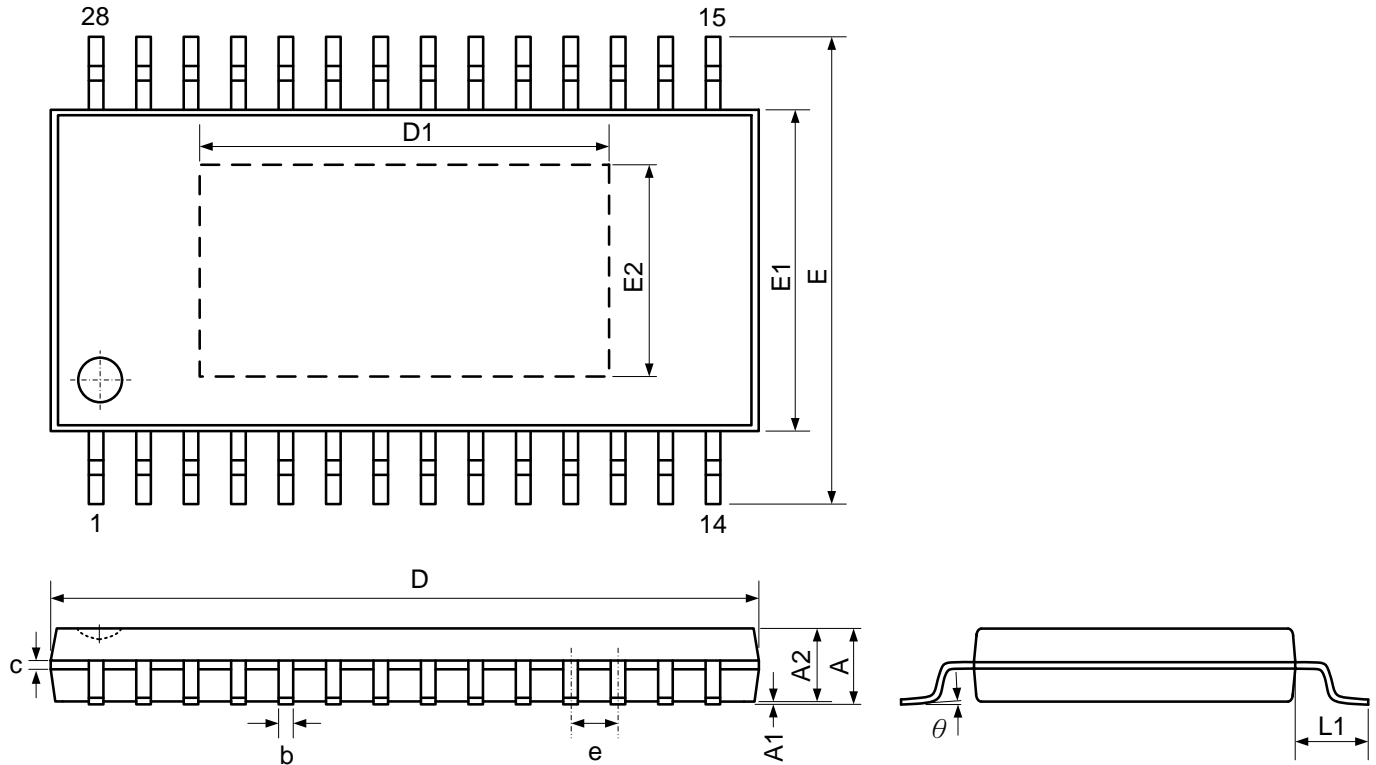
TA=25°C , VM=24V ,operating on static air flow ambient (unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply current	I_M	$V_M = 24V, R_{STN}=H$		10	13	mA
		$V_M = 24V, \text{sleep mode}$		20	30	μA
3V3REF REGULATOR						
3V3REF output voltage	V3P3	$I_{3V3} = 0 \text{ to } 1\text{mA}, V_M=24V$	3.18	3.30	3.42	V
CHARGE PUMP						
Charge pump output voltage	VCP	Between VCP and VM	4.5	5	5.5	V
LOGIC LEVEL INPUTS						
Input high level	V_{IH}		2.2		5.25	V
Input low level	V_{IL}			0.6	0.7	V
Input hysteresis	V_{HYS}			0.7		V
Input high current	I_{IH}	$V_{IN} = 3.3 V$		33	100	μA
Input low current	I_{IL}	$V_{IN} = 0V$	-20		20	μA
Internal pulldown resistance	R_{PD}			100		K Ω
Input deglitch time	T_{DG}	Input to output	2		3	μs
FALTN OUTPUT (OPEN-DRAIN)						
Output low voltage	V_{OL}	$I_O = 5\text{mA}$			0.5	V
Output high leakage current	I_{OH}	$V_O = 3.3 V$			1	μA
DECAY INPUT						
Input high voltage	V_{IH}	For fast decay mode	2			V
Input low voltage	V_{IL}	For slow decay mode	0		0.6	V
Input current	I_{IN}	-			± 20	μA
Internal pullup resistance	R_{UP}			250		K Ω
Internal pulldown resistance	R_{DN}			250		K Ω
H-BRIDGE DRIVER						
High side switch resistance	$R_{DS(HS)}$	$V_M = 24V, I_O = 1A, T_J = 25^\circ C$		0.2		Ω
		$V_M = 24V, I_O = 1A, T_J = 85^\circ C$		0.25	0.32	Ω
Low side switch resistance	$R_{DS(LS)}$	$V_M = 24V, I_O = 1A, T_J = 25^\circ C$		0.2		Ω
		$V_M = 24V, I_O = 1A, T_J = 85^\circ C$		0.25	0.32	Ω
Off-State Leakage Current	I_{OFF}		-20		20	μA
Output rise time	t_R	$V_M = 24V$	100		200	ns
Output fall time	t_F	$V_M = 24V$	50		150	ns
Crossover dead time	t_{DT}	$V_M = 24V$	40		200	ns

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
INTERNAL PWM CURRENT REGULATION						
Internal PWM current regulation frequency	f_{PWM}			50		KHz
VREFx input current	I_{REF}	VREFx = 3.3V	-3		3	μA
Current sense blanking time	t_{BLANK}			4	4.5	μs
ISENx trip voltage	V_{TRIP}	VREFx = 3.3V, 100% current setting	635	660	685	mV
		VREFx = 3.3V, 71% current setting	445	469	492	mV
		VREFx = 3.3V, 38% current setting	225	251	276	mV
Current sense amplifier gain	A_{SENSE}	Design Guarantee		5		V/V
PROTECTION CIRCUITS						
Overcurrent protection trip level	I_{OCP}		3.8	4.5		A
OCP deglitch time	T_{OCDG}			2	3	μs
Thermal shutdown temperature	t_{TSD}	Junction temperature	150	160	180	$^{\circ}C$
Thermal shutdown recovery window	t_{RW}			50		$^{\circ}C$
Under voltage lock out	UV_R	V_M rising		7.4	7.8	V
	UV_F	V_M falling		6.9	7.3	V

PACKAGE INFORMATION

28-PIN, HTSSOP, 173MIL



Symbol	Dimensions(mm)		
	Min.	Nom.	Max.
A	-	-	1.20
A1	0	-	0.15
A2	0.8	-	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	9.60	9.70	9.80
E1	4.30	4.40	4.50
E	6.4 BSC		
e	0.65 BSC		
D1	5.30	5.60	5.90
E2	2.50	2.80	3.10
L1	1.00 REF		
θ	0°	-	8°

Notes: Refer to JEDEC MO-153 AET

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