

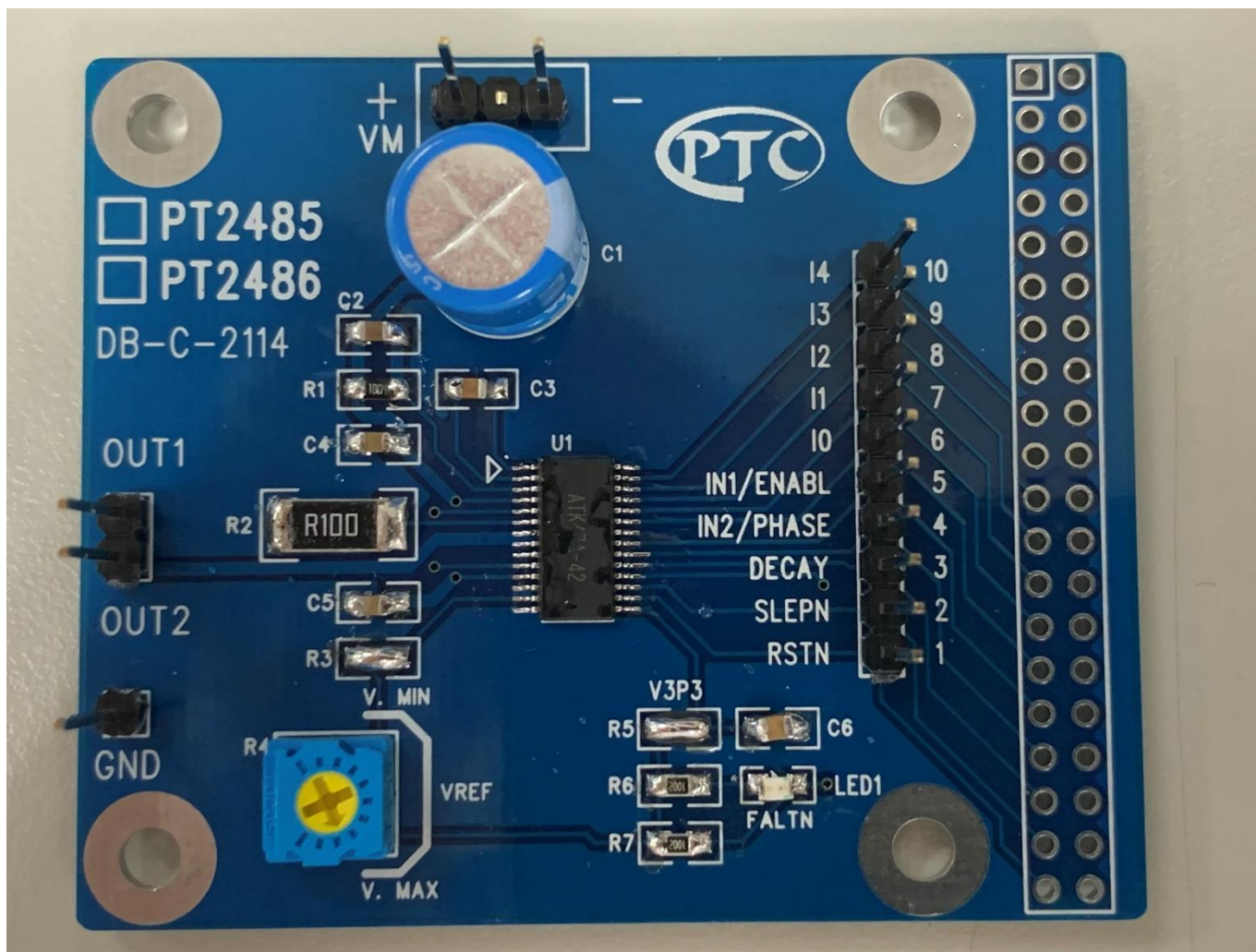
# PT2485 Demo Board Operation

2021/04/06

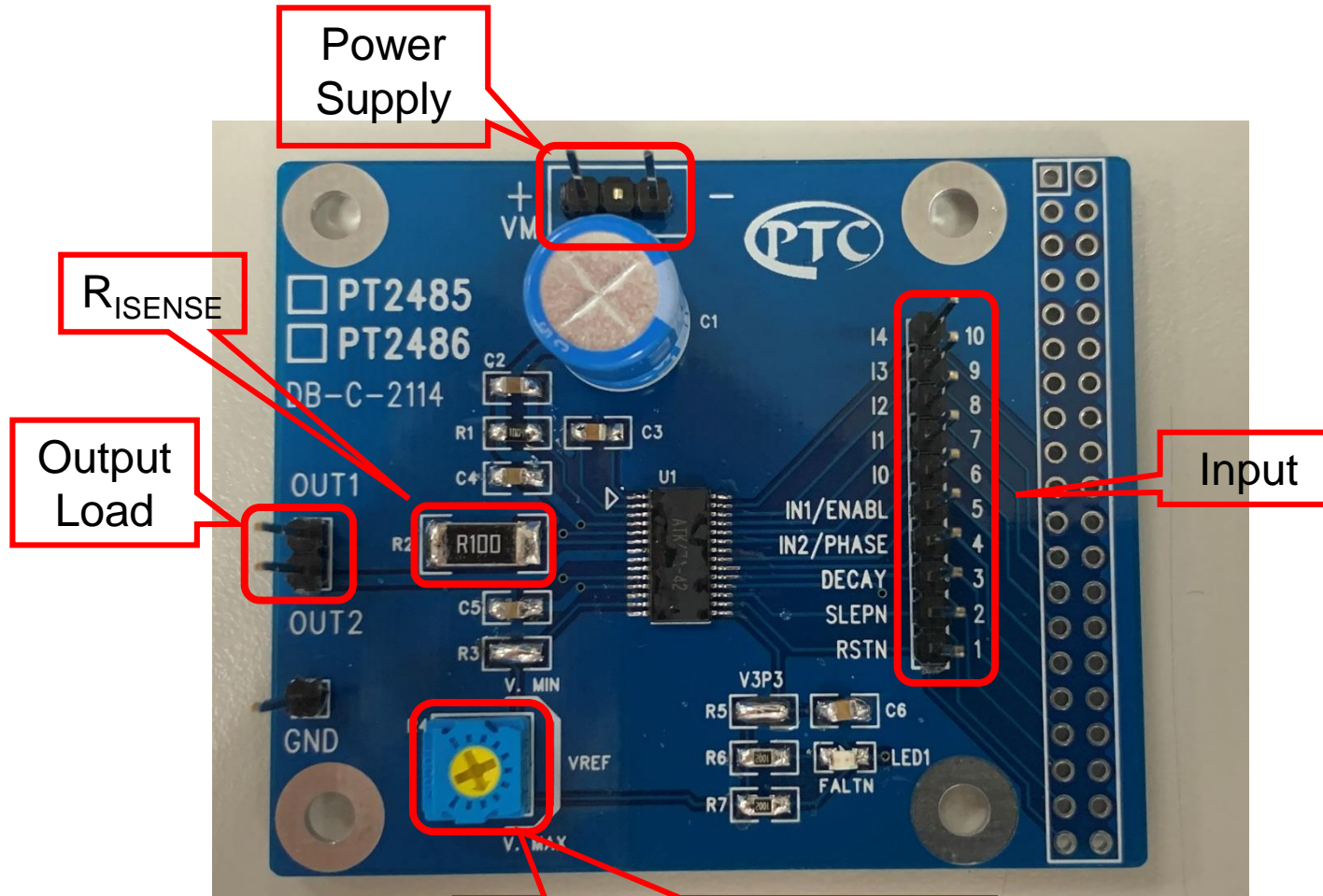
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# PT2485 EV Board Outline

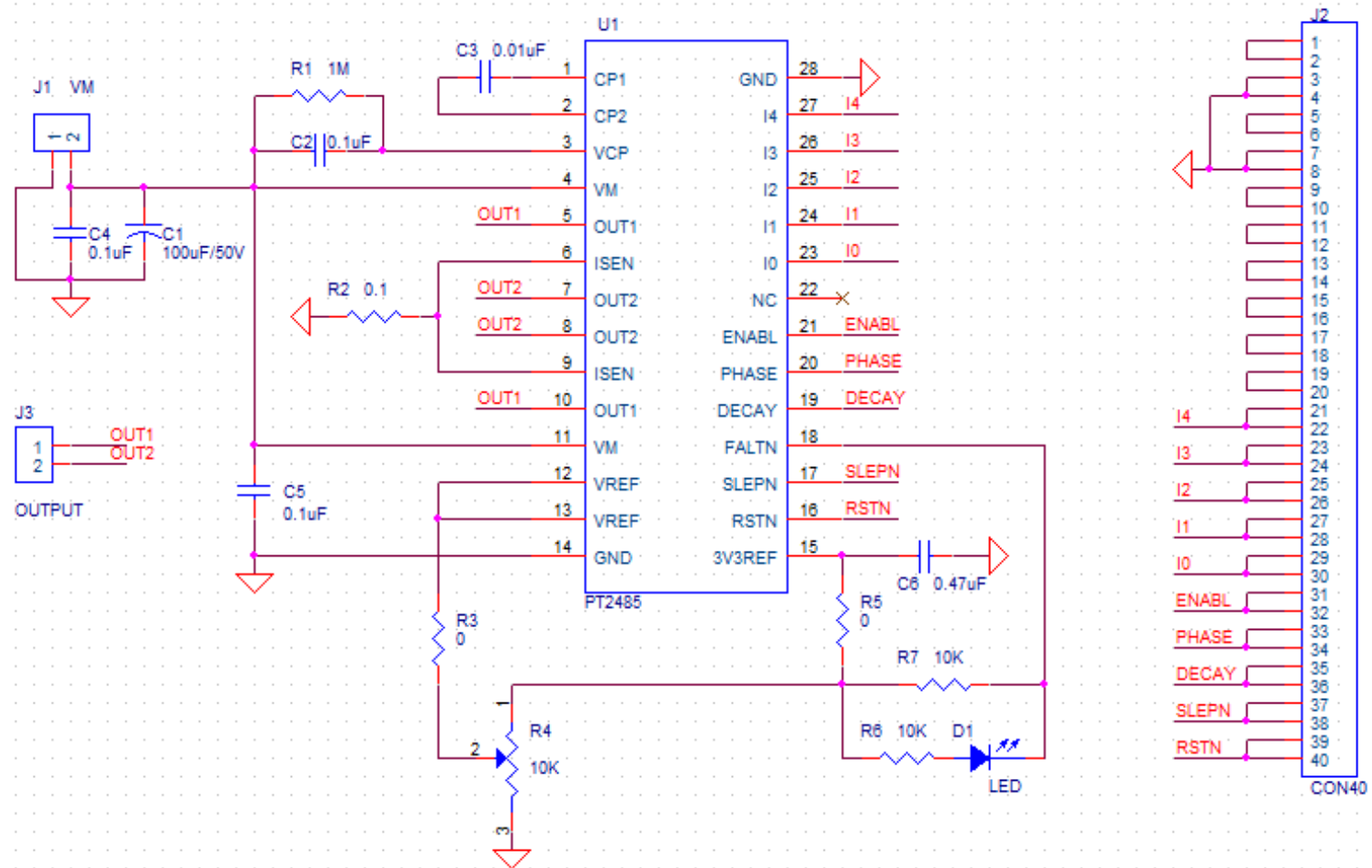


# PT2485 EV Board I/O Port Description



$$I_{CHOP} = \frac{V_{REF} \times DAC \text{ ratio}}{5 \times R_{ISENSE}}$$

# PT2485 EV Board Circuit



# PT2485 EV Board Input Pins Setting

I4	I3	I2	I1	I0	Hex Value	VREF DAC Ratio (% Full-Scale Chopping Current)
1	1	1	1	1	0x1Fh	100%
1	1	1	1	0	0x1Eh	100%
1	1	1	0	1	0x1Dh	99%
1	1	1	0	0	0x1Ch	98%
1	1	0	1	1	0x1Bh	97%
1	1	0	1	0	0x1Ah	96%
1	1	0	0	1	0x19h	94%
1	1	0	0	0	0x18h	92%
1	0	1	1	1	0x17h	90%
1	0	1	1	0	0x16h	88%
1	0	1	0	1	0x15h	86%
1	0	1	0	0	0x14h	83%
1	0	0	1	1	0x13h	80%
1	0	0	1	0	0x12h	77%
1	0	0	0	1	0x11h	74%
1	0	0	0	0	0x10h	71%
0	1	1	1	1	0x0Fh	67%
0	1	1	1	0	0x0Eh	63%
0	1	1	0	1	0x0Dh	60%
0	1	1	0	0	0x0Ch	56%
0	1	0	1	1	0x0Bh	51%
0	1	0	1	0	0x0Ah	47%
0	1	0	0	1	0x09h	43%
0	1	0	0	0	0x08h	38%
0	0	1	1	1	0x07h	34%
0	0	1	1	0	0x06h	29%
0	0	1	0	1	0x05h	24%
0	0	1	0	0	0x04h	20%
0	0	0	1	1	0x03h	15%
0	0	0	1	0	0x02h	10%
0	0	0	0	1	0x01h	5%
0	0	0	0	0	0x00h	0% (H-bridge disabled)

ENABL	PHASE	OUT1	OUT2
0	X	HiZ	HiZ
1	1	H	L
1	0	L	H