DESCRIPTION

The PT2505 is a three-phase, hall sensor sinusoidal brushless DC motor control chip with different protection mechanism. The three-phase control is based on sine wave driving scheme and it is designed to reduce electrical audible noise in motor phase commutation. On-chip +5V LDO provide voltage for logic and analog circuits operation. Combined with an external high voltage gate driver and six n-channel MOSFETs, PT2505 can operate with high voltage motor. The PT2505 offers OTP parameters setting to optimize with different motors and applications. PT2505 with package in SSOP24 and SSOP28. For SSOP24 package, its pin assignment is compatible to ROHM BD62017AFS.

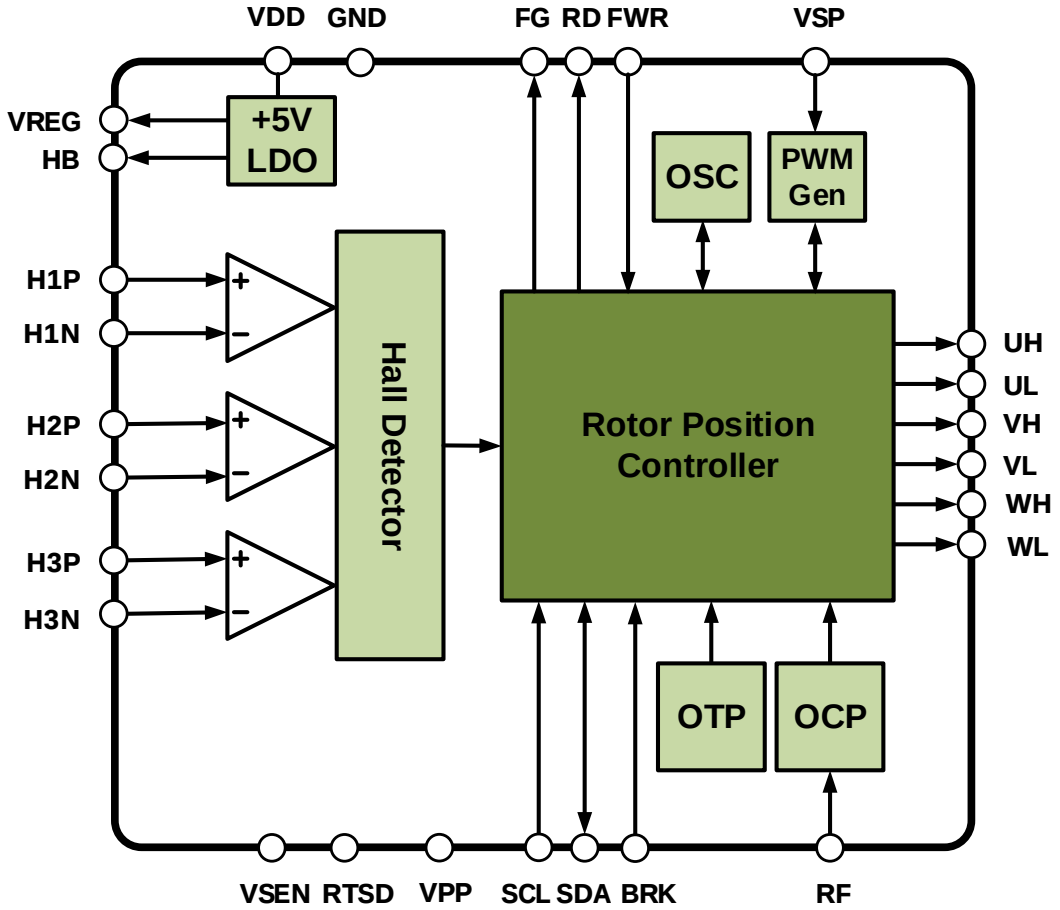
FEATURES

- Hall sensor sinusoidal control for 3-phase BLDC
- Operation voltage 9V to 28V
- Over Current Protection(OCP)
- Thermal Shut Down protection(TSD)
- Under Voltage Lock-Out protection(UVLO)
- Over Voltage Lock-Out protection(OVLO)
- Motor lock protection and fault input protection
- Reverse function with pin FWR.
- DC, PWM, I^2C or clock input for speed control
- FG output for rotation speed
- +5V logic output to drive external gate driver.
- Support Hall element and Hall sensor
- I^2C interface for parameter setting and write to internal OTP.

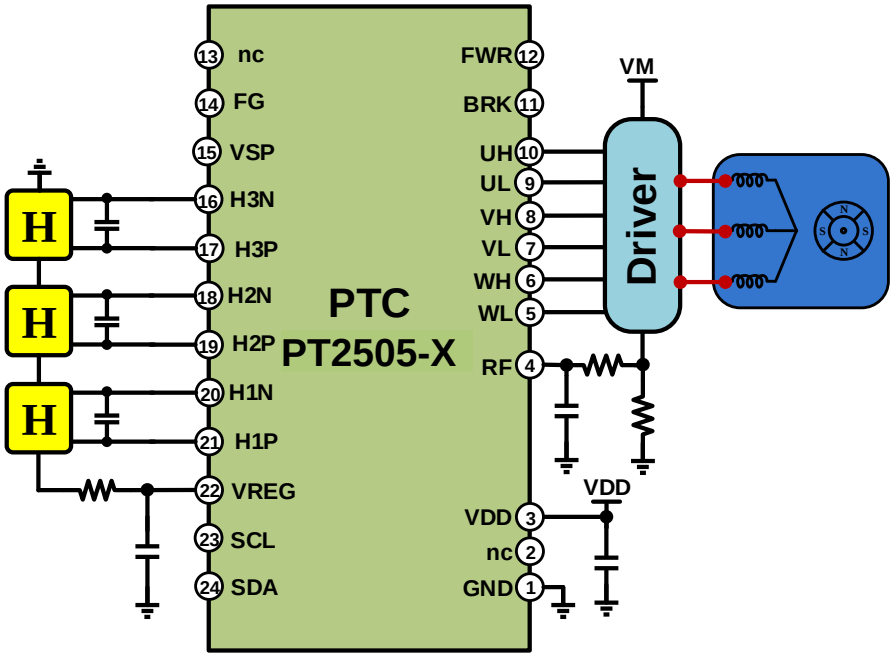
APPLICATIONS

- Three-phase BLDC motor
- Fan application

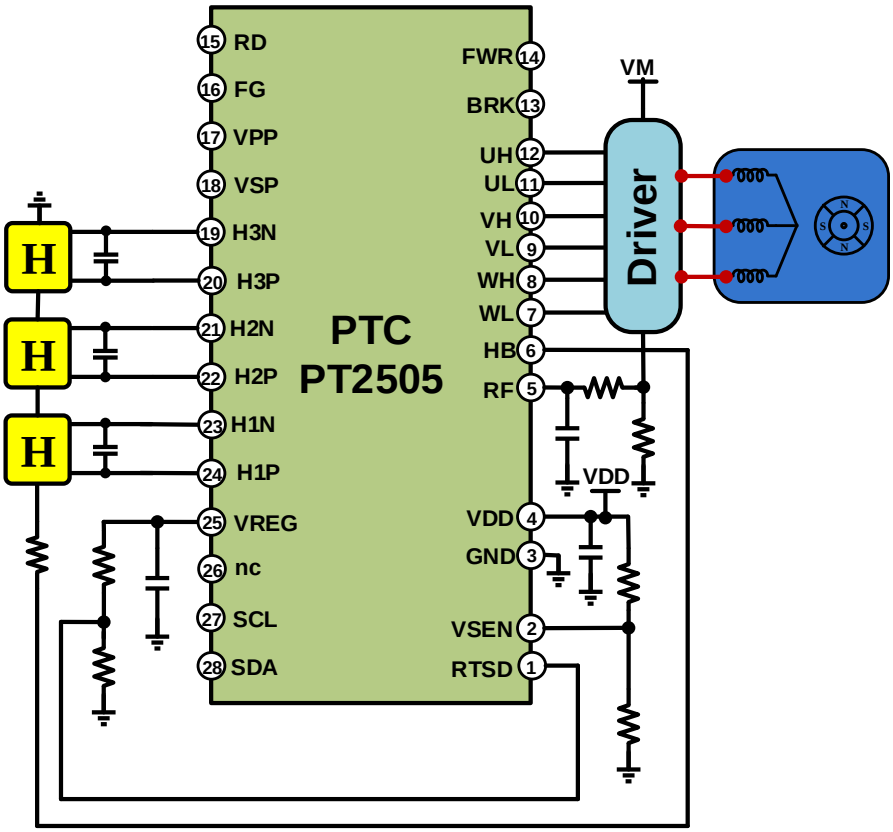
BLOCK DIAGRAM



APPLICATION BLOCK DIAGRAM – SSOP24



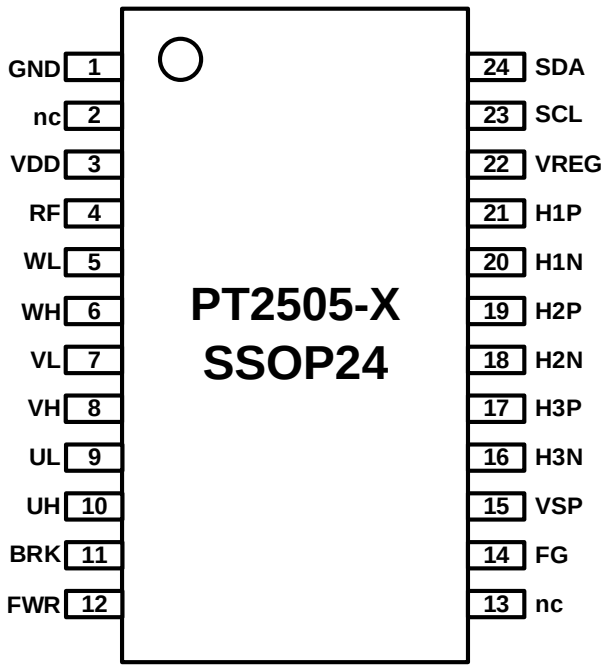
APPLICATION BLOCK DIAGRAM – SSOP28

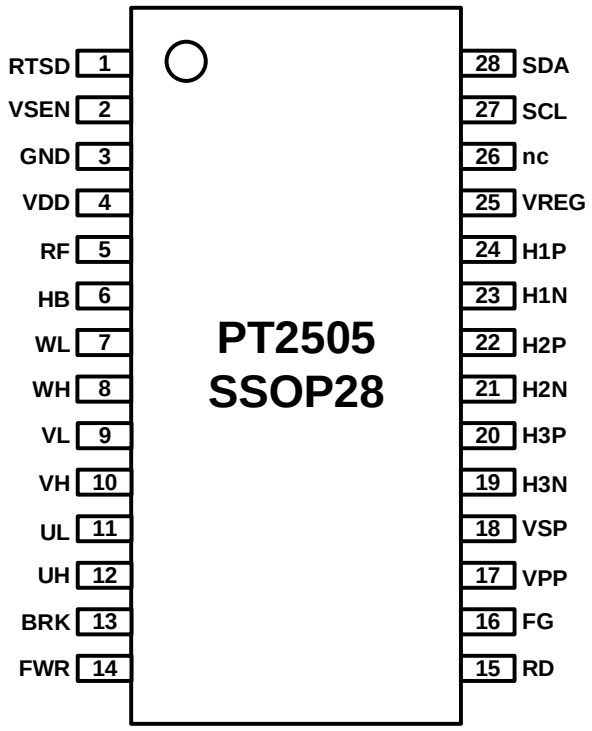


ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT2505-X	24-PIN, SSOP, 150MIL	PT2505-X
PT2505	28-PIN, SSOP, 150MIL	PT2505

PIN ASSIGNMENT





PIN DESCRIPTION

Pin Name	I/O/P	Description	24 Pin Pin No.	28 Pin Pin No.
GND	P	System ground	1	3
VDD	P	Power supply input	3	4
RF	I	Power MOS reference ground for current feedback	4	5
HB	O	Controlled +5V output for Hall sensor bias	nc	6
WL	O	W phase low side signal output	5	7
WH	O	W phase high side signal output	6	8
VL	O	V phase low side signal output	7	9
VH	O	V phase high side signal output	8	10
UL	O	U phase low side signal output	9	11
UH	O	U phase high side signal output	10	12
BRK	I	External brake input, low active, internal pull up	11	13
FWR	I	Forward/Reverse control, internal pull-high as forward	12	14
RD	O	Lock mode indicator, HIGH for abnormal event.	nc	15
FG	O	Motor rotation speed indicator, logic level output	14	16
VPP	O	VPP pin need apply +7.5V during OTP programming.	nc	17
VSP	I	DC or PWM input for speed control	15	18
H3N	I	Hall element 3 input-	16	19
H3P	I	Hall element 3 input+ or Hall sensor input	17	20
H2N	I	Hall element 2 input-	18	21
H2P	I	Hall element 2 input+ or Hall sensor input	19	22
H1N	I	Hall element 1 input-	20	23
H1P	I	Hall element 1 input+ or Hall sensor input	21	24
VREG	O	+5V LDO output	22	25
SCL	I	Serial clock input - I^2C control interface	23	27
SDA	I/O	Serial data input/output – I^2C control interface	24	28
RTSD	I	Thermal shutdown sensing resistor connection	DB	1
VSEN	I	Operation voltage protection sensing connection	DB	2

FUNCTION DESCRIPTION

POWER SUPPLY

PT2505 consumes very low current (<5mA) and build-in a 5V LDO for logic and analog circuits. The output driving signal is 5V logic to gate driver application. PT2505 will detect VREG and stop system when it lower than 3V to avoid unstable power supply. When the power supply is restored, a power good signal will send to logic circuit and system will start operation within 10ms. Adding proper bypass capacitor(s) close to the sensible IC pins will reduce interference from motor systems or wires and improve chip performance.

For Hall sensor/Hall element, the PT2505 HB pin provides a 5V power supply voltage. When the system is in the standby state, it can be turned off through parameter settings to save more power. HB can provide about 10mA current, it is recommended to series a 100Ω resister to limit current between HB and Hall device power supply. When the Hall device requires a higher voltage or current, the HB pin can also be used as a control signal to external power supply.

For internal one-time programming memory (OTP), PT2505 internally provides 7.5V VPP voltage. It only turns on automatically when the memory is being programmed. When OTP is in the programming state, the VDD voltage should be higher than 9V to ensure that the VPP voltage is sufficient.

SPEED CONTROL INTERFACE

The PT2505 has I^2C, DC voltage, PWM and Clock to change the motor speed. For PWM and Clock input, the HIGH voltage level and the LOW voltage level should be compliant with 3.3V and 5V logic system. PT2505 also uses the above speed control interface to provide closed-loop speed control via register settings. The PWM carrier frequency is recommended between 1 KHz to 25 KHz. For DC input, the DC control voltage should range from V_{SPMIN} to V_{SPMAX}. The VSP pin is pulled down internally by a 200kΩ resistor. Therefore, note the impedance when setting the VSP voltage with a resistance voltage divider.

To work for different VSP range, the V_{SPMAX} and V_{SPMIN} are controlled with registers setting. The V_{SPMAX} range from 3.0V to 5.4V and the V_{SPMIN} range from 0.3V to 2.1V. The operation shown as **Figure 1**

a. VspSel select VSP go directly to a comparator or attenuate its value to 2/3*VSP
b. OschSel and OsclSel to set the peak and valley value of the ramp waveform.
c. OschSel is register selected to (3V, 3.6V). OsclSel is register selected to (0.3V, 0.5V, 0.7V, 1.4V)
d. The combination for V_{SPMAX} and V_{SPMIN} are
   Set1: V_{SPMAX} = (3V, 3.6V) / V_{SPMIN} = (0.3V, 0.5V, 0.7V, 1.4V)
   Set2: V_{SPMAX} = (4.5V, 5.4V) / V_{SPMIN} = (0.45V, 0.75V, 1.05V, 2.1V)
e. The controlled register is 0x54

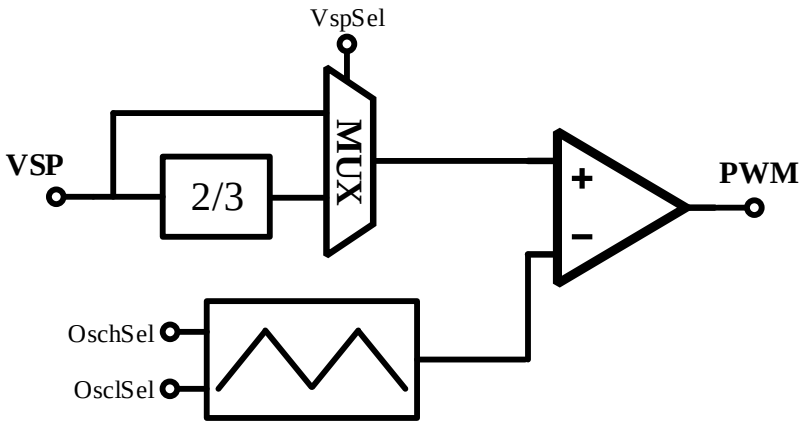


Figure 1. VSP input range explanation

HALL SENSOR CONTROL SCHEME

The PT2505 control scheme is based on hall sensor information and produce sinusoidal excitation waveform. It benefits to provide accurate and silent (without electrical noise) driving control. Unlike the sensorless control scheme, hall sensor control provides smooth start-up without reverse rotation.

As shown in **Figure 2** and **Figure 3**, three hall sensors can be configured as 60° or 120° spacing through internal parameter, **PhCode**, 0: 60 degree spacing, 1: 120 degree spacing.

Figure 2. 120 degree spacing of the hall signals

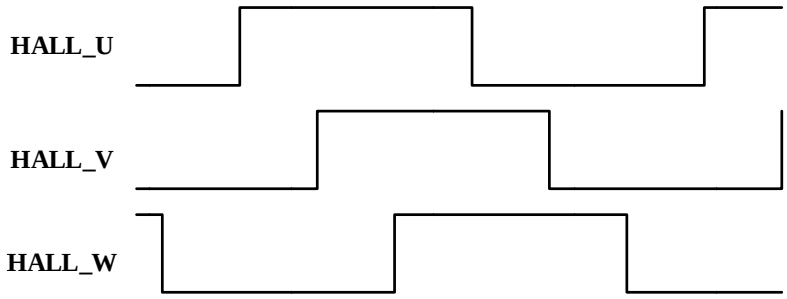


Figure 3. 60 degree spacing of the hall signals

The hall sensor has different sensitivity and layout distance from the rotor to cause phase offset. As shown in **Figure 4**, PT2505 can synchronize the phase offset related to HALL_U, range from -60 degree to 60 degree through internal parameters, **SyncAng** and **RSyncAng**. The phase offset is set individually for the forward or reverse rotation.
PT2505 also support different type or sensitivity hall device, for examples, hall IC or hall element.

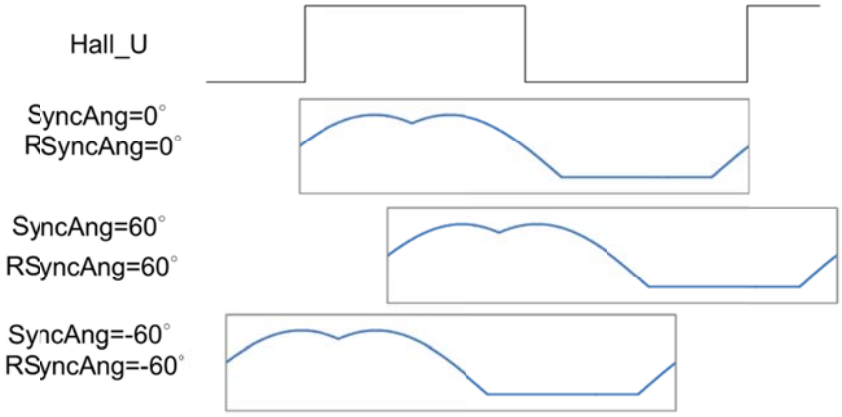


Figure 4. Phase offset setting of the hall sensor signal

PHASE ADVANCE SETTING

Due to the characteristics of inductance loading of stator winding, the phase of the shunt current may drift away as the rotor speed increase. The PT2505 provide automatic or manual adjustment through the setting **PAAuto** in address 0x30. It's easy for customer to achieve best efficiency in any circumstance. In the automatic setting, it provides sixteen curves **PASlope** and one maximum phase leading limitation **MaxPA** to choose.

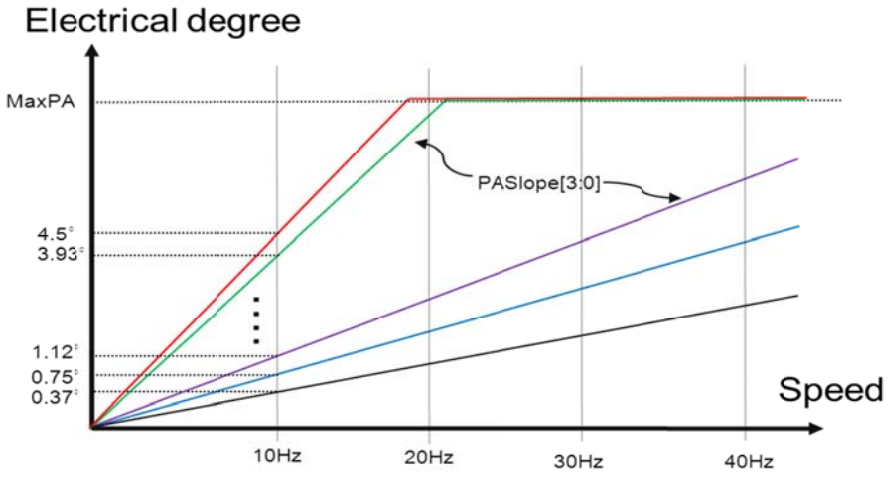


Figure 5. Automatic phase advance slope selection

Moreover, the best efficiency point may vary with the intensity of back EMF, shunt current, rotor speed and shunt inductance, etc. With the non-linear characteristic, the parameters of **PAM10HZ~PAM150HZ** help to adjust phase advance in individual rotation speed manually. The maximum manual adjustment speed is up to 150Hz. And the maximum phase leading limitation **MaxPA** is also applied in manual mode.

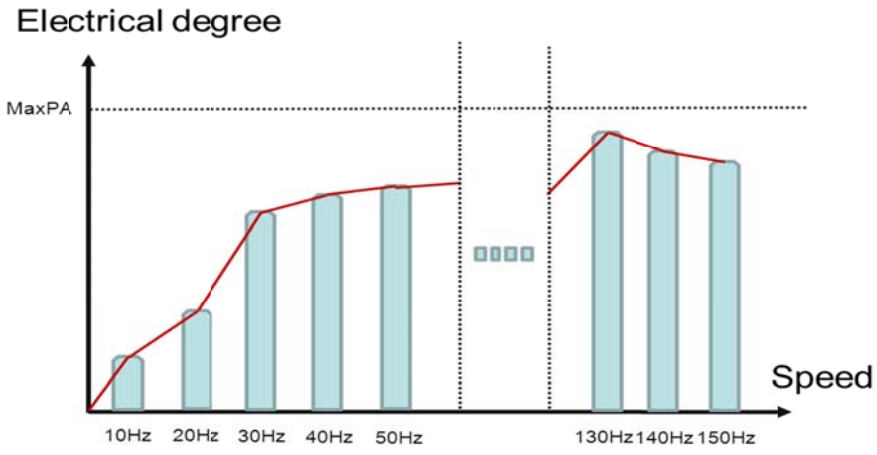


Figure 6. Manual phase advance setting according to speed

INPUT COMMAND PROFILE

PT2505 provide smooth speed up/down profile with different load as depicted in **Figure 7**. With the **StopDuty** setting, user can decide when to release the excitation to reduce the audible current noise caused by the reverse current during the deceleration.

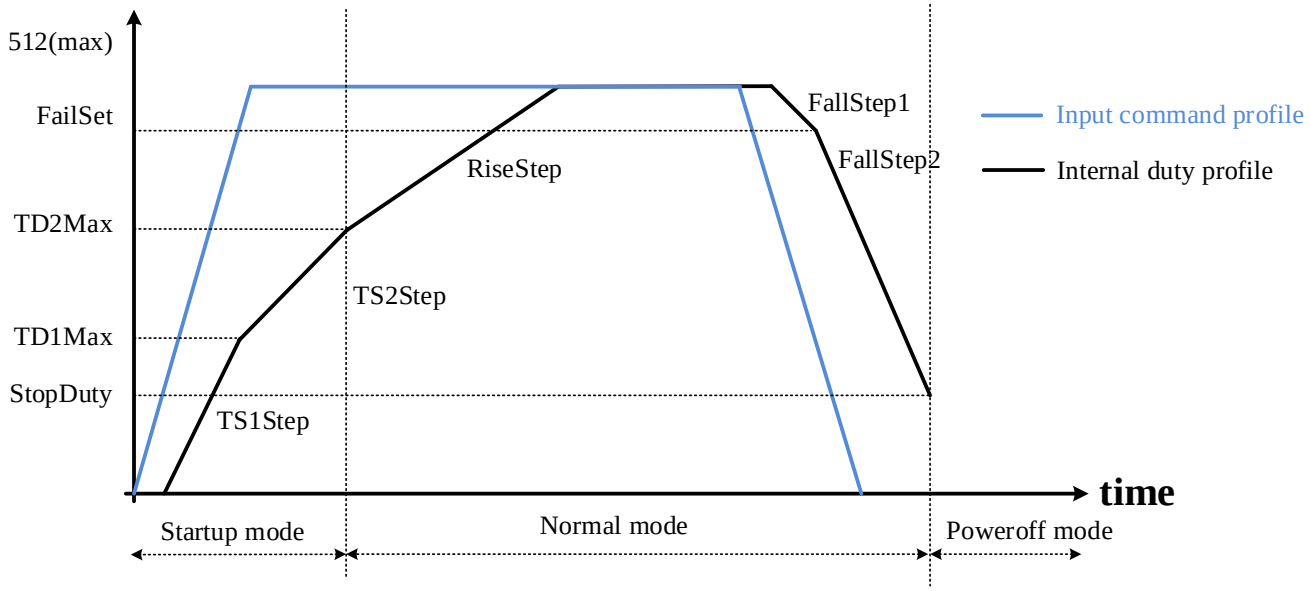


Figure 7. Smooth parameter for speed up/down.

CURRENT PROTECTION

The PT2505 has a two-level current protection function by using a sense resistor over RF pin and the sensed signal (V_{RF}) are related to motor current**(Imotor)** after low pass filter. When the V_{RF} exceeds V_{OCPL}, **OCPL** signal is triggered, PWM duty will reduce to keep V_{RF} under V_{OCPL} threshold. And if the V_{RF} exceed V_{OCPH}, **OCPH** signal is triggered, PWM turnoff and system go into the lock mode.

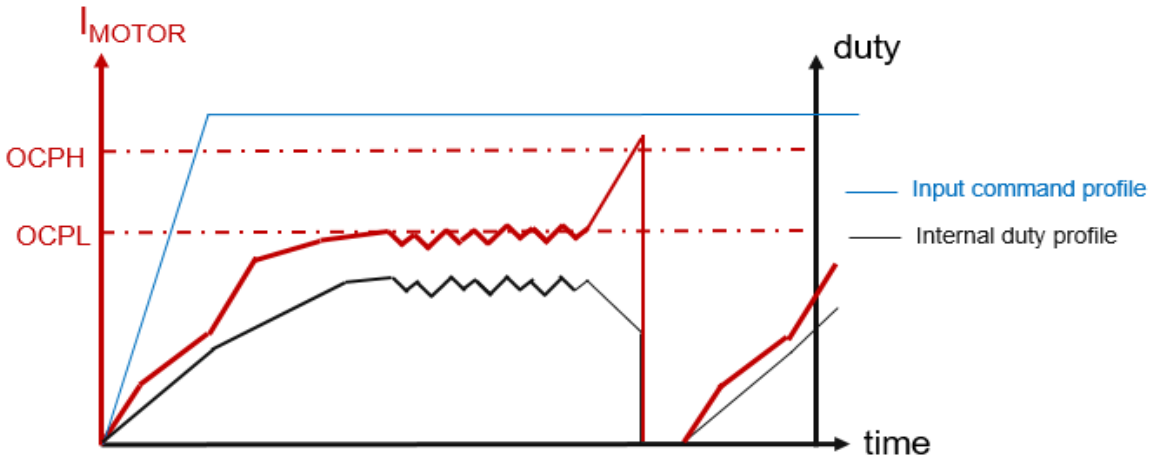


Figure 8. Two-stage over current protection

The **OCPHFilter** and **OCPLFilter** provide deglitch time period ranging from 0.4us to 0.4ms to make sure stable motor operation. Due to the different applications, PT2505 provide multi-level V_{OCPL}/ V_{OCPH} setting through **OCPLsel/OCPHsel** register(0x5A). In addition, PT2505 provide **OCPLL** setting, to limit motor maximum startup current.

START UP & LOCK PROTECTION

The initial position information is provided by hall sensor. According to hall signal, PT2505 commutates motor and startup. The startup mode maximum duty is set by **TD2Max**, in other words, the maximum startup force for different motor application. Increasing / decreasing PWM duty, the motor speed can be accelerated/ decelerated. And the profile can be set from parameters.

If the controller did not detect the expected hall sensor signal, the state machine would go to the lock protection mode. PT2505 will wait a period and re-start again (the period and re-start times are set by internal parameter **CTRise** and **CTFall)** and the **ExptNum** exception number counter will plus 1. If the motor remained to be locked, and the counter number exceed the **MaxExptNum** setting, it would cause system fall into the dead lock status. System no longer start at this state, and the only way to restart the system is turning off then turning on the supply voltage.

THERMAL SHUTDOWN PROTECTION AND EMERGENCY BRAKE

PT2505 supports external or internal temperature protection.

When **OTPSEL=**1, the PT2505 will stop operation for IC temperature over 150℃, this condition will release until the temperature is under 95℃. User can monitor the TSD bit in system status register **SYS_CTRL2**.

When **OTPSEL=0,** a temperature sense resistor is placed outside the chip, the sensed voltage is sent to RTSD.
If the sensed voltage is lower than V_{REFL}, then TSD is occurred. If the sensed voltage send to RTSD is higher than V_{REFH}, then TSD is released. The RTSD and NTC(Negative Temperature Coefficient) resistor connection method is shown in **Figure 9**.
When the BRK input is LOW, PT2505 will put the output power device upper arm OFF and lower arm SHORT immediately as a brake action to the motor.

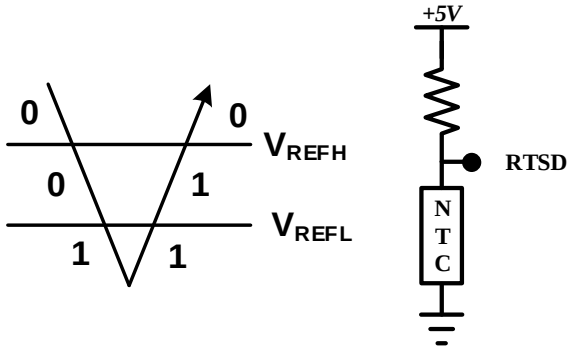


Figure 9. Thermal shutdown protection trigger level and NTC connection method

OPERATION VOLTAGE PROTECTION

PT2505 can operate with different under voltage lock-out(UVLO) and over-voltage lock-out(OVLO) condition,
When **OvphSel** =0(see Figure 10 left),
a. No over voltage protection provided.
b. For VDD < 8V, the UVLO condition is happened; For VDD > 9V, the UVLO condition is released
When **OvphSel** =1(see Figure 10 right),
a. A resistor divider from VDD send the divided voltage to pin VSEN
b. The OVLO condition is happened when the VSEN voltage is larger than 3.5V
c. The UVLO condition is happened when the VSEN voltage is lower than V_{PRTL}, V_{PRTL} is adjustable from 0.8V to 3.2V
Either UVLO or OVLO is happened, the **OVP** bit in system status register **SYS_CTRL2** will be set and it will also stop PT2505 to operation.

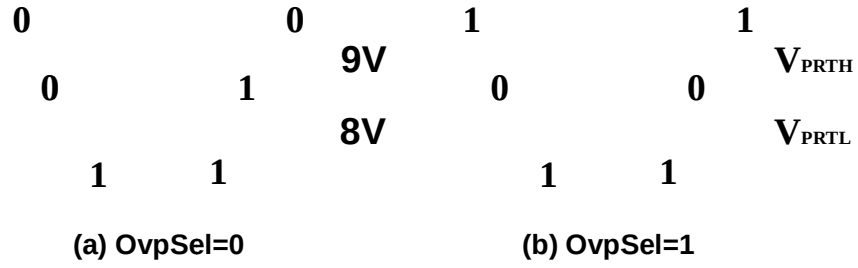


Figure 10. Operation Voltage Protection for OvpSel=0 and OvpSel=1

FG OUTPUT FOR SPEED INFORMATION

PT2505 has FG output to observe motor speed. When the rotor is running an electric cycle, the FG output toggles High to Low. So when calculating the rotation speed, it needs to take into account the pole numbers of the rotor. For example, if rotor is 8 poles (four pairs of NS), the motor run a lap will have 4 FG output. Motor speed is usually present in RPM (Revolutions per Minute), so the rotation speed of the simple formula is calculated as

RPM = FG x 120 / POLE, FG is frequency in Hz, “POLE” is numbers of rotor.

PT2505 provide different FG configuration for external device to access, as the **Figure 11** depicted. XOREn setting enable three times factor and FGDiv provide divided by 1,2,4,8 setting. FG pin is a 5V logic output.

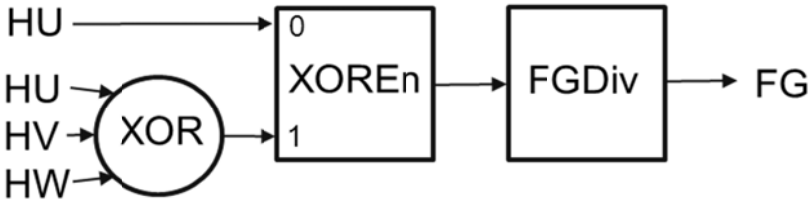


Figure 11. FG output configuration

FORWARD AND REVERSE ROTATION SETTING

PT2505 can use external FWR pin or internal parameters to set PT2505 to forward or reverse rotation. If the direction of rotation is switched during operation, the motor will automatically stop and rotate in the opposite direction. It is recommended to control the motor speed by monitoring the FG signal to optimize the reverse behavior, such as deceleration curve or reverse start waiting time.

UPWIND OR DOWNWIND STARTUP SETTING

PT2505 can automatically detect whether the motor is rotating and whether the direction is forward or reverse before starting. These rotations may be gliding or external forces, such as downwind and upwind. In order to ensure the normal operation of the motor, the PT2505 will first apply the braking method under upwind conditions until the rotor speed drops to an acceptable range before starting. Under downwind conditions, the PT2505 provides a solution to adjust the start-up duty cycle to avoid excessive back-EMF damage to the circuit due to power difference transfer. During this period, the starting duty cycle is reduced by a certain percentage according to the rotor speed, and then a compensation value is added.

StartDudy=(RotorSpeed>>DNWScale) + DNWInit, where“>>” means shift for a ratio

PARAMETERS PROGRAMMING

PT2505 provides flexible parameter adjustment function, which can be instantly adjusted and stored in the temporary register. After the IC is powered off, the register value will be cleared. When the IC is powered on again, the register will first read the programmed parameters within the OTP. If the OTP has not been programmed, the register will read the IC default value.

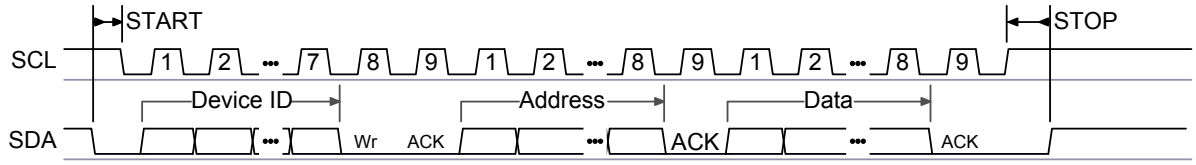
The adjusted parameters can be written to the internal one-time programming (OTP) memory. OTP memory can be burned through the I2C interface, PT2505 has 2 sets of storage space (bank0 & bank1), can provide two burns. During OTP programming, +7.5V needs to be applied to the VPP pin. Through VDD step-down, 7.5V is generated inside PT2505, providing VPP voltage. However, when the external VDD voltage is too low (<9V), the internal VPP voltage may be less than 7.5V. It is recommended to apply 7.5V voltage to the VPP pin or increase the VDD voltage to ensure that the OTP programming is effective.

In addition to using internal OTP to store parameters, another way is through I2C control. If the system has another MCU, the user can store the parameters in the MCU, and the parameters will be transferred to the PT2505 temporary register by the I2C every time it is turned on. The MCU can also dynamically change the parameters needed to achieve a more flexible control mode according to the needs.

I^2C *MICROPROCESSOR INTERFACE*

To communicate with PT2505, the following control and status registers are accessible via I^2C interface. I^2C communicates with multiple devices by only two lines, **START** bit means a start condition; any transmission must start with it. **Device ID** is 7-bit device address identifier, each device owns only one address, and PT2505 is fixed to 0110100b. **Wr/Rd** issuing a read or write operation, **ACK** is acknowledge bit, perform in the receiver, to inform the transmitter the data is properly received or stop data transmitting. **Address** is PT2505's register number to be described in next section. **STOP** is stop bit; any sequence must end with it. The I^2C write operation is byte write mode, and read operation is byte read mode as described in **Figure 12**. The current I^2C protocol speed support up to 50 KHz.

I^2C Byte Write



I^2C Byte Read

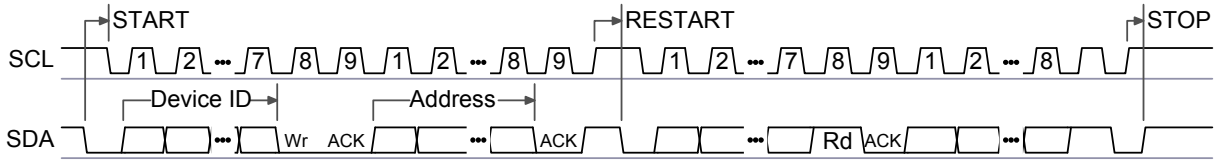


Figure 12. I^2C byte write and byte read timing.

REGISTER TABLE

Register table mapping for address 0x0~0x0b

Bit								Address
7	6	5	4	3	2	1	0	Hex
PWM_I2C[9:8]		Reserved			PWMS	FWRS[1:0]		0
PWM_I2C[7:0]								1
FGCnt[7:0]								2
Mstate[2:0]			RDL	TSD	FGCnt[10:8]			3
OVP		FLD	SumErr	BlankErr[1:0]		OCPL	OCPH	4
Reserved	Reserved	Reserved	VppAlarm	Reserved				5
HVID								6
ExpNum[7:0]								7
Reserved							ExpNum[8]	8
ActDuty[7:0]								9
Reserved						ActDuty[9:8]		0A
NumID								0B
PTM				PCTL				10

Register table mapping for address 0x21~0x5E

								20
TS1Step[7:0]								21
TD2Max[7:0]								22
TS1Step[8]	DnWScale[1:0]		TD1Max[5:0]					23
TS2Step[7:0]								24
RiseStep[7:0]								25
DnWInit[5:0]						TS2Step[8]	RiseStep[8]	26
FallStep1[7:0]								27
FallStep2[7:0]								28
HallP[2:0]			DeadTime[2:0]			FallStep1[8]	FallStep2[8]	29
FallSet[7:0]								2A
StopDuty[7:0]								2B
OCPHDis	Reserved	HallSel		Reserved				2C
Reserved								2D
FilterMax[9:8]		Reserved						2E
FilterMax[7:0]								2F
HallPwrEn	OCPLSlope[1:0]		PAAuto	PASlope[3:0]				30
RSyncAng[7:0]								31
SyncAng[7:0]								32
CTRise[3:0]				CTFall[3:0]				33
Deadlock[7:0]								34
TimeUp1[7:0]								35
HsfEn	Deadlock[8]	TimeUp1[13:8]						36
TimeUp2[7:0]								37
Reserved		TimeUp2[13:8]						38
HsMos	HallCode	Reserved	IfDiv	SpdEn	FreqEn	SpdHyst[1:0]		39
Reserved								3A
MaxPA[7:0]								3B
Pam10Hz[7:0]								3C

Pam20Hz[7:0]							3D
Pam30Hz[7:0]							3E
Pam40Hz[7:0]							3F
Pam50Hz[7:0]							40
Pam60Hz[7:0]							41
Pam70Hz[7:0]							42
Pam80Hz[7:0]							43
Pam90Hz[7:0]							44
Pam100Hz[7:0]							45
Pam110Hz[7:0]							46
Pam120Hz[7:0]							47
Pam130Hz[7:0]							48
Pam140Hz[7:0]							49
Pam150Hz[7:0]							4A
TrimClk[7:0]							4B
OVPSel[3:0]				Reserved			4C
OCPHFltr[7:0]							4D
OCPLFltr[5:0]						OCPHFltr[9:8]	4E
UpWSel[1:0]	TSOVDis	Reserved		HallUP	HallVP	HallWP	4F
UpWNum[7:0]							50
MinDuty[7:0]							51
Reserved							52
Reserved					FGDiv[1:0]	HXorEn	53
VspSel	OschSel	OsclSel[1:0]		LdoTrim[3:0]			54
Reserved					OvphSel	OtpSel	55
MaxDuty[7:0]							56
Reserved				PWMSmp	MaxDuty[9:8]		57
Reserved							58
HSmthEn	HSmthT	Reserved	OneHall	UVWP[2:0]			59
OCPLSel[3:0]			OCPHSel[3:0]				5A
Reserved					VspOffBk	Reserved	5B
SDutyCtl[3:0]			Reserved	AlignTime[2:0]			5C
Reserved	IRSpd[2:0]		Reserved	Racc[2:0]			5D
HzPDuty[7:0]							5E

REGISTER DESCRIPTION

Address 0x00~0x11 is system control registers, providing information such as system status, even direct control the PWM duty, forward or reverse, etc.

Address	Register Name	Description		Unit	Default	R/W
0x00	**SYS_CTL1**	Bit[7:6]	**PWM_I2C**[9:8]		0x00	R/W
		Bit[5:3]	Reserved			
		Bit[2]	**PWMS,** PWM Selection 1 : use I2C(UI) for PWM duty control 0 : external VSP pin control			
		Bit[1:0]	**FWRS**, FWR is controlled by 0x: external FWR pin 10: use I2C(UI) as reverse 11: use I2C(UI) as forward			
0x01	**PWM_I2C**	**PWM_I2C**[7:0]: When PWMS set 1, PWM duty is controlled by PWM_I2C[9:0]		duty	0x00	R/W
0x02	**FGCnt**	Combine FGCnt[10:8] to get a 11 bit frequency counter value for every second		count	0x00	R
0x03	**MState**	Bit[7:5]	Motor status 0:Startup 1:Normal 2:PWM Off 3:Align Start Up 4:Lock On 5:Dead Lock 6:Power Saving Ack 7:Power Saving		0x40	R
	RDL	Bit[4]	Normal operation status 0 : motor is in the normal state 1 : motor is not in the normal state			
	TSD	Bit[3]	TSD signal from the RSEN pin 0 : Comparator result is correct 1 : Comparator result is not correct			
		Bit[2:0]	FGCnt[10:8]			
0x04	**OVP**	Bit[7]	Overvoltage Protection: 0: Normal 1: Overvoltage happening		0x00	R
		Bit[6]	Not used			
	FLD	Bit[5]	Frequency lock up detection 1: Frequency locked up 0: Frequency not locked up			
	SumErr	Bit[4]	OTP checksum error indicator. If the first byte is 0x5A, the checksum is generated automatically. 1 : OTP checksum is error 0 : OTP checksum is correct.			
	BlankErr	Bit[3:2]	OTP blanking check. 00 : Bank 0 and 1 is blank. 01 : Bank 0 is blank, bank 1 is not blank. 10 : Bank 0 is not blank, bank 1 is blank. 11 : Bank 0 and 1 is not blank.			
	OCPL	Bit[1]	1 : RF pin voltage exceed low level threshold. 0 : RF pin voltage is under low level threshold.			
	OCPH	Bit[0]	1 : RF pin voltage exceed high level threshold. 0 : RF pin voltage is under high level threshold.			

Address	Register Name	Description		Unit	Default	R/W
0x05		Bit[7:5]	Reserved		0x10	
	VppAlarm	Bit[4]	VppAlarm Signal 0: VPP OK 1: VPP abnormal			R
		Bit[3:0]	Reserved for system test			
0x06	**HVID**	**HVID**, Hardware version control ID			0x00	R
0x07	**ExpNum**	Combine with ExpNum[8] to get a ExpNum[8:0] register. The EXPTNUM will add one automatically when exception happens, for example, OCPH or LockOn state happens.		count	0x00	R
0x08		Bit[7:1]	Reserved		0x00	R
		Bit[0]	**ExpNum**[8]			
0x09	**ActDuty**	Combine with ActDuty[9:8] to get a ActDuty[9:0] register array. The register array means real work duty in motor system.		duty	0x00	R
0x0a		Bit[7:2]	Reserved		0x00	R
		Bit[1:0]	**ActDuty**[9:8]			

Address 0x21~0x5F is OTP parameters mapping registers, provide motor control related parameters.

Address	Register Name	Description		Unit	Default	R/W
0x21	**TS1Step**	Combine with bit 7 of sub-address 0x23 to form 9-bit of TS1Step[8:0] TS1Step is the first stage slope before reaching TD1MAX in the startup mode. Please refer to **Figure** 7. Unit is ms		0.25ms	0x0A	R/W
0x22	**TD2Max**	The maximum duty of the second stage startup. Please refer to **Figure** 7		4 duty	0x32	R/W
0x23		Bit [7]			0x03	R/W
	DnWScale	Bit[6:5]	A scale of current speed in Hz, for example, the current speed is 48Hz, DnwScale set to 3, then the initial duty is startup from (48>> 3)x4 +DnwInit.	scale		
	TD1Max	Bit[4:0]	The maximum duty of the first stage startup. Please refer to Figure 7	4 duty		
0x24	**TS2Step**	Combine with bit 1 of sub-address 0x26 to form 9-bit of TS2Step[8:0] TS2Step is the second stage slope before reaching TD2MAX in the startup mode. Please refer to **Figure** 7.		0.25 ms	0x2F	R/W
0x25	**RiseStep**	Combine with bit 0 of sub-address 0x26 to form 9-bit of RiseStep[8:0] RiseStep is the update slope before reaching the OCPL or desire speed setting. Please refer to **Figure** 7.		0.25 ms	0x2F	R/W
0x26	**DnWInit**	Bit [7:2]	Combine with Dnwcale[1:0], a suitable initial force to startup the motor when motor in a forward running situation.	4 duty	0x00	R/W
		Bit [1]	**TS2Step**[8]			
		Bit [0]	**RiseStep**[8]			
0x27	**FallStep1**	The first stage slope of slow down before the actual duty down to Fallset.		0.25 ms	0x2F	R/W
0x28	**FallStep2**	The second stage slope of slow down before the actual duty down to StopDuty		0.25 ms	0x2F	R/W
0x29	**HallP**	Bit[7:5]	Hall Input Permutation 0: [U， V， W] 1: [U， W， V] 2: [V， U， W] 3: [V， W， U] 4: [W， U， V] 5: [W， V， U] Others: [U， V， W]	clock	0x00	R/W
	DeadTime	Bit[4:2]	Dead time setting, range from 0.4us to 2.4us, suit for wide voltage operation. 0: 0.4us, 1: 0.8us, 2: 1.2us, 3: 1.6us, 4: 2.0us, 5~7: 2.4us			
		bit [1]	**FallStep1**[8]			
		bit [0]	**FallStep2**[8]			
0x2A	**FallSet**	The first stage duty for the actual duty decrease to.		4 duty	0x28	R/W
0x2B	**StopDuty**	When PWM off，PWM duty will decrease gradually，if it reach this setting, no PWM output any more		4 duty	0x40	R/W

Address	Register Name	Description		Unit	Default	R/W
0x2C	**OCPHDis**	Bit[7]	OCPH disable 1: OCPH function disable 0: OCPH function normal	count	0x06	R/W
		Bit[6]	Reserved			
	HallSet	Bit[5]	Hall selection 0: Hall Sensor 1: Hall element			
		Bit[3:0]	Reserved			
0x2D	**ZCCntMn**	Bit[7:0]	Combine ZCCntMn[13:8] to get a ZCCntMn[13:0]. The register array means the minimum pulse width of zero crossing signal.	4 clock	0xC8	
0x2E		Bit[7:6]	**FilterMax**[9:8]		0x00	R/W
		Bit[5:0]	**ZCCntMn**[13:8]			
0x2F	**FilterMax**	Combine with bit[7:6] of sub-address 0x2E, to form 10-bit of FilterMax[9:0]. FilterMax is the deglitch time period both for the hall sensor/hall element signal.		4 clock	0x64	R/W
0x30	**HallPwrEn**	Bit[7]	HB power output control 0: Turn off HB output during power-off mode, 1: HB output is always enable.	0	0x57	R/W
	OCPLSlope	Bit[6:5]	OCPL update rate selection when the OCPL event happens. 0: 1.5ms, 1: 3ms, 2:5.75ms, 4:11.75ms	msec		
	PAAuto	Bit[4]	**PAAuto**, Phase leading adjustment selection, 0: manually, 1: auto	1		
	PASlope	Bit[3:0]	When PAAuto set to 1, there are 16 slope curves selection according to the rotation speed. Please check **Figure 5** and **6** for further explanation. The sixteen slope of phase advance per 10Hz is 4.5, 3.93, 3.56, 3.18, 3.0 ,2.8, 2.6, 2.43, 2.25, 2.06, 1.87, 1.68, 1.5, 1.12, 0.75, 0.37 degree.	7		
0x31	**RSyncAng**	Hall sensor synchronization angle for the reversion rotation.		0.75 deg	0x5A	R/W
0x32	**SyncAng**	Hall sensor synchronization angle for the forward rotation		0.75 deg	0x5A	R/W
0x33	**CTRisel**	Bit[7:4]	Maximum time period before entering normal mode. If startup period exceed this period, lock-on number plus one and restart again.	0.5 sec	0x55	R/W
	CTFal	Bit[3:0]	Rest time period between each startup.	0.5 sec		
0x34	**DeadLock**	Combine DeadLock[8] to get a DeadLock[8:0]. The register array means the maximum exception number before entering dead-lock state. The exception includes OCPH and lock-on. When entering dead-lock state, PT2505 release it only by system power on again.		times	0x14	R/W
0x35	**TimeUp1**	Combine TimeUp1[13:8] to a TimUp1[13:0]. The register array means that the minimum time when zero crossing signals must toggle without toggling once before. With the condition, system will restart the motor.		1ms	0xE8	R/W

Address	Register Name	Description		Unit	Default	R/W
0x36	**HsfEn**	Bit[7]	Hall U signal sampling edge 0: positive edge sampling 1: positive and negative edge sampling		0x03	R/W
		Bit[6]	**DeadLock**[8]			
		Bit[5:0]	**TimeUp1**[13:8]			
0x37	**TimeUp2**	Combine TimeUp2[13:8] to get a TimeUp2[13:0] . The register array means that the minimum time when zero crossing signals must toggle with toggling at least once before. With this condition, system will restart the motor.		1ms	0xE8	R/W
0x38		Bit[7:6]	Reserved		0xC3	R/W
		Bit[5:0]	**TimeUp2**[13:8]			
0x39	**HsMos**	Bit[7]	High side MOS type selection 0:PMOS, 1:NMOS		0x00	R/W
	HallCode	Bit[6]	Hall effect sensor position 0: 60 degree spacing, 1: 120 degree spacing			
		Bit[5]	Reserved			
	IfDiv	Bit[4]	Input frequency divider for VSP speed command 0: divide by 1, 1: divide by 4			
	SpdEn	Bit[3]	Speed input enable in VSP pin 0: open loop control, 1: close loop control			
	FreqEn	Bit[2]	Frequency input enable in VSP pin. 0: Speed controlled by DC/PWM 1: Speed controlled by CLOCK			
	SpdHyst	Bit[1:0]	Speed Control Hysteresis setting 0: No speed hysteresis control. 1: 1/16 speed hysteresis(If the difference between desired and measured speed is lower than 1/16 desired speed, no further PWM adjusted) 2: 1/64 speed hysteresis 3: 1/128 speed hysteresis			
0x3B	**MaxPA**	Maximum phase advance limitation		0.75 deg	0x3C	R/W
0x3C~ 0x4A	**Pam10HZ~ Pam150HZ**	Phase advance adjusted manually from 10Hz to 150Hz according the rotation speed.		0.75 deg	2,4,6,8,10 ,12,13,15, 17,18,20, 21,23,24, 25	R/W
0x4B	**TrimClk**	8 bits provided to trim the system clock for reaching 10.24MHz		level	0xA4	R/W
0x4C	**OVPSel**	Bit[7:4]	Over voltage protection level(V_{PRTL}), selection, range from 0.8V~3.2V(0x0~0xE), 15 level settings.	level	0x88	R/W
		Bit[3:0]	Reserved			

Address	Register Name	Description		Unit	Default	R/W
0x4D	**OCPHFltr**	Combine with bit[1:0] of sub-address 0x4E, to form 10-bit of deglitch time period for the OCPH signal, range from 0.4us to 0.4ms.		4 clock	0x00	R/W
0x4E	**OCPLFltr**	Bit[7:2]	Deglitch time period for the OCPL signal, range from 0.4us to 25.6us.	4 clock	0x21	R/W
		Bit[1:0]	**OCPHFltr**[9:8]			
0x4F	**UpWSel**	Bit[7:6]	Upwind startup setting, the motor brake until the speed reach: 0:4Hz, 1:6Hz, 2:8Hz, 3:12Hz, then start up with six-step till the motor in the forward direction.		0x5F	R/W
	TSOVDis	Bit[5]	Thermal Shut down/Over Voltage Protection 0: with protection 1: without protection			
		Bit[4:3]				
	HallUP	Bit[2]	Hall U polarity 0: inverse Hall U 1: not inverse Hall U			
	HallVP	Bit[1]	Hall V polarity: 0: inverse Hall V 1: not inverse Hall V			
	HallWP	Bit[0]	Hall W polarity: 0: inverse Hall W 1: not inverse Hall W			
0x50	**UpWNum**	Upwind brake time limitation, When the brake time exceed **UpWNum***0.5 second then **ExpNum** add 1 and restart the upwind procedure		number	0x14	R/W
0x51	**MinDuty**	The motor is activated until the duty setting exceed **MinDuty**		2 duty	0x00	R/W
0x52		Bit[7:0]	Reserved		0x50	
0x53		Bit[7:3]	Reserved		0x00	R/W
	FGDiv	Bit[2:1]	FG divide setting, 0:1, 1:2, 2:4, 3:8			
	HXorEn	Bit[0]	**HXorEn**: FG XOR enable setting, 0:disable, 1:enable			
0x54	**VspSel**	Bit[7]	VSP input attenuation selection 0: no attenuation, 1: attenuate to 2/3*VSP		0x08	R/W
	OschSel	Bit[6]	PWM input high level setting 0: PWM input high level is set to 3V. 1: PWM input high level is set to 3.6V.			
	OsclSel	Bit[5:4]	PWM input low level setting 0: 0.3V 1: 0.5V 2: 0.7V 3: 1.4V.			
	LdoTrim	Bit[3:0]	4 bit for precise 5V output (VREG) adjustment			
0x55		Bit[7:2]	Reserved		0x80	
	OvphSel	Bit[1]	Operation voltage protection reference 0: internal 1: external			
	OtpSel	Bit[0]	Over temperature protection reference 0: internal 1: external			
0x56	**MaxDuty**	Combine MaxDuty[9:8] to get a MaxDuty[9:0]. The register array means maximum duty option		duty	0x00	R/W
0x57		Bit[7:3]	Reserved		0x22	R/W

Address	Register Name	Description		Unit	Default	R/W
	PWMSmp	Bit[2]	PWM sampling rate setting 0: 20KHz 1: 40KHz			
		Bit[1:0]	MaxDuty[9:8]			
0x58		Bit[7:0]	Reserved		0x12	
0x59	**HSmthEn**	Bit[7]	Hall U Sensor Signal Smooth 0: Disable 0: Enable		0x20	R/W
	HSmthT	Bit[6]	Hall U Sensor Signal Smooth Threshold on the condition HSmthEn = 1. 0: 1/8 1: 1/16			
		Bit[5:3]	Reserved			
	UVWP	Bit[2:0]	U/V/W drive signal permutation: 0: UVW 1: UWV 2: VUW 3: VWU 4: WUV 5: WVU Others: UVW			
0x5A	**OCPLSel**	Bit[7:4]	Over current protection level selection, range from 0.1V to 0.4V, 16 level settings.		0x88	R/W
	OCPHSel	Bit[3:0]	Over current protection level selection, range from 0.16V to 0.7V, 16 level settings.			
0x5B		Bit[7:2]	Reserved		0x00	R/W
	VspOffBk	Bit[1]	When PWM is off, braking enables or disables. 0: disable 1: braking until FG<= 4HZ			
		Bit[0]	Reserved			
0x5C	**SDutyCtl**	Bit[7:4]	Section Duty setting for speed control: 1~15: 1~15 section		0x75	R/W
		Bit[3:0]	Reserved			
0x5D		Bit[7:0]	Reserved		0x00	
0x5E	**HzPDuty**	The number of Hz per Duty for speed control by duties. Bit 7-6 : Integral part Bit 5-0 : Fractional part			0x40	R/W

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Max.	Unit
VDD supply voltage	VDD_{MAX}	PT2505 no break down	32	V
Input pin withstand voltage	Vin_{MAX}	FR, BRK, PWM, RTSD, ROVP	6	V
Operating temperature	T_{OPR}	No thermal shunt down	–40 to+85	°C
Storage temperature	T_{STG}	–	–40 to +150	°C

ELECTRICAL CHARACTERISTICS

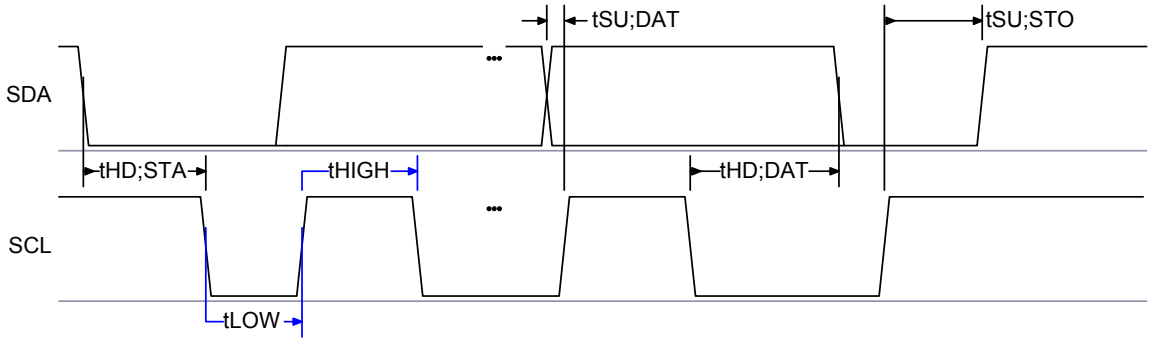
Nominal conditions: V_{DD} =24.0V, GND=0V, T_A = +27°C.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
General Characteristics						
Supply voltage	V_{DD}		9*	24	28	V
Current consumption	I_{DD}			5**	7	mA
Regulator output voltage	V_{REG}		4.75	5	5.25	V
Regulator output current	I_{REG}	Voltage drop < 5%		20		mA
Thermal Shutdown Protection (OtpSel=0, external TSD)						
Low protection voltage	V_{REFL}	RTSD pin		1.2		V
High protection voltage	V_{REFH}	RTSD pin		2.6		V
Under/Over Voltage Protection (OvphSel=1, external OVP)						
Low protection voltage***	V_{PRTL}	ROVP pin	0.8		3.2	V
High protection voltage	V_{PRTH}	ROVP pin		3.5		V
Under Voltage Lock Out (OvphSel=0, internal OVP)						
Release voltage	V_{UVH}		8.5	9	9.5	V
Lockout voltage	V_{UVL}		7.5	8.0	8.5	V
Hysteresis voltage	V_{UVHY}		0.5	1.0	1.5	V
Over Current Protection						
Over current protection voltage level low (OCPL, current limit)***	V_{OCPL}	RF pin	0.1		0.4	V
Over current protection voltage level high (OCPH, lock protection)	V_{OCPH}	RF pin	0.16		0.7	V
Driver Output						
Output low voltage	V_{DOL}	UH,VH,WH,UL,VL,WL	0	0.14	0.60	V
Output high voltage	V_{DOH}	UH,VH,WH,UL,VL,WL	V_{REG} - 0.6	V_{REG} - 0.2	V_{REG}	V
Hall Element Amplifier Characteristics						
Common-mode input range	V_{HCM}	Using hall element	+0.5		V_{REG} - 0.5	V
Hall input sensitivity	V_{HSEN}			80		mV
HB output voltage	V_{HB}	I_{HB}= 10mA	4.5			V
I/O Interface						
Logic output low level	V_{OL}	FG, FAULT, RD		0	0.3	V
Logic output high level	V_{OH}	FG, FAULT, RD	4.0	4.5	5.5	V
Duty Control						
Duty minimum voltage***	V_{SPMIN}		0.3		2.1	V
Duty maximum voltage	V_{SPMAX}		3.0		5.4	V
PWM input clock****	F_{PWM_IN}	PWM input (VSP pin)		20		KHz

*Worked for internal VPP generation. For lower operation voltage requirement, feed the regulator voltage and VPP externally

**Current consumption is counted for the IC only. The connected Hall sensor will draw more current from the chip.
*** V_{PRTL}, V_{OCPH}, V_{OCPL}, V_{SPMIN}, V_{SPMAX} is adjustable with I^2C interface
****PWM input over VSP pin to work for 5V logic level

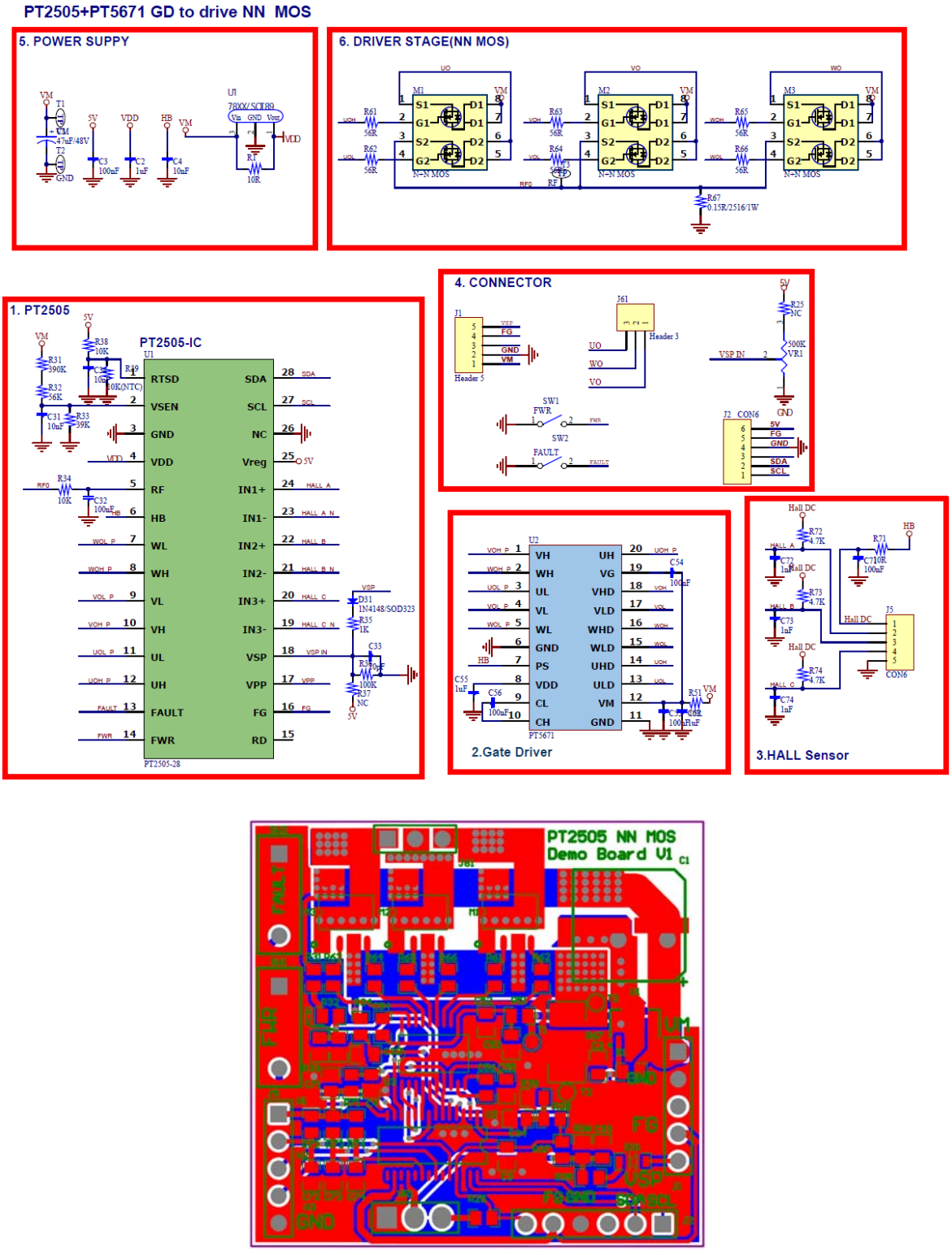
I^2C timing:



Parameter	Symbol	Min	Max	Unit
SCL clock frequency	f_{SCL}	0	50	KHz
Hold time START condition	$t_{HD;STA}$	4		µS
LOW period of the SCL clock	t_{LOW}	4.7		µS
HIGH period of the SCL clock	t_{HIGH}	4.0		µS
Data setup time	$t_{SU;DAT}$	250		nS
Data hold time	$t_{HD;DAT}$	5.0		µS
Setup time for STOP condition	$t_{SU;STO}$	4.0		µS

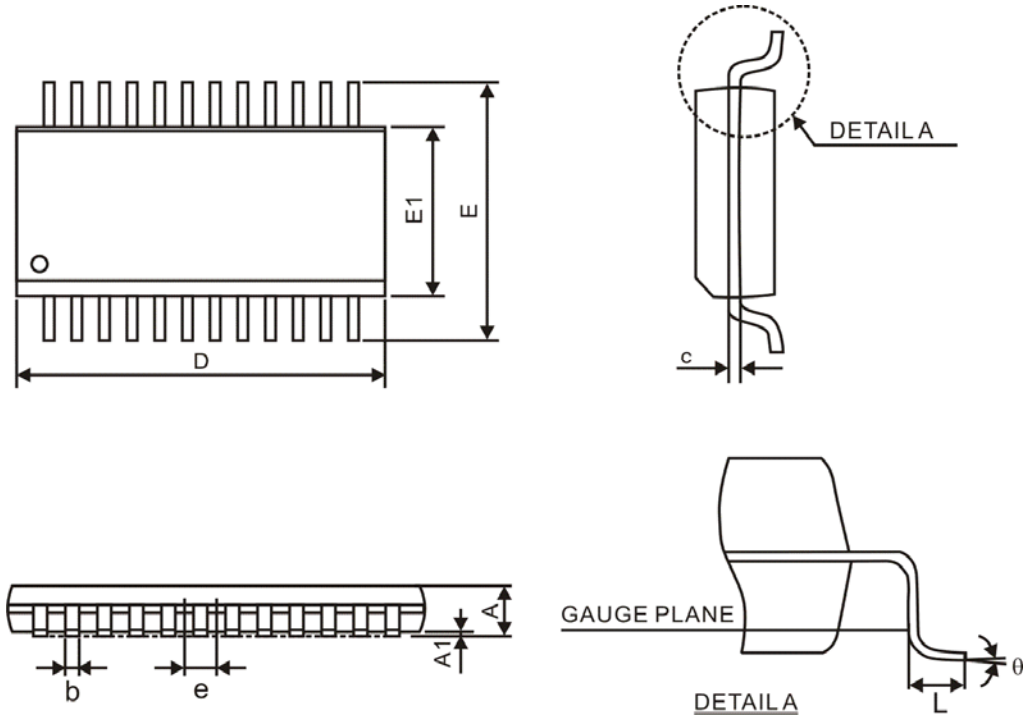
APPLICATION CIRCUIT

EVB with Gatedriver, Power MOS and Hall Sensor IC



PACKAGE INFORMATION

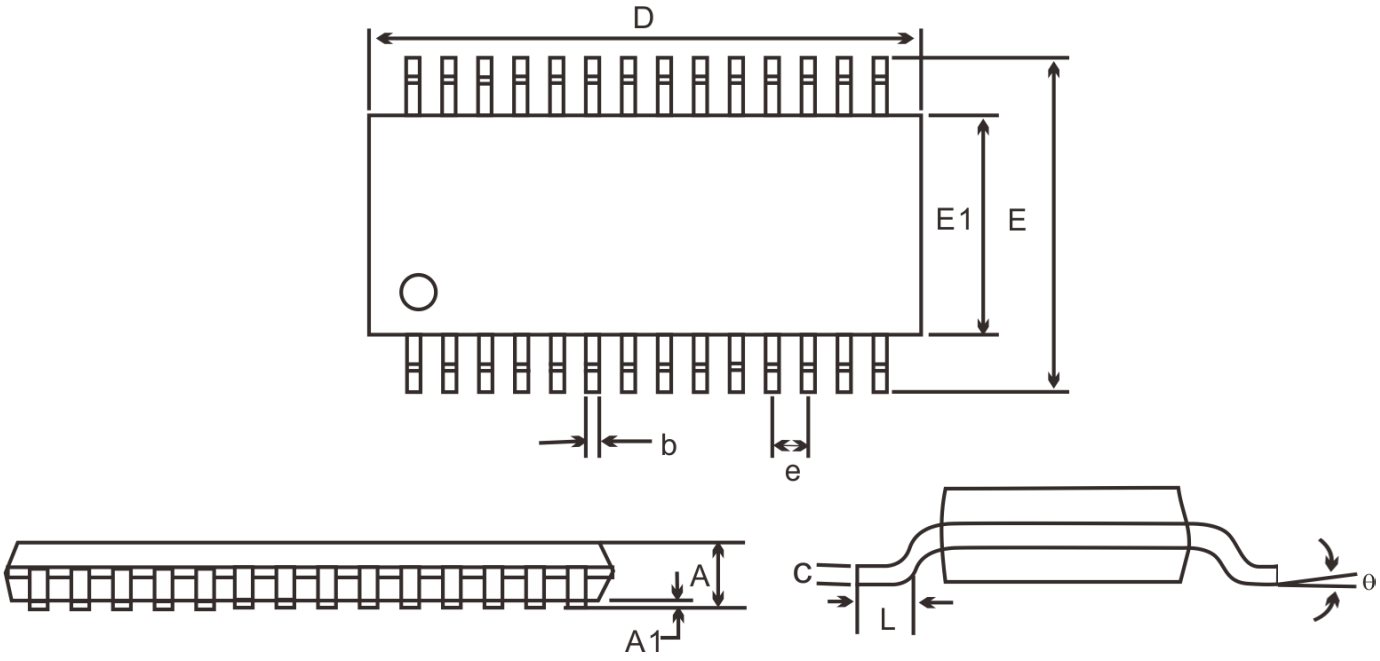
24 Pins, SSOP 150MIL



Symbol	Dimensions		
	Min.	Nom.	Max.
A	-	-	1.750
A1	0.100		0.250
b	0.20	-	0.30
c	0.10	-	0.25
e	0.635 BSC		
D	8.66 BSC		
E	5.99 BSC		
E1	3.91 BSC		
L	0.41	0.635	1.27
θ	0°	-	8°

Notes :
1. Refer to JEDEC MO-137 AE
2. Unit : mm

28 Pins, SSOP 150MIL



Symbol	Dimensions		
	Min.	Nom.	Max.
A	-	-	1.75
A1	0.10	-	0.25
b	0.20	-	0.30
c	0.10	-	0.25
e	0.635 BSC		
D	9.90 BSC		
E	5.99 BSC		
E1	3.91 BSC		
L	0.410	-	1.27
θ	0°	-	8°

Notes :
1. Refer to JEDEC MO-137 AF
2. Unit : mm

IMPORTANT NOTICE

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