普誠科技 Princeton Technology Corp.

DESCRIPTION

The PT2512 is an integrated three-phase sine wave current BLDC motor driver that is driven without Hall sensors. This driver has multiple protection functions, including over-current protection, over-temperature protection, lock protection, etc. PT2512 supports VSP(DC), PWM, Clock input command control. The motor parameters can be adjusted by using the capacitors or resistors on the peripheral pins of the IC to achieve the best performance control, and no software or program recording is required, which can shorten the development and production time. The small QFN16 or DFN10 3x3mm package with few peripheral components enables a compact PCB layout. The typical operating voltage of PT2512 is 5V and can provide a maximum driving current of about 1A, which is suitable for use in 1W ~ 5W motor applications.

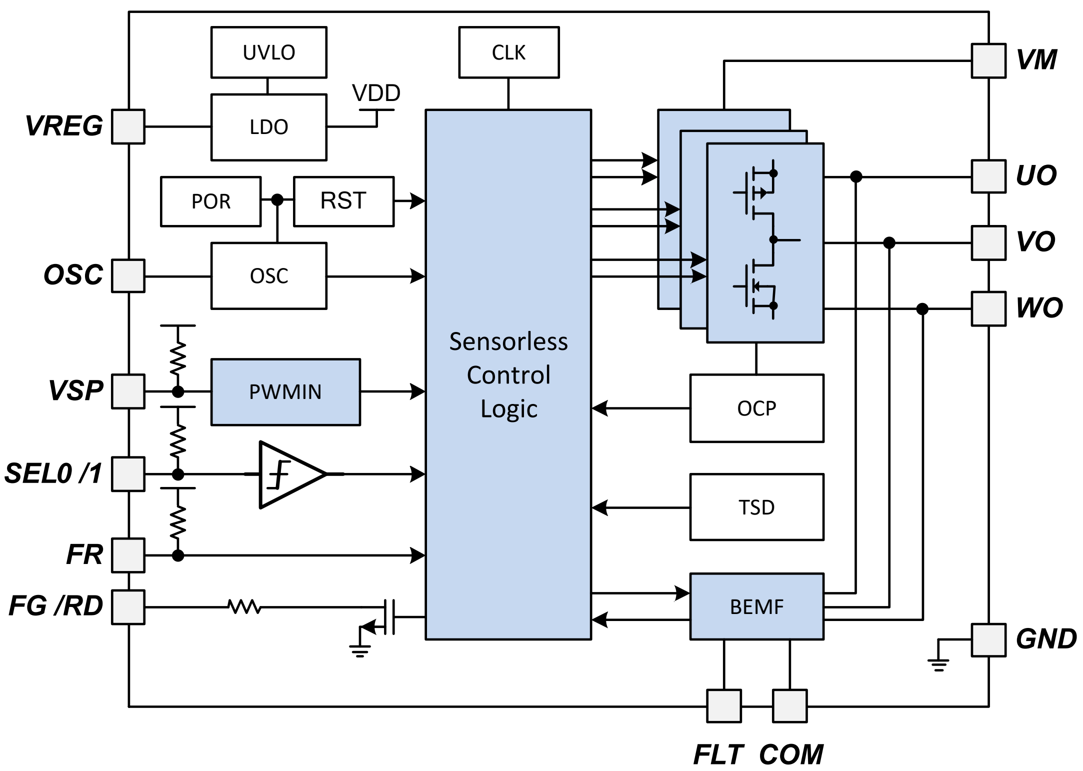
FEATURES

- Three-phase sensorless drive
- 2.2V ~ 8V operating voltage range
- 180° sinusoidal current for silent operation
- VSP, PWM input open loop control
- CLK input closed loop control
- Over current, over temperature & lock protection
- Open drain FG and RD(QFN16) output,
- FG, 1/2FG, 1/3FG speed out setting (QFN16)
- Forward and reverse FR input (QFN16)

APPLICATIONS

- Three-phase sensorless BLDC motor driver
- Cooling fans
- Water pump

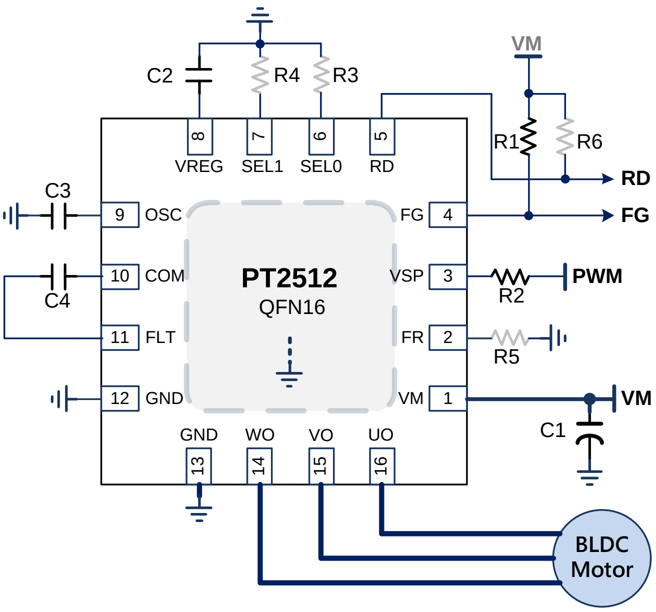
FUNCTION BLOCK

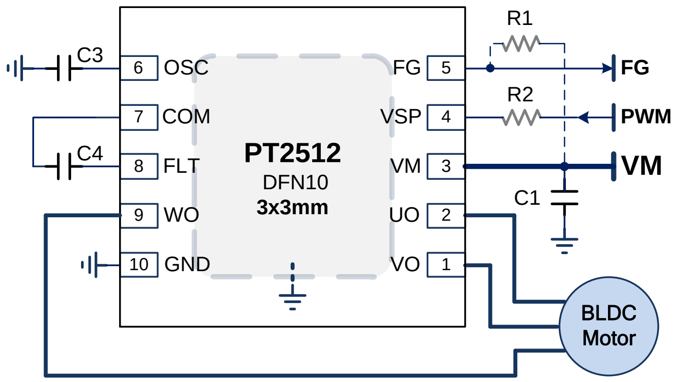


ORDER INFORMATION

Part Number	Package	Top Logo
PT2512	16-PIN, QFN	PT2512
PT2512	10-PIN, DFN	PT2512

APPLICATION CIRCUIT





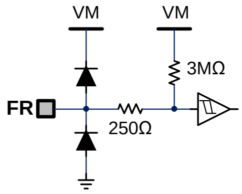
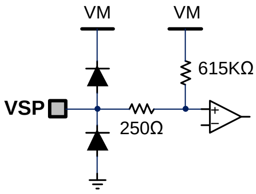
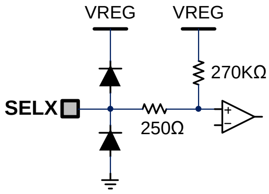
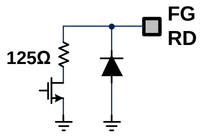
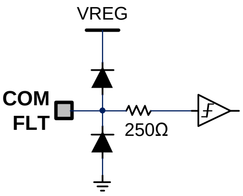
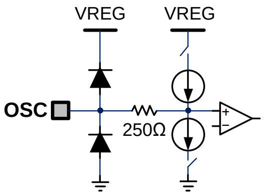
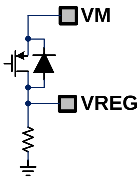
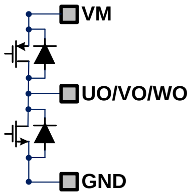
BOM FOR REFERENCE

Part	Value	Unit	Description
R1	10K	Ω	FG open drain pull high resistor (option)
R2	1K ~10K	Ω	VSP input protection resistor (option)
R3/R4	220K ~ 330K	Ω	SELx setting resistor (option)
R5	10K	Ω	FR 设定电组 (option)
R7	10K ~ 100K	Ω	RD open drain pull high resistor (option)
C1	10u ~47u	F	Power supply bypass capacitor
C2	10n	F	VREG input bypass capacitor
C3	100p ~ 10n	F	Startup step setting capacitor
C4	10p ~ 10n	F	ZC single process low pass filter capacitor

PIN NAME & DESCRIPTION

Pin Name	I/O	Description	Pin No.	
			QFN16	DFN10
VDD	P	Power supply input	1	3
FR	I	Forward and reverse setting, high (floating) for UVW CW ; low (connect to GND) for CCW rotation	2	-
VSP	I	Control input，allow VSP (DC) , PWM or Clock command	3	4
FG	O	FG output ; open drain structure, it can be set as FG or 1/2 FG or 1/3 FG output via SEL pin	4	5
RD	O	RD output；open drain structure	5	-
SEL0	I	SEL0 parameter setting, H, M, L tri-states	6	-
SEL1	I	SEL1 parameter setting, H, M, L tri-states	7	-
VREG	P	1.8V regulator, connect external bypass capacitor	8	-
OSC	I	External capacitor for startup and acc./deceleration settings	9	6
COM	I	Motor virtual common, BEMF comparison reference potential	10	7
FLT	I	BEMF signal filter input	11	8
GND	P	System grounding	12	10
GND	P	System grounding	13	-
WO	O	W output	14	9
VO	O	V output	15	1
UO	O	U output	16	2
Heat sink	P	Heat sink	back-side	Back-side

PIN EQUIVALENT CIRCUIT

FR	VSP	SEL0/1	FG/RD
			
COM/FLT	**OCP**	**VDD/VREG**	**UO/VO/WO**
			

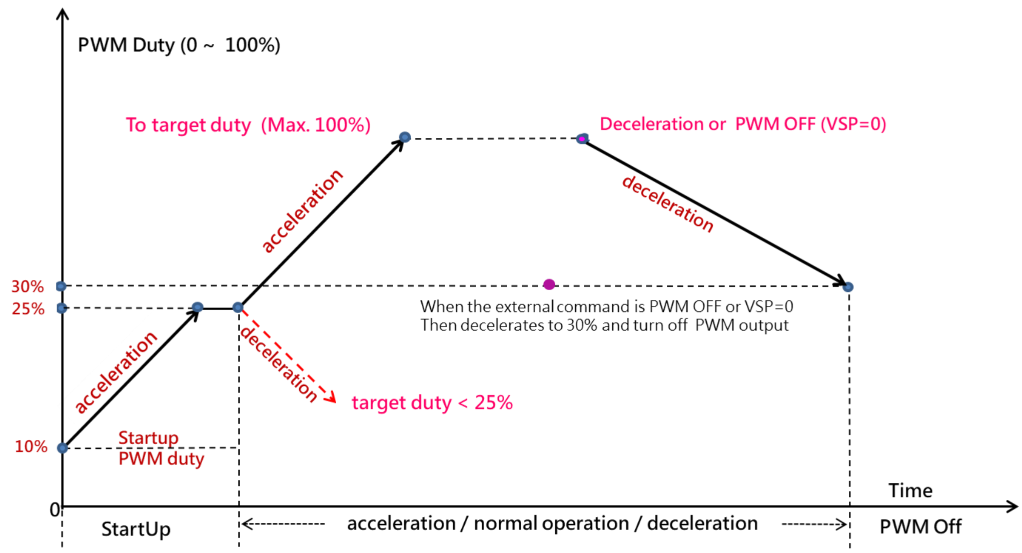
FUNCTION DESCRIPTION

Power supply

The PT2512 supports operation over a supply voltage range of 2.2V to 8V. VDD is the output stage MOS power supply and provides the internal voltage regulator VREG input voltage. VREG provides 1.8V for internal analog and digital circuits. Since the application side load is an induction motor coil, when the motor starts to rotate, a large current and voltage surge may be induced. Use appropriate bypass capacitors as close as possible to the VDD pin. The quiescent current (VSP = 0V or PWM = 0%) of PT2512 is less than 20uA when VDD is operated below 5.5V.

VSP input control

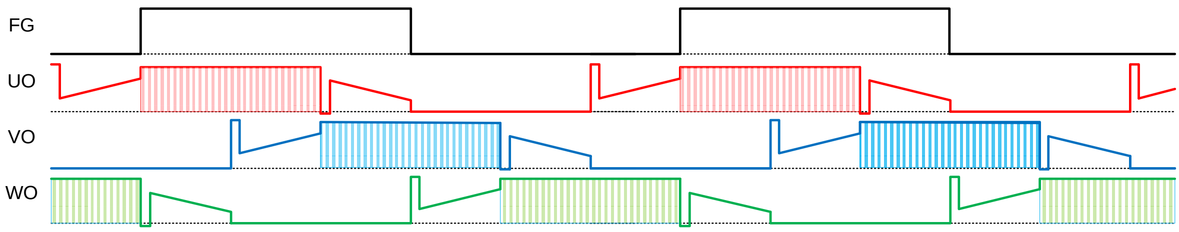
PT2512 can accept external VSP (DC voltage), PWM or CLK signal to adjust motor speed. When using PWM input, the high voltage potential needs to be greater than 1.8V; the low voltage potential needs to be less than 0.2V. The recommended PWM input frequency is between 5K and 50KHz. When using the VSP input, the voltage control range should be between 0.2V and 1.8V. When the VSP pin is not connected, it is weakly pulled high internally and the motor runs at full speed with 100% PWM duty cycle. The control program of VSP (PWM) will accelerate and decelerate according to the situation in the figure below.



In addition to using VSP or PWM for open-loop control, PT2512 can also perform speed closed-loop control. Using the CLK input, when the VSP input frequency is between 10Hz and 3KHz, the PT2512 will automatically perform speed closed-loop control. The U-phase commutation frequency is the same as the input CLK frequency, and the controllable range is 10Hz to 3KHz. This method can achieve more precise speed control.

Startup

For sensorless control, the most difficult part is the start-up process because the rotor position is unknown and the BEMF signal is weak or undetectable. The starting method of the PT2512 is initial alignment and a gradual increase in control voltage (or increase in PWM duty cycle) to achieve motor excitation and rotation. The initial alignment may cause the rotor to randomly rotate forward or backward one electrical cycle at startup. If the ZC signal is unclear, it will cause the motor to fail to start. If the motor does not start successfully within a certain period of time, the PT2512 will enter the lock protection mode and restart after a period of time. PT2512 adopts square wave PWM control mode during startup process, and there is a large BEMF detection interval at this time, which reduces the probability of startup failure, as shown in the figure below.



The startup process adopts 120° square wave PWM control mode

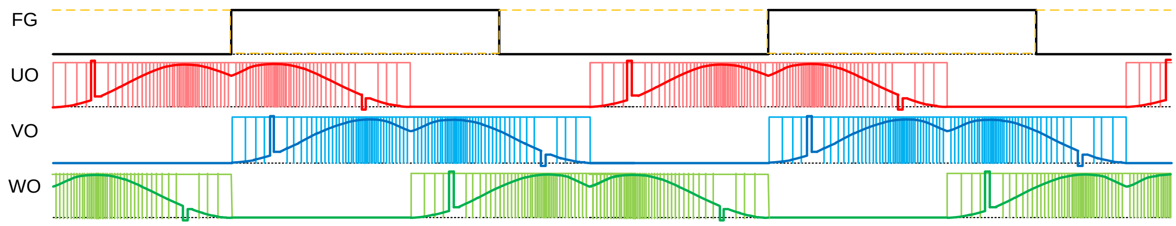
In order to adapt to the load requirements of different motors, the starting capacitor of the OSC pin can be adjusted to make the motor start smoothly. The range of OSC capacitance values is about 10pF~3.9nF. Lighter and faster motors generally require smaller capacitance values, and heavier and slower motors generally require larger capacitance values.

Sensorless control

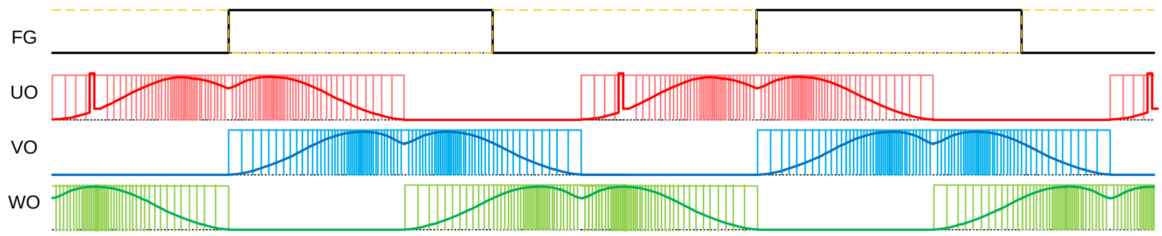
The PT2512 control scheme is based on a sensorless sinusoidal current waveform. Feedback for sensorless control is primarily achieved by measuring the induced electromotive force (BEMF) of the motor leads as the motor rotates. Sensorless control is achieved by using the U-phase to open a narrow window at the beginning of the commutation interval to detect the zero-crossing signal.

The PT2512 processes and generates the ZC signal for commutation detection through internal circuitry. Since factors such as different motors, operating voltages or loads can affect the ZC signal, an external ZC filter capacitor needs to be adjusted for optimal operation. The capacitance value range between "COM" and "FLT" is approximately 100pF to 10nF.

PT2512 (QFN16) can set the ZC opening mode through SEL0/1. When the PWM is less than 20%, because the BEMF is small or changes drastically, the PWM control mode of 6 Hi-Z windows will be forced to be used at this time.



Sensorless sine wave acceleration and deceleration process or PWM < 20%, using six Hi-Z windows to detect BEMF



Sensorless sine wave operation uses a U-phase Hi-Z window to detect BEMF

Current limit (OCL) and overcurrent protection (OCP)

The PT2512 implements over-current limit (OCL) and over-current protection (OCP) functions by detecting the peak current flowing through the motor coil. Under the application condition of 5V, the current limit (OCP) is about 1.0A (QFN16) or 0.8A (DFN10). At this time, if VSP/PWM/CLK is increased, the motor will no longer speed up. When the peak current exceeds 1.5A, the overcurrent protection (OCP) will be triggered, and the system will enter the locked protection mode.

Lock Protection

The PT2512 has four conditions that cause the control algorithm to enter lock protection mode. First, the controller cannot determine any correct commutation signals when the motor is in the start-up phase. Second, when the motor starts successfully and is in run mode, but the ZC signal suddenly changes too much. Third, when the motor current is too large to trigger the OCP potential. Fourth, when the speed is too high. At this point the motor will immediately stop and the output driver stage will be switched off. After a few seconds, the control algorithm will try to restart the motor. If the motor starts successfully, it will continue to operate normally. However, if the motor still fails to start, the control algorithm will return to lock protection mode and try to restart again after a few seconds.

Over temperature protection (OTP)

PT2512 has built-in temperature detection circuit. When the internal temperature exceeds 150°C, the PT2512 will shut down the output driver stage. When the internal temperature drops below 120°C, the PT2512 will restart again and operate normally.

FG and RD output setting

PT2512 provides FG and RD output to monitor motor speed and faults. When the rotor runs for one (electrical) cycle, the FG pin will output a high and a low. The number of rotor poles needs to be known when calculating the rotational speed. For example, if the rotor has 8 poles (four pairs of NS), one cycle of the motor will produce 4 FG outputs. Generally, the motor speed is in RPM (revolutions per minute), and the conversion formula between the speed (RPM) and the FG frequency (Hz) is as follows:

$$RPM = FG \times 120 / POLE,$$

Where FG is the frequency in Hz; POLE is the number of stages of the motor rotor (N and S are one pole each).

When PT2512 starts to output PWM, it detects BEMF signal and starts to output FG. When PWM stops output, FG will stop output regardless of whether the motor is rotating or not. The position of the FG trigger is about 90 degrees behind the U-phase commutation point, and the starting point may be the rising edge or the falling edge.

The FG or RD output pin is an open drain structure, and the highest pull-up power supply can be up to VDD. In addition, PT2512 (QFN16) also provides 1/2FG or 1/3FG frequency output. Please refer to SEL pin setting.

RD is an indicator of an abnormality occurs. When locked protection, over-temperature protection or over-current protection occurs, RD will pull the external pull-high resistor to a low potential.

Forward and reverse setting

The PT2512 (QFN16) can be set to forward or reverse mode through the FR pin. UVW CW when FR=5V or high, CCW operation when FR=0V or low. The FR mode can be changed directly during operation. There is a pull-up resistor inside the FR pin, which can be left empty when forward and reverse switching is not required. The forward and reverse settings can also be changed by swapping the motor wiring when the PT2512 is in sensorless control mode.

Capacitor value selection between COM and FLT pins

The PT2512 detects the motor position by comparing the back EMF generated by the motor rotation with the virtual midpoint voltage, thereby generating the ZC signal. However, noise from motor startup or rotation may interfere with the accuracy of the zero-crossing signal, which may cause startup failure or affect rotational stability. Capacitors between the COM and FLT pins help reduce noise. The recommended capacitance range is 10pF to 3.3nF.

The RC filter circuit will cause ZC to be delayed. Usually the higher the speed of the motor, the smaller the capacitance value, so that the efficiency will not be affected by too much delay. When FLT_C=1nF, it can be applied to the motor whose maximum speed FG is about 100Hz. For other applications with different maximum rpm, this value can be used as an initial setting and then fine-tuned for more stable and efficient results. Generally, the higher the motor speed and the higher the frequency, the smaller the FLT capacitor can be, and vice versa.

Capacitor value selection for OSC pin

OSC is the relative benchmark for all variable adjustment steps or times of the PT2512, including start-up steps, acceleration and deceleration times. When OSC_C=1nF and OSC~1KHz, it is also suitable for applications where FG is about 100Hz at the highest speed of the motor. Other applications with different maximum speeds can be equivalent to OSC_C=1nF, FG=100Hz as the initial setting value, and then fine-tune to achieve a smoother startup effect. Typically higher speed or faster startup applications choose a smaller OSC capacitor and vice versa.

One of the conditions for PT2512 to trigger the lock protection is that the too high rotation speed. The set value of the maximum speed is relative with the OSC. The smaller OSC capacitor value, the higher allowable speed is limited. For example, when OSC_C=1nF, OSC is about 1KHz and the allowable FG is around 100Hz.

SEL0 & SEL1 setting

PT2512 can set different application requirements through SEL0 & SEL1, such as PWM modulation waveform, FG output, etc. Its settings are divided into 3 configurations. When the pin is floating, the SEL is about 1.8V, and SEL=H; when the pin is connected to a 270KΩ resistor, the SEL is about 0.9V, and SEL=M; when the pin is shorted to ground, the SEL is about 0V, and SEL=L. The following table is the adjustment content:

(SEL0 , SEL1)	PWM Switching	PWM Change	When PWM<10%	When FR Change	FG out	RD out	Lock on	Max Speed
(H , H)	Sinewave Hi-Z 9°	smooth	= 10%	BRK + waiting	FG	RD	5sec	by OSC
(H ,M)	Sinewave Hi-Z 9°	smooth	= 10%	BRK + waiting	1/2FG	RD	5sec	by OSC
(H , L)	Sinewave Hi-Z 9°	smooth	= 10%	BRK + waiting	1/3FG	RD	5sec	by OSC

(L , H)	Sinewave Hi-Z 15°	smooth	= 10%	BRK + waiting	FG	RD	5sec	by OSC
(L , M)	Sinewave Hi-Z 15°	smooth	= 10%	BRK + waiting	1/2FG	RD	5sec	by OSC
(L , L)	Sinewave Hi-Z 15°	smooth	= 10%	BRK + waiting	1/3FG	RD	5sec	by OSC
(M , H)	Squarewave	smooth	= 10%	BRK + waiting	FG	RD	5sec	by OSC
(M , M)	Squarewave	w/o smooth	= PWM in	No waiting	FG	Fault	disable	NA
(M , L)	Squarewave	w/o smooth	= PWM in	No waiting	FG	RD	5sec	by OSC

Note : DFN10 package，SEL0/SEL1 default (H, H)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Max.	Unit
VDD supply voltage	VDDmax	PT2512 no break down	9	V
Output pin current(1)	Iout,max	QFN16 UO, VO, WO pins	1.0	A
		DFN10 UO, VO, WO pins	0.8	A
Input pin withstand voltage	Vin,max	VSP, FR	6	V
		SELx	VREG	V
Open Drain withstand voltage	Vopen,max	FG, RD	9	V
Power dissipation 1	Pd,max1	IC only	0.3	W
Power dissipation 2	Pd,max2	IC assembled on the test board (2)	0.9	W
External ambient temperature	Ta	TSD is not triggered	–40 to+105	°C
Core operating temperature	Tj	TSD is not triggered	–40 to+150	°C
Storage temperature	Ts	–	–40 to +150	°C

Notes: 1. 500ms of test time and installed in designated areas with heat sinks
2. Mounted on a board with a heat sink.

ELECTRICAL CHARACTERISTICS

(Standard conditions : VDD = 5V, T = 25℃)

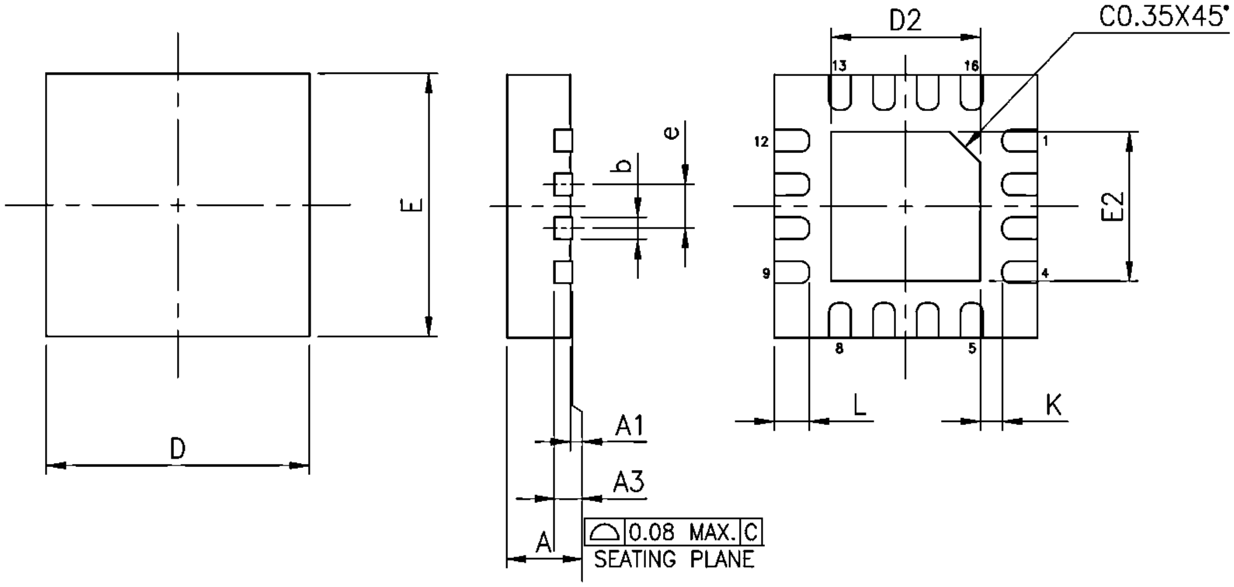
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
VDD supply voltage	VDD	PT2512	2.2	5	8	V
VDD consumption current	IDD	VSP = VDD, motor wires disconnected	–	2.5	4.0	mA
MOS stage resistance	Rdson	Io = 500mA, (H+L)	–	0.8	–	Ω
MOS switching frequency	Fmos	U, V, W output,	30	40	50	kHz
OSC charge/discharge current	Iosc	OSC pin	–	3.4	–	μA
VREG pin voltage	Vreg	No external load	1.6	1.8	2.0	V
VSP DC control range (Note)	DCvsp	VSP input	0	–	VREG	V
VSP PWM input frequency	Fpwm	VSP input	5	–	25	kHz
VSP CLK input frequency	Fclk	VSP input	10	–	3000	Hz

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
VSP PWM/CLK input high threshold	Vpwmh	VSP input , PWM/CLK voltage rising	1.0	–	VDD	V
VSP PWM/CLK input low threshold	Vpwml	VSP input PWM/CLK voltage falling	0	–	0.3	V
FG output low	Vfgl	IFG=1mA	–	0.1	–	V
FG output leakage current	Ifgl	VFG=9V	–	–	1	μA
Logic input pull high current	Isource	FR pin	–	5	–	μA
Logic input pull high resistance	Rselx	SELx pins	220K	270K	330K	Ω
Lock protection release time	Tlock	SEL≠ (M, M) setting	–	5.0	–	S
Thermal shunt down	Tshdn	Temperature increasing, design target	–	150	–	°C
TSD release	Trel	Temperature decreasing, design target	–	120	–	°C

Note : When PWM input, the allowable minimum PWM duty = 3%, when VSP(DC) input, the allowable minimum startup voltage is about 0.3V. If the PWM/VSP is too small, it may fail to start. When the voltage exceeds 1.8V, it will run at 100% PWM duty.

PACKAGE INFORMATION

16 Pins, QFN 3x3mm

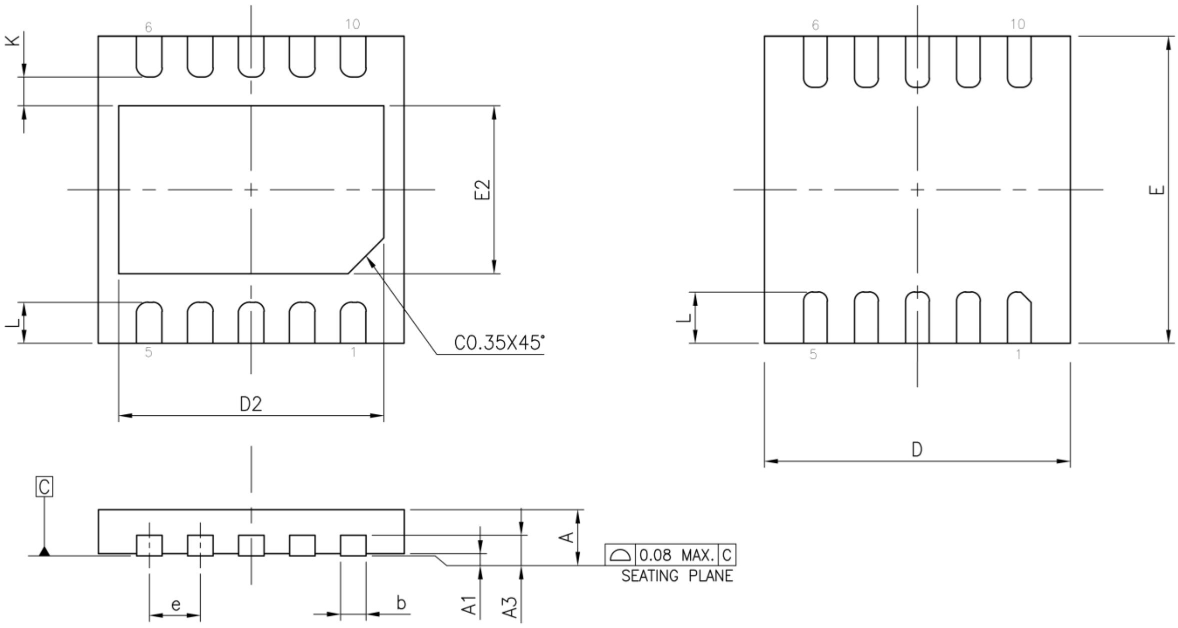


Symbol	Dimension (mm)		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20 REF.		
b	0.18	0.25	0.30
D	3.00 BSC		
E	3.00 BSC		
e	0.50 BSC		
K	0.20	-	-
E2	1.60	1.70	1.75
D2	1.60	1.70	1.75
L	0.30	0.35	0.40

Notes:

1. Unit : mm

10 Pins, DFN 3x3x0.55mm



Symbol	Dimension (mm)		
	Min.	典型	Min.
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A3	0.150 REF.		
b	0.18	0.25	0.30
D	3.00 BSC		
E	3.00 BSC		
e	0.50 BSC		
K	0.20	-	-
L	0.30	0.40	0.50
D2	2.20	2.30	2.35
E2	1.55	1.60	1.65

Notes:

1. Unit : mm

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