

DESCRIPTION

PT2522 is a combination of PT2502 and PT5619. It is a three-phase, sensor-less brushless DC motor control driver chip. The three-phase control is a square wave/trapezoidal wave control method based on detecting the zero-crossing of the motor back electromotive force (BEMF). It has a stable control effect and is not easily affected by motor differences. The chip's soft switching technology can achieve trapezoidal wave or sine wave like current waveform, further reducing the phase electromagnetic noise. The built-in +5V LDO of the chip provides the operation of the logic circuit and the analog circuit. Three 90V half-bridge gate drivers are integrated at the same chip, which is particularly suitable for gate drive of high-speed power MOSFETs in three-phase motor applications. PT2522 provides to change the internal parameter settings by burning to optimize different motors and applications. The package of PT2522 is LQFP32.

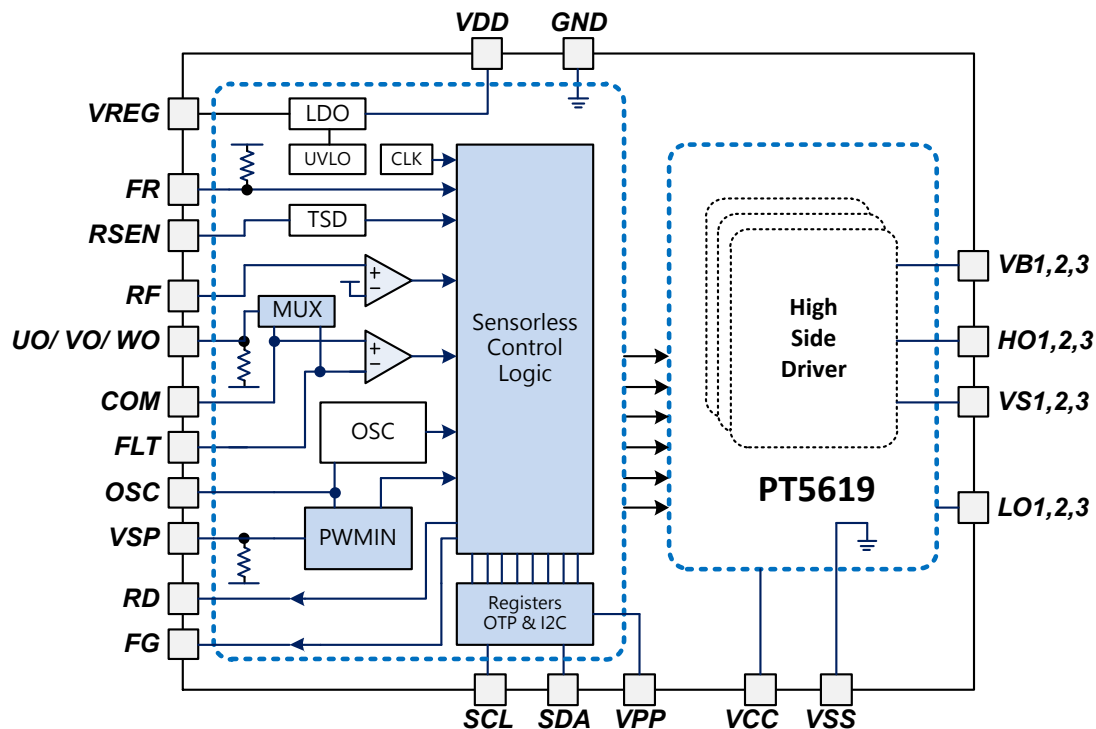
FEATURES

- Sensor-less three-phase brushless DC motor control driver chip
- Integrated three 90V half-bridge gate drivers
- Driver pull-out/inrush current: 1.2A / 2.0A
- Built-in +5V LDO (power input below VDD 24V)
- OTP (one time programming) for motor parameters
- Set OTP parameters through I2C
- Current limit and lock protection
- Temperature protection function (using external NTC resistor)
- VSP (DC), PWM or Clock input for speed control
- FG, RD indicator signal output

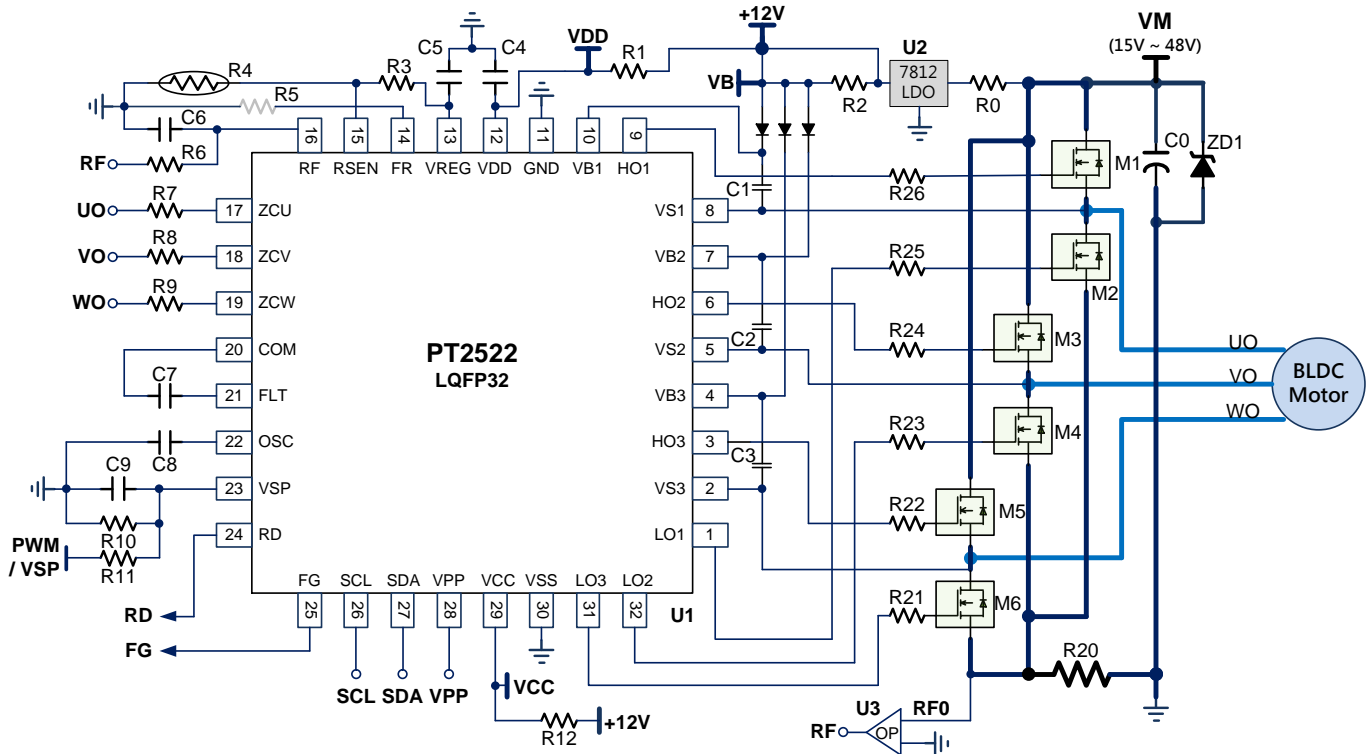
APPLICATION

- Three-phase DC brushless motor below 48V
- Power tools and handheld vacuum cleaner
- Water pump application

BLOCK DIAGRAM



APPLICATION CIRCUIT

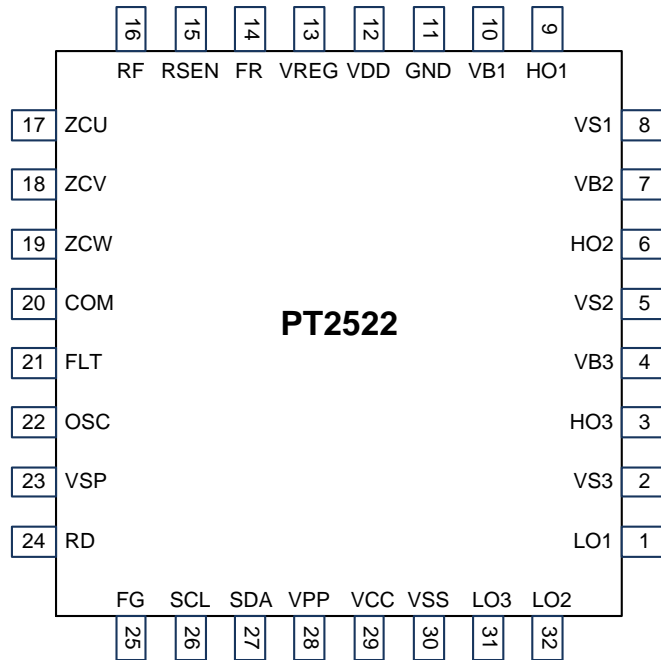


BOM FOR APPLICATION CIRCUIT

Parts	Function Value	Unit Side	Description
U1	Controller	LQFP32	PT2522 (PT2502 + PT5619)
U2	LDO	SOT89 TO251	7812 LDO, convert VM to 12V, please pay attention to component input withstand voltage If the input withstand voltage is insufficient, please change to another LDO or DC/DC substitute LDO peripheral circuit is not included in the application circuit
U3	OP AMP	SOT25	Current detection amplification is used, if the current limit is relatively small or the comparison voltage is relatively high, OP AMP may not be used, RF0 = RF OP AMP peripheral circuit is not included in the application circuit
VM	15 ~ 48	V	Current detection amplification is used, if the current limit is relatively small or the comparison voltage is relatively high, OP AMP may not be used, RF0 = RF OP AMP peripheral circuit is not included in the application circuit
VCC	6V ~ 15V	V	Gate driver internal and low side Vg power supply
VB	6V ~ 15V	V	Gate driver high side Vg power supply
VDD	6V ~ 15V	V	Controller (PT2502) input power supply

VREG	5V / 20mA	V	Controller internal LDO
M1 ~ M6	20V ~ 200V	V	NMOS, Please select the appropriate specifications according to application needs. It is recommended that the withstand voltage is higher than 2 times the motor power supply voltage (VM)
R0	0~100	Ω	Noise isolation resistance for controller power supply, to reduce the interference from the motor switching. When the VM voltage is higher, the larger package resistance can be used to disperse the heat generated by the LDO voltage drop
R1	0~100	Ω	VDD input bypass resistance
R2	10~100	Ω	VB input current limit resistance
R3	>10K	Ω	Over temperature protection voltage divider resistance
R4	NTC	Ω	Over temperature protection detection resistance, negative temperature coefficient characteristics
R5	0~10K	Ω	Forward and reverse switching, 0V/5V logic voltage, keep floating when not used
R6	1K ~ 100K	Ω	Current limit signal input filter resistance
R7 ~ R9	22K ~ 47K	Ω	BEMF detection divide resistance
R10	10K ~ 100K	Ω	VSP/PWM input pull low resistance
R11	1K ~ 10K	Ω	VSP/PWM input filter resistance
R12	0 ~ 100	Ω	VCC input bypass resistance
R20	0.01 ~ 1	Ω	The current limit detection resistor needs to use a higher power resistor according to the demand to avoid overheating and burning. Another way is to use a smaller value resistor and then use OP AMP to amplify the voltage.
R21 ~ R26	10 ~ 200	Ω	The Rg resistance at the gate affects the switching speed and EMI of the MOSFET. Diodes can be connected in parallel to shorten the turn-off time of MOSFET
C0	1u ~	F	Motor power supply terminal (VM) bypass capacitor. It is recommended to use electrolytic capacitors with a withstand voltage of more than 2 times. Small capacitors (~ 100n) can be connected in parallel to filter high frequency PWM noise.
C1 ~ C3	100n ~ 10u	F	Bootstrap capacitor provides high side power supply. It is recommended to use a withstand voltage above 20V and a low ESR capacitor to avoid insufficient voltage due to limited charging and discharging capabilities
C4	100n ~ 1u	F	VDD bypass capacitance
C5	100n	F	VREG bypass capacitance
C6	100p ~ 100n	F	Current limit signal input filter capacitance
C7	10p ~ 10n	F	ZC detection filter capacitance
C8	10p ~ 10n	F	Triangle wave generator capacitor
C9	1n ~ 100n	F	VSP input filter capacitance
ZD1	15 ~ 18	V	Zener diode, prevent excessive back EMF or voltage surge

PIN CONFIGURATION



PIN DESCRIPTION

Pin Name	I / O / P	Description	Pin No.
LO1	I/O	Phase 1 low side gate driver output	1
VS3	P	Phase 3 high side driver floating power supply swing voltage	2
HO3	I/O	Phase 3 high side driver output	3
VB3	P	Phase 3 high side driver floating power supply	4
VS2	P	Phase 2 high side driver floating power supply swing voltage	5
HO2	I/O	Phase 2 high side driver output	6
VB2	P	Phase 2 high side driver floating power supply	7
VS1	P	Phase 1 high side driver floating power supply swing voltage	8
HO1	I/O	Phase 1 high side driver output	9
VB1	P	Phase 1 high side driver floating power supply	10
GND	P	Signal ground	11
VDD	P	Voltage input	12
VREG	P	+5V voltage output	13
FWR	I	Positive and negative switching	14
RSEN	I	External NTC resistor can be connected as over temperature protection	15
RF	I	Current limiting voltage sensing	16
ZCU	I	U opposite electromotive zero-crossing input	17

ZCV	I	V opposite electromotive zero-crossing input	18
ZCW	I	W reverse electric zero-crossing input	19
COM	I	Motor three-phase virtual neutral point	20
FLT	I	Six-step commutation signal filter input	21
OSC	IO	Connect an external capacitor as a triangular wave for PWM comparison	22
VSP	I	DC or PWM input speed control	23
RD	O	Stall protection indication output (5V CMOS logic)	24
FG	O	Speed indicator output (5V CMOS logic)	25
SCL	I	I2C Control Interface – Serial Frequency (Clock) Input	26
SDA	I/O	I2C Control Interface – Serial Data Input/Output	27
VPP	P	OTP Burning Power Input (7.5V)	28
VCC	P	Internal logic circuit and low side gate driver power input	29
VSS	P	Internal logic circuit and low side gate driver power ground	30
LO3	I/O	Phase 3 low side gate driver output	31
LO2	I/O	Phase 2 low side gate driver output	32

ORDER INFORMATION

Part Number	Package	Top Logo
PT2522-LQ	32 Pins, LQFP	PT2522-LQ
PT2522	32-PIN, QFN	PT2522

FUNCTION DESCRIPTION

POWER SUPPLY

PT2522 is packaged by PT2502 and PT5619, there are several different power requirements inside. According to different input voltage ranges, there are some different voltage arrangements as below.

When the motor power supply $V_M < 15V$, V_M can provide VDD and VCC power supply through simple filtering.

When the motor power supply V_M is between $15V \sim 24V$, it is recommended to use an external step-down IC (such as 7812) to reduce the voltage to 12V, and then supply the VDD and VCC power supply.

When the motor power supply V_M is higher than 24V, it is suggested use a DC/DC IC to reduce the voltage to 12V, and then supply VDD and VCC power.

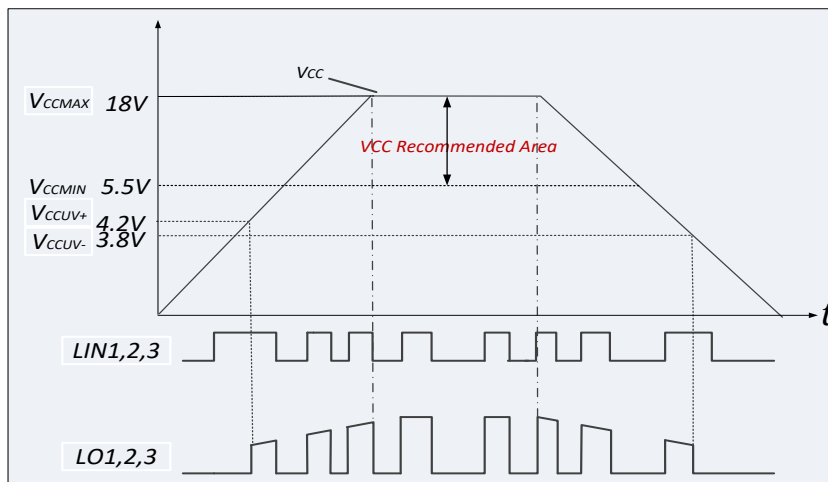
PT2522 has built-in a 5V LDO to supply controller circuits. When the LDO voltage exceeds 3.5V, the logic circuit will wake up to operation within 10ms. In motor systems, there is a noisy environment. It is recommended to place the bypass capacitor as close to the IC power pin as possible.

V_M recommends connecting larger electrolytic capacitors and Zener diodes in parallel. In addition to stabilizing the power supply voltage, it can also absorb part of the regenerative voltage generated when the motor decelerates.

PT2522 cancels the low-voltage and over-voltage protection functions of the original PT2502 due to pin limitation. The gate driver part retains the UVLO function of VBS and VCC, and its function is explained as follows.

GATE DRIVER LOW-SIDE POWER SUPPLY VCC AND UVLO

VCC is the power supply terminal of the low-side circuit, which can provide the required driving energy for the operation of the input logic circuit and the low-side output power stage. The built-in under-voltage lockout circuit can ensure that the chip works in a sufficiently supply voltage range, thereby preventing damage to the MOSFET due to heat dissipation caused by the low driving voltage. As below figure, when VCC rises and exceeds the threshold voltage $V_{CCUV+} = 4.2V$, the low-side control circuit is unlocked and starts to work, and LO starts to output; on the contrary, when VCC falls and falls below the threshold voltage $V_{CCUV-} = 3.8V$, the low-side control circuit The circuit is locked, the chip stops working, and the LO stops output. The recommended working voltage range of VCC is 6V-18V.

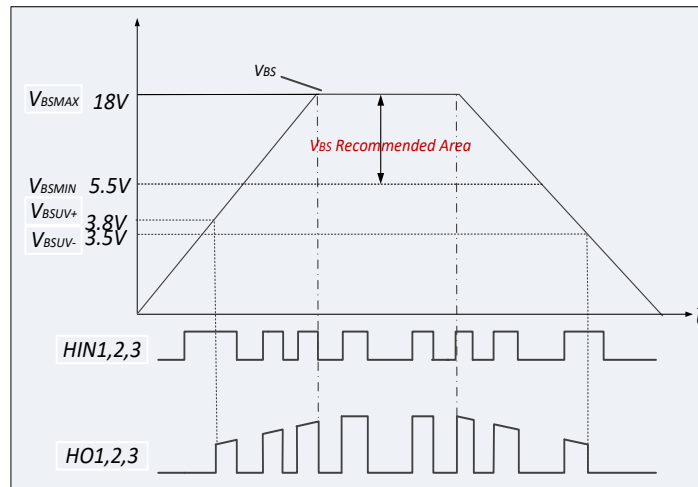


VCC supply and its UVLO operation area

GATE DRIVER HIGH-SIDE POWER SUPPLY VBS AND UVLO

The VBS power supply is the power supply for the high-side circuit, where VBS (VB1,2,3-VS1,2,3) corresponds to the

three-phase high-side drive power supply. The overall high-side circuit powered by the floating power supply VBS takes VS1,2,3 as the reference point, and follows the source/emitter voltage of the external power MOSFET, swinging between the ground and bus voltages. Because the high-side circuit has low quiescent current consumption, the entire high-side circuit is supplied by the bootstrap diode connected to VCC, and only a small capacitor can maintain the voltage required to drive the power tube. As shown in the figure below, the under-voltage lockout of the high-side power supply VBS is similar to the low-side VCC power supply, and the recommended working voltage range of VBS is 6V-18V.

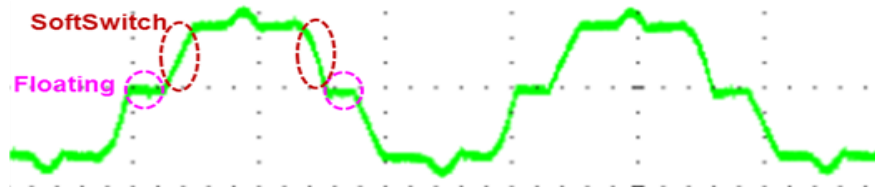


VBS1,2,3 supply and its UVLO operation area

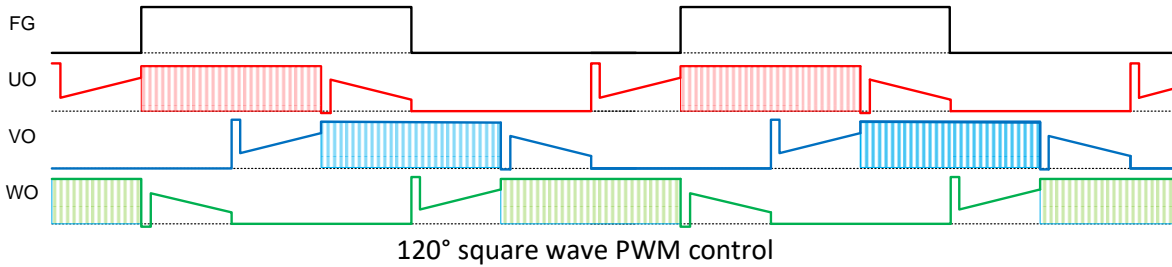
SENSOR-LESS CONTROL

The PT2522 control scheme is based on sensorless trapezoidal wave control. The main advantage is that there is no need for a Hall sensor, thereby reducing the cost of the module and the problem of temperature changes. The feedback of sensorless control is mainly realized by measuring the BEMF induced by the motor coil when the motor is rotating. When the motor is controlled, the UVW coil terminal voltage (phase voltage) mixes the control signal and BEMF, making it difficult to separate the back EMF from the phase voltage. When using motor commutation, floating the motor for a period of time (a specific angle) is a way to obtain the back-EMF signal. In general, the angle of the floating electrical appliance is 60° in pure square wave control, which is generally called 120° commutation control. The angle of the floating electrical appliance is 30° to 60° under trapezoidal wave control. Generally, when the angle of 30° of floating electrical appliances is used, there is also a commutation control called 150°. PT2522 can choose to use square wave or trapezoidal wave through parameter setting, and can also set the opening width of different BEMF detection.

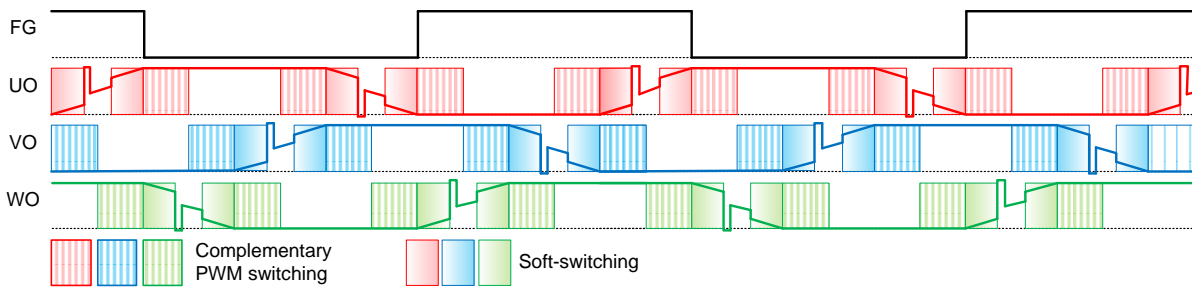
PT2522 reduces the phase voltage below 5V by using a voltage divider resistor (there is a 10K floor resistance inside), allowing analog circuits to process the signal and generate a zero-crossing (ZC) signal to sense UVW commutation. Because of the motor, working voltage, speed and other factors, the system noise is too large or the motor's BEMF signal is too weak, which will affect the accuracy of the ZC signal, and this may cause control failures. You can adjust the analog filter (external capacitor) or digital filter (Internal parameters) to improve. PT2522 adopts soft switching mode to help reduce audible motor current noise.



PT2522 commutation current wave pattern example



120° square wave PWM control



150° trapezoidal wave control, FG & phase voltage relation

CAPACITANCE SELECTION BETWEEN COM AND FLT PINS

The PT2522 detects the motor position by comparing the back electromotive force generated by the motor rotation with the 3-phase virtual midpoint voltage to generate a ZC signal. However, noise from the start or rotation of the motor may interfere with the accuracy of the zero-crossing signal and may result in failure at startup or reduced motor efficiency. Capacitors between the COM and FLT pins help mitigate the effects of noise interference. The recommended range of capacitance values is 0.1nF to 10nF, because the filter capacitor also affects the judgment of the commutation delay. Therefore, the smaller the motor capacitor value, the higher the speed, the less the delay will affect. Alternatively, it also can set a digital filter by parameters. Whether digital or analog filters cause delays, the PT2522 can compensate for various delays through parameters, allowing the motor to maintain efficient operation.

CURRENT LIMIT

The PT2522 uses a sense resistor to obtain a current-limiting function (at the RF pin) that is related to the relative phase current. When the detected RF voltage exceeds 0.3V, you can choose to reduce the PWM duty or turn off the PWM operation mode. RF resistors require high-power precision resistors to avoid burnout due to overheating. When the RF resistor is burned, it will cause an open circuit, which may cause extensive damage to components such as the controller, Gate Driver, and MOSFET.

OVER TEMPERATURE PROTECTION

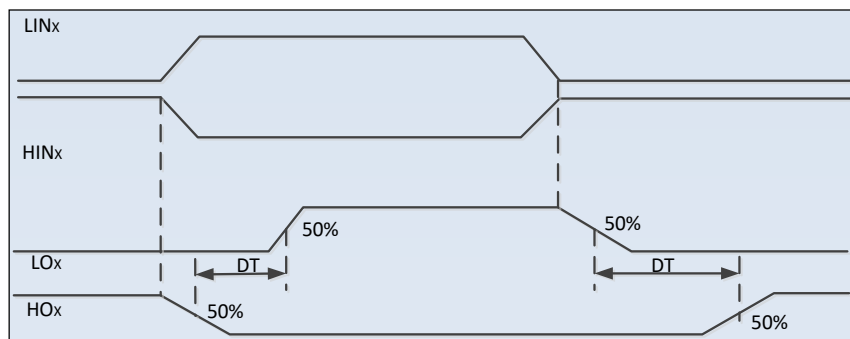
PT2522 uses an external negative temperature coefficient resistor (NTC) as the source of the over-temperature protection detector. In the RSEN pin, the resistor will be connected to 5V, and the NTC resistor will be connected to ground. The NTC resistor should be placed near the protected target (such as MOSFET). If the temperature rises, the NTC resistance value will decrease, and the voltage level of the RESE pin will decrease also. When the RSEN voltage is lower than 0.6V, the PT2522 enters the over-temperature protection (OTP) mode, pulls the RD pin to a high level, and the system enters the shutdown mode. After the temperature is lower, the voltage of the RSEN pin is higher than 1.2V, and the motor system will start again. In the shutdown mode of PT2522, Gate Driver will turn off the output.

MOTOR LOCK OUT PROTECTION

During the startup process, when the controller cannot determine any valid ZC signal, it will make the motor enter the locked-rotor protection mode. If external force intervenes or interferes during the operation of the motor, resulting in excessive ZC variation, it will also force the motor to enter the locked-rotor protection mode. After a period, the controller will try to restart the motor. After the motor restarts successfully, normal operation will continue. However, if the motor still fails to start, the control algorithm will continue to return to the locked-rotor protection mode and try to restart the motor again. If the continuous startup fails to reach the dead lock condition, it will enter the shutdown protection mode, and it will release after power-on again. PT2522 can use parameters to set the conditions for entering and leaving the locked rotor. When entering the locked rotor protection mode, the RD pin will output a high level.

GATE DRIVER DEAD TIME PROTECTION

In addition to the dead time that can set by the controller part, the Gate Driver part is equipped with a fixed dead time protection circuit. During the dead time, both the high-side and low-side driver outputs are set to "low". The set dead time must ensure that one power device effectively turn off before to turn on the other power device to prevent the phenomenon that the upper and lower MOSFETs are directly connected. When the dead time of the external logic input is different from the internal fixed dead time, the longer time will be taken. The following figure describes the timing relationship between dead time, input signal and driver output.

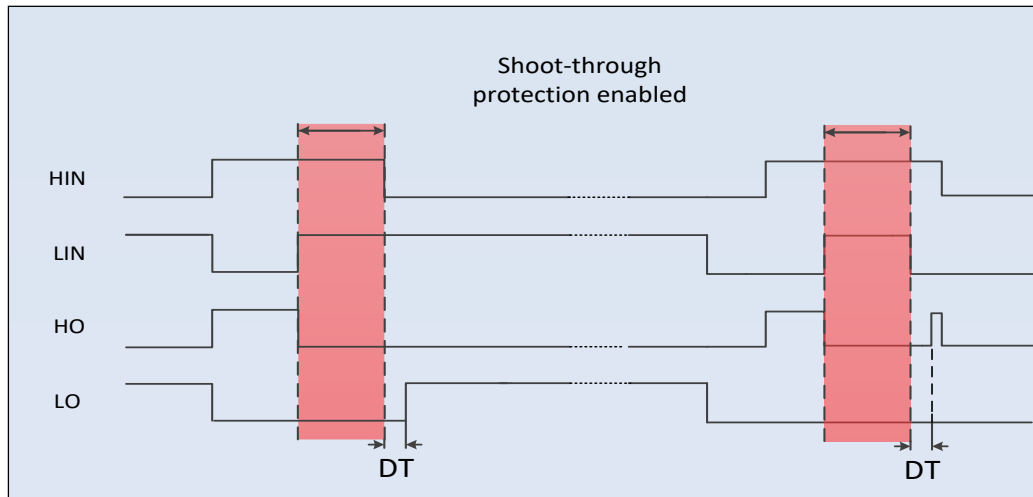


Gate driver dead time protection diagram

MOSFET SHOOT THROUGH PROTECTION

The chip is equipped with a protection circuit specially used to prevent the power tube from passing through, which can effectively prevent the power tube damage caused by the common mode interference of the high-side and low-side input signals. Below figure shows how the shoot-through protection circuit protects the power stage. The power stage shoot-through means that the high-side gate driver output HO and the low-side gate driver output LO in the same half-bridge are both "high". At this time, there will be very large harmful currents flowing through the upper and

lower power devices at the same time, and Accompanied by large power loss, it will directly damage the power devices in severe cases. When internal interference may cause the low-side input and high-side input of the same phase to be "high" at the same time, the protection circuit pulls the driver output HO and LO to "low", effectively turning off the power tube. When one of the input signals becomes "low", the driver output needs a dead time delay to output "high". This measure avoids the excessive switching of the power device caused by harmful short input pulses, effectively reduces the loss, and reduces the risk of damage to the power device.



Gate driver half bridge shoot-through protection diagram

GATE DRIVER OUTPUT (HO1,2,3/ LO1,2,3)

Both low-side and high-side drivers use voltage pulse output as the working mode, which is particularly suitable for driving power MOSFETs. Special attention is that after the high-side power supply VBS UVLO released, a new high-side logic input rising edge is required to re-energize the corresponding high-side output driver, and the output is "high". The low-side part will output directly when the VCC release from UVLO.

FORWARD AND REVERSE ROTATION SETTING

PT2522 can be set to forward or reverse mode through the FR pin, and can also be controlled through I2C. If the FR mode is changed, the motor will automatically stop and then rotate in the opposite direction.

VSP INPUT ROTATION SPEED CONTROL

The VSP of PT2522 can use external DC voltage, PWM or Clock frequency control to change the motor speed. When using PWM input, the highest voltage must be greater than 3.5V, and the lowest voltage must be less than 0.3V. The recommended PWM frequency is 15KHz to 25KHz.

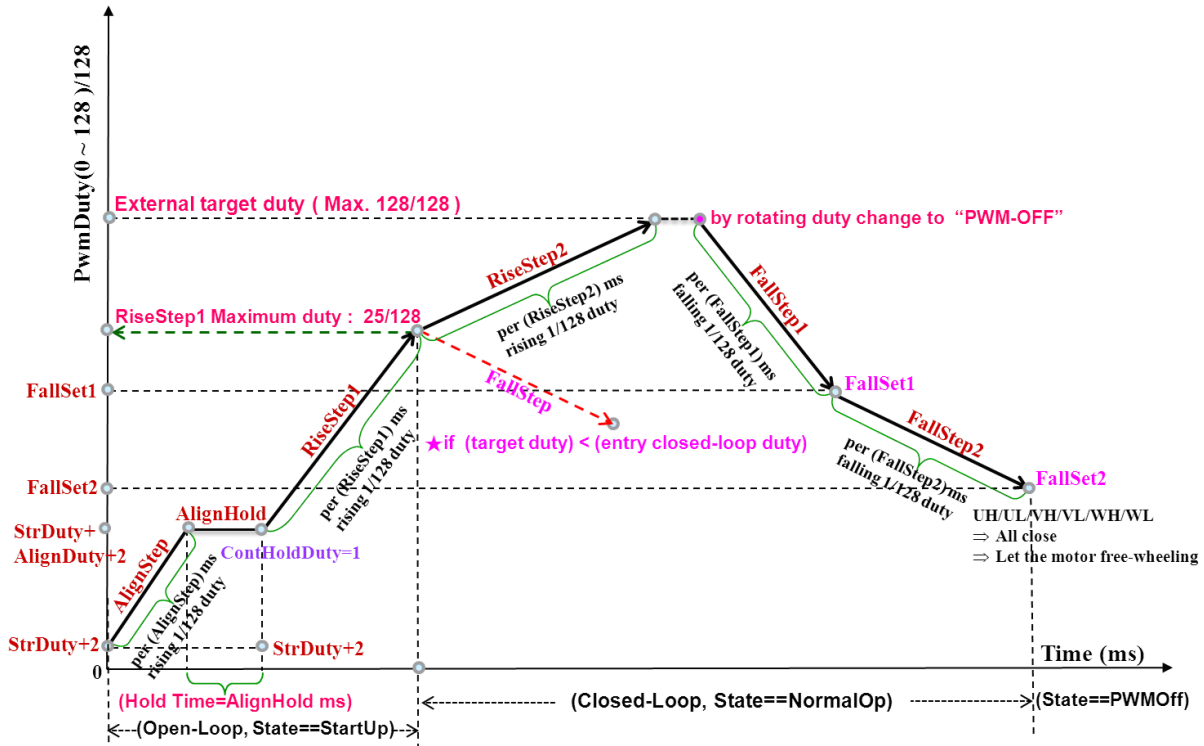
When PT2522 uses DC or PWM input, open loop and closed loop control can be set, and clock input can only be used for closed loop control. For detailed setting, please refer to the parameter setting section. When using DC direct current control, the adjustable speed range is between 0.6V and 3.3V. When using an external MCU to control the PT2522, the FG signal is the indicator for speed control.

In addition, PT2522 can also accept I2C to input PWM duty commands. In this case, please set VSP below 0.3V.

PARAMETERS SETTING

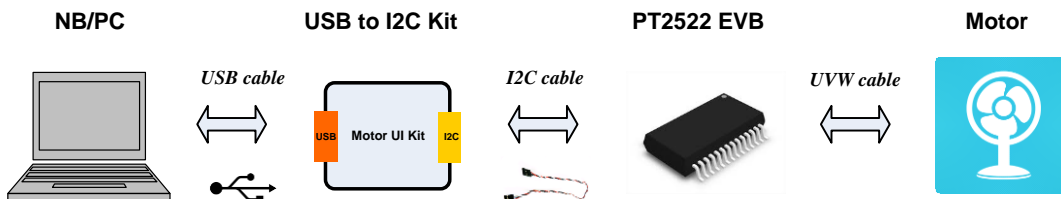
In addition to overcurrent, overheat protection and zero-crossing signal filter of PT2522, it needs to be set by resistor and capacitor of external pin. The other parameters need to be adjusted and recorded in internal OTP memory through I2C, such as startup process and acceleration/deceleration time. And voltage backward compensation. When using OTP to burn, it is necessary to provide +7.5V to the VPP pin.

The figure below shows a schematic diagram of some parameters of PT2522. For detailed parameter description and adjustment method, please refer to PT2502 or PT2522_UI_Application_Note file.



I²C INTERFACE

The PT2522 can control or release parameters or perform OTP parameter recording via I2C. When parameter adjustment is made, the internal interface of the IC can be modified by using the USB interface of the NB/PC to the I2C mode. The connection mode is as follows:



When the parameter adjustment of the IC register is performed through I2C, it does not affect the OTP recording, so it can be arbitrarily adjusted until it meets the requirements.

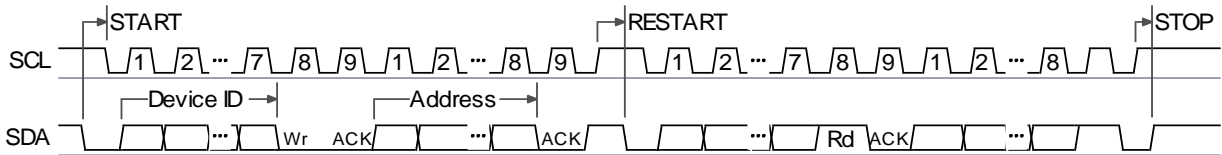
The adjusted parameters can be archived or burned. Please note that when the adjusted value is not recorded in the OTP of the IC, the register value will not be the value of the NB/PC end after the IC is re-powered, but there will be three cases:

1. When OTP bank0 & bank1 is blank, the register will be filled in by default.
2. When OTP bank0 has a value and bank1 is blank, the register will fill in the bank0 value.
3. When both OTP bank0 & bank1 have a value, the register will fill in the bank1 value.

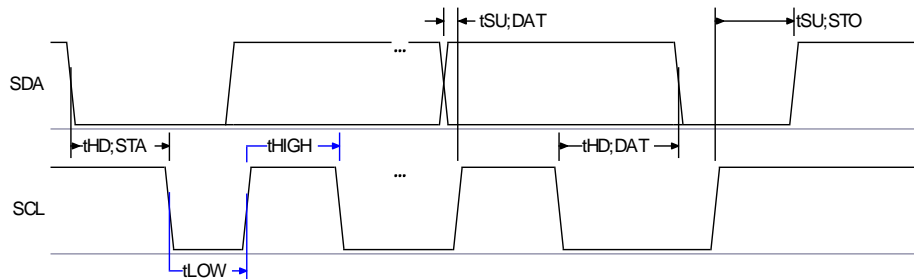
I²C DATA WRITE TIMING DIAGRAM



I²C DATA READ TIMING DIAGRAM



I²C FREQUENCY SPECIFICATION



Parameter	Symbol	Min.	Max.	Unit
SCL clock frequency	f _{SCL}	0	50	KHz
Hold time START condition	t _{HD,STA}	4		μS
LOW period of the SCL clock	t _{LOW}	4.7		μS
HIGH period of the SCL clock	t _{HIGH}	4.0		μS
Data setup time	t _{SU,DAT}	250		nS
Data hold time	t _{HD,DAT}	5.0		μS
Setup time for STOP condition	t _{SU,STO}	4.0		μS

I²C READ / WRITE CONTROL

The commonly used I2C read/write command table (READ / WRITE COMMAND TABLE) is as follows:

Register map (address h00 ~ h04):

Bit							Address	Default	
7	6	5	4	3	2	1	0	Hex	Hex
PWM_I2C							0	0x00	
FG_I2C[7:0]							1	0x00	
FG_I2C[11:8]							2	0x00	
Mstate[2:0]							3	0x00	
RD							4	0x40	
TSD									
OVP									
OCP									

Read /Write command table (address h00 ~ h04):

Address (HEX)	Bytes	Register	Description	Default (Hex)	(R/W)
0X00	BIT[7:3]	RESERVED		0X00	
	BIT[2]	PWMS_EN	1: select PWM duty cycle via I2C (PWM_I2C[7:0]) 0: select PWM duty cycle via external VSP input		W
	BIT[1]	FWRS1_EN	1: forward/reverse control by I2C 0: forward/reverse control via external FWR input pin		W
	BIT[0]	FWRS0	Forward/reverse control 1: forward (default) 0: reverse		W
0X01	BIT[7:0]	PWM_I2C[7:0]	PWM duty command (written by I2C)	0X00	W
0X02	BIT[7:0]	FG_I2C[7:0]	FG frequency (read by I2C)	0X00	R
0X03	BIT[3:0]	FG_I2C[11:8]	Connect to 0x20 Bit[7:0]	0X00	R
0X04	BIT[7:5]	MSTATE[2:0]	Motor system status: [000] : Startup state (Start-Up) [001] : Normal operation (Normal) [010] : Shutdown state (PWM-Off) [011] : Over temperature/voltage protection status (TSD/OVP) [100] : Stalled state (Lock-On) [101] : Deadlock state (Dead-Lock)	0X40	R
	BIT[4]	RD	1 : Enter protection status 0 : Normal operation		R
	BIT[3]	TSD	1 : Over temperature protection status 0 : Normal		R
	BIT[2]	OVP	1 : Overvoltage protection status 0 : Normal		R
	BIT[1]	OCP	1 : Overcurrent protection status 0 : Normal		R
	BIT[0]	RESERVED			

I²C CONTROL PARAMETERS

The commonly used I2C control parameters are as follows:

Register Map (address h21 ~ h49):

Bit								Address	Default	
7	6	5	4	3	2	1	0			Hex
AlignStep[7:0]								21	0x64	
AlignHold[7:0]								22	0x00	
RiseStep1[7:0]								23	0x64	
RiseStep2[7:0]								24	0x64	
DutySel	SmoothSel[1:0]		RiseStep2[8]		RiseStep1[8]		AlignHold[9:8]	AlignStep[8]	25	0xC0
FallStep2[8]	FallStep1[8]	SSWDegree[2:0]			HMOS	ContHoldDuty	OCPSel		26	0x1E
FallStep1[7:0]								27	0x32	
FallStep2[7:0]								28	0x64	
EnOVP	BrakeEndSet[2:0]			DeadTime[3:0]				29	0x33	
FallSet1[7:0]								2A	0x28	
FallSet2[7:0]								2B	0x12	
OCP BlankWidth[2:0]			ZCTarget[4:0]					2C	0x8F	
ZCCntMn[7:0]								2D	0xC8	
DigitalFilter[9:8]			ZCCntMn[13:8]					2E	0x00	
DigitalFilter[7:0]								2F	0xC0	
FilterDelay[7:0]								30	0xB8	
FilterDelay[15:8]								31	0x0B	
MinDuty[7:0]								32	0x05	
StartTimeLimit[3:0]				LockStopTime[3:0]				33	0x55	
DeadLock[7:0]								34	0x14	
StartStep1[7:0]								35	0xE8	
EnSpdCtrl	DeadLock[8]	StartStep1[13:8]						36	0x03	
StartStep2[7:0]								37	0x20	
ShortNum[1:0]		StartStep2[13:8]						38	0xC3	
LowFreqthd[1:0]		WaitTime[9:8]			FrFloating[3:0]			39	0x41	
WaitTime[7:0]								3A	0x0D	
EnFreqSpd	StrDuty[6:0]							3B	0x03	
PreMUXTime[1:0]		AlignDuty[5:0]						3C	0x86	
MaxDuty[7:0]								3D	0x80	
Div4	BrakeCountSet[6:0]							3E	0x7F	
PreCheckTime[7:0]								3F	0x7C	
FGLSel[1:0]		PreCheckTime[13:8]						40	0x41	
BrakeClkSel[1:0]		RevBrakeTime[5:0]						41	0x7C	
TrimA[7:0]								42	0x88	
TrimB[7:0]								43	0x88	
TrimC[7:0]								44	0xF0	
ZcTooLong[7:0]								45	0xC8	
ZcTooLong[11:8]				EnPreCheck	SpdSel[2:0]				46	0x0B
ZCIgnoreTime[7:0]								47	0x80	
HysterSel[1:0]		ZCIgnoreTime[13:8]						48	0x42	
				ZCIgnoreSelect	ZCIgnorePhase[2:0]				49	0x01

PARAMETER LIST

(Address h21 ~ h49):

Address (HEX)	Bytes	Register	Description	Default (Hex)
0X21	BIT[7:0]	ALIGNSTEP [7:0]	During the process of setting Align, the force is gradually increased to avoid excessive swing. Add 1/128 duty to each set time (AlignStep).	0X64
0X22	BIT[7:0]	ALIGNHOLD [7:0]	Set the duration of Align.	0X00
0X23	BIT[7:0]	RISESTEP1 [7:0]	Set the slope of the start acceleration before entering the sensor-less control. Increase the RiseStep1 time by 1/128 duty and increase the maximum to 25/128 duty.	0X64
0X24	BIT[7:0]	RISESTEP2 [7:0]	After setting the sensor-less control, the slope of the acceleration is increased by 1/128 duty per RiseStep2 time, and the maximum increase is to the externally set speed or the PWM duty clamped by the internal protection control.	0X64
0X25	BIT[7]	DUTYSELECT	PWM duty processing selection, Default : 1. Set 1: The change of PWM duty output will be processed by the internal controller, and the ascending and descending curve can reach the progressive mode. Set 0: The PWM DUTY output change is not processed by the internal controller and is controlled by an external command.	0XC0
	BIT[6:5]	SMOOTHSEL [1:0]	After entering sensor-less, if the ZC signal is too jittery, it will be judged to be abnormal and the system will enter the stall protection. Set the range of ZC jitter.	
	BIT[4]	RISESTEP2 [8]	Connect to 0x24 Bit[7:0]	
	BIT[3]	RISESTEP1 [8]	Connect to 0x23 Bit[7:0]	
	BIT[2:1]	ALIGNHOLD [9:8]	Set the duration of Align. Unit ms. Default : 0.	
	BIT[0]	ALIGNSTEP [8]	Connect to 0x21 Bit[7:0]	
0X26	BIT[7]	FALLSTEP2 [8]	Connect to 0x28 Bit[7:0]	0X1E
	BIT[6]	FALLSTEP1 [8]	Connect to 0x27 Bit[7:0]	
	BIT[5:3]	SSWDEGREE [2:0]	Set the Soft-Switch angle setting. The larger the SSWDegree angle, the shorter the floating time angle will be.	
	BIT[2]	HIGH-SIDE MOS	High MOS polarity setting, default : 1. Set 1: Positive logic, Set 0: Negative logic.	
	BIT[1]	CONTHOLDDUTY	When AlignHold is finished, set whether to extend the power of Align as the starting force for starting. Default : 1. Set 0: RiseStep1 Duty starts with (StrDuty+2) Set 1: RiseStep1 Duty to continue Duty after the end of HoldTime.	

Address (HEX)	Bytes	Register	Description	Default (Hex)
	BIT[0]	OCPSEL	The PT2522 uses the voltage signal on the RF pin to detect the current flowing through the motor and MOS. When the voltage exceeds the set value, the PT2522 will reduce the PWM duty as an overcurrent or current limit protection. When the PWM duty is lowered, the reaction speed can be selected. Default : 0. Set 1: The reaction rate is 20KHz (0.5us), the reaction is fast, but there may be electronic noise. Set 0: The reaction rate is one electrical cycle (or ZC cycle), the reaction is slow, and there is no electronic noise due to OCP.	
0X27	BIT[7:0]	FALLSTEP1 [7:0]	The slope setting of the first step when PWM Duty decreases is reduced by 1/128 duty every (FallStep1)*ms.	0X32
0X28	BIT[7:0]	FALLSTEP2 [7:0]	The slope setting of the second step when PWM Duty decreases is reduced by 1/128 duty every (FallStep2)*ms.	0X64
0X29	BIT[7]	ENOV	Set 0: To cancel the overvoltage protection function.	0X33
	BIT[6:4]	BRAKEENDSET [2:0]	Setting the ZC length of the headwind brake to the quick stop. Default : 3 . Set 0: 7.8ms, Set 1: 15.6ms, Set 2: 23.4ms, Set 3: 31.2ms, Set 4: 39ms, Set 5: 46.8ms, Set 6: 54.6ms, Set 7: 70.2ms. Then start the Alignment program.	
	BIT[3:0]	DEADTIME [3:0]	The unit is a clock-cycle (0.39us), default: 3.	
0X2A	BIT[7:0]	FALLSET1 [7:0]	The set value of the separation of the two slopes of PWM Duty down decrease, and use FALLSTEP2 slope from this value.	0X28
0X2B	BIT[7:0]	FALLSET2[7:0]	If the PWMOFF or FWR reverse command is executed during operation, the PWM Duty is reduced to the Duty setting of the coasting (six MOS fully closed) state.	0X12
0X2C	BIT[7:5]	OCP_BLANKWIDTH [2:0]	Since the PWM signal is generated when the PWM is switched, and the switching noise could be filtered by an external low-pass filter. It can also be controlled internally to avoid this time, thus ensuring that the correct OCP signal can be read. This time is OCP blank. 0~4 clock-cycle (0.39us) can be set. When set to 0, the OCP blank function is canceled, Default : 4.	0X8F
	BIT[4:0]	ZCTARGET [4:0]	It is set that during the starting process, the correct number of ZCs are read and the system will be close to the sensor-less control. Recommended value is 10~25, Default : 15 .	
0X2D	BIT[7:0]	ZCNTMIN [7:0]	After entering sensor-less, if the ZC signal is too short, it will determine that it is not normal, and the system enters the stall protection. Set the ZC minimum time, the unit clock-cycle (0.39us).	0XC8

Address (HEX)	Bytes	Register	Description	Default (Hex)
0X2E	BIT[7:6]	DIGITALFILTER [9:8]	Connect to0x2F BIT[7:0]	0X00
	BIT[5:0]	ZCCNTMN [13:8]	Connect to0x2D BIT[7:0]	
0X2F	BIT[7:0]	DIGITALFILTER [7:0]	Set the width of the ZC signal digital filter (de-glitch). The unit is a clock-cycle (0.39us), Default: 192.	0XC0
0X30	BIT[7:0]	FILTERDELAY [7:0]	It is the delay time corresponding to the "External Circuit Filter Capacitor" + "Digital Filter". If this "Filter Delay" value is adjusted, the current waveform will be more stable than the symmetric ZC, and the efficiency control will be optimal. The unit is a clock-cycle (0.39us), default : 3000.	0XB8
0X31	BIT[7:0]	FILTERDELAY [15:8]		0X0B
0X32	BIT[7:0]	MINDUTY [7:0]	Limit the minimum duty of PWMIN, in units of 1/128 duty. The maximum setting is 64/128. When the input PWM duty is less than minDuty, it is PWM OFF, default : 5.	0X05
0X33	BIT[7:4]	STARTTIMELIMIT [3:0]	At startup, enter the sensor-less time limit, in seconds, default: 5. The setting range is 1~15 seconds. If sensor-less is not entered within the time, it will enter Lock-On State.	0X55
	BIT[3:0]	LOCKSTOPTIME [3:0]	The wait time setting when the System State enters the stall protection. Unit seconds, default : 5. The setting range is 1~15 seconds.	
0X34	BIT[7:0]	DEADLOCK [7:0]	The number of times Lock-On State is locked to the lock state, in units of Lock-On. That is, how many times Lock-On stops, it will lock the machine, you must re-plug the power to release.	0X14
0X35	BIT[7:0]	STARTSTEP1 [7:0]	During the start-up process, the correct ZC signal has not yet appeared, and the length of the step is forced to change.	0XE8
0X36	BIT[7]	ENSPDCTRL	Enable PWM-Duty Speed Control, default : 0, This enable is only useful when "enFreqSpd" is 0. This is the second level control command. Set 1: PWM IN is the fixed speed command controlled by duty. Set 0: When enFreqSpd is also 0, PWM IN is the original duty command.	0X03
	BIT[6]	DEADLOCK [8]	Connect to0x34 Bit[7:0]	
	BIT[5:0]	STARTSTEP1 [13:8]	Connect to0x35 Bit[7:0]	
0X37	BIT[7:0]	STARTSTEP2 [7:0]	During the start-up process, the ZC appears, but the length of the step is forced to change when the sensor-less control condition has not been reached. Unit is "ms", default : 800.	0X20
0X38	BIT[7:6]	SHORTNUM [1:0]	Since the ZC may be disturbed when it is too short, this parameter is set to be continuous. If the number of ZCs is too short, it is determined that the state is blocked. Set 0: disable , not judge, Set 1: Detect once, Set 2: detect two consecutive times, Set 3: Detected three times in succession.	0XC3

Address (HEX)	Bytes	Register	Description	Default (Hex)
	BIT[5:0]	STARTSTEP2 [13:8]	Connect to 0x37 Bit[7:0]	
0X39	BIT[7:6]	LOWFREQTHD	Low Frequency Threshold, the lowest frequency limit entered during the frequency speed control command. When the input control frequency is less than the "LowFreqThd" setting value, it is Frequency OFF, default : 1. Set 0: 1Hz, Set 1: 5Hz, Set 2: 10Hz, Set 3: 20Hz.	0X41
	BIT[5:4]	WAITTIME 9:8]	Connect to 0x3A Bit[7:0]	
	BIT[3:0]	FRFLOATING [3:0]	When the FWR reverse command is executed, and FallSet2 is executed, the fan coasts down to the fast stop (ZC does not change for 0.3 seconds), and the buffer time setting for starting in the reverse direction is prepared.	
0X3A	BIT[7:0]	WAITTIME [7:0]	The PT2522 uses square wave control (120 degree control) during start-up. This is the delay time to change the trapezoidal wave control after entering the sensor-less control, so that the sensor-less control is more stable. WaitTime is 32ms per unit, Default : 13, which is 416ms.	0X0D
0X3B	BIT[7]	ENFREQSPD	Enable Frequency Speed Control, default: 0, This is the highest control command. Set 1: Speed control command for frequency input, Set 0: The fixed speed command controlled by Duty or the original PWM Duty command.	0X03
	BIT[6:0]	STRDUTY [6:0]	Set the initial force to overcome the static friction of the motor. Set the startup duty in Alignment & Startup stage. Unit 1/128 duty, default: 3.	
0X3C	BIT[7:6]	PREMUXTIME [1:0]	Set the time to check the U, V, W three-phase in turn, to determine whether the motor is in forward or reverse rotation, default : 2.	0X86
	BIT[5:0]	ALIGNDUTY [5:0]	Set the maximum force of Align, unit 1/128 duty. Maximum is 31/128 duty, default : 6	
0X3D	BIT[7:0]	MAXDUTY [7:0]	Limit the maximum duty of PWMIN in units of 1/128 duty. The minimum setting is 64/128. When the input PWM duty is greater than maxDuty, the output is maxDuty, default : 128 °	0X80
0X3E	BIT[7]	DIV4	Input Frequency Divided by 4 , default : 0 ° Set 1: The input frequency is four times the FG output frequency. Set 0: The input frequency is the same as the FG output frequency.	0X7F
	BIT[6:0]	BRAKECOUNTSE T [6:0]	Set the time interval between breaks (resting), which is a multiple of BrakeClkSel (1~127), default: 127.	
0X3F	BIT[7:0]	PRECHECKTIME [7:0]	Set the maximum time for the PreCheck program to start upwind.	0X7C

Address (HEX)	Bytes	Register	Description	Default (Hex)
0X40	BIT[7:6]	FGLSEL [1:0]	FG output frequency setting, unit Hz, default : 1 . Set 0: FG output is the FG frequency divided by 2, Set 1: For normal FG frequency, if it is 8 poles motor, the speed is (15 * FG frequency) rpm, Set 2: FG output is the FG frequency multiplied by 2. Set 3: FG output be the FG frequency multiplied by 3.	0X41
	BIT[5:0]	PRECHECKTIME [13:8]	Connect to 0x3F Bit[7:0]	
0X41	BIT[7:6]	BRAKECLKSEL [1:0]	When the headwind is detected, the PT2522 will stop and restart first. The brake adopts the point brake method, and the time is longer than the one brake, such as the first brake for 1ms, the second time for 2ms, the third time. It is 3ms, and so on until the motor stops. BrakeCLKSel is the unit time for setting the brake, default : 1 (500us). Set 0: 100us, Set 1:500us, Set 2: 1ms, Set 3: 2ms.	0X7C
	BIT[5:0]	RESERVED		
0X42	BIT[7:0]	RESERVED		0X88
0X43	BIT[7:0]	RESERVED		0X88
0X44	BIT[7:0]	RESERVED		0XF0
0X45	BIT[7:0]	ZCTOOLONG [7:0]	After entering sensor-less, if the ZC signal is too long, it will judge that it is not normal, and the system enters the stall protection. Set the ZC for the longest time.	0XC8
0X46	BIT[7:4]	ZCTOOLONG [11:8]	Connect to 0x46 Bitp7:0]	0X0B
	BIT[3]	ENPRECHECK	Default : 1 . Set 1: There is a forward wind start detection procedure Set 0: No forward wind start detection procedure	
	BIT[2:0]	SPDSEL [2:0]	Select the FG frequency range of the fixed speed command with PWM-Duty control, Default : 3. Set 0: 16Hz, Set 1:32Hz, Set 2: 64Hz, Set 3: 128Hz, Set 4: 256Hz, Set 5: 512Hz, Set 6: 1024Hz, Set 7: 2048Hz	
0X47	BIT[7:0]	ZCIGNORETIME [7:0]	For the fixed time in the ST1 & ST2 formula, the unit is a clock-cycle (0.39us), default : 640.	0X80

Address (HEX)	Bytes	Register	Description	Default (Hex)
0X48	BIT[7:6]	HYSTERSEL [1:0]	The PT2522 provides constant speed control (speed closed loop control). The command input can use Frequency (or Clock), PWM duty, VSP voltage. The same is required for the hysteresis parameter. Set the frequency or the hysteresis angle of the PWM-Duty fixed speed command. Hysteresis select ,default : 1 . Set 0: no hysteresis, Set 1: Hysteresis 0.23 degrees, Set 2: Hysteresis 0.47 degrees, Set 3: hysteresis of 0.94 degrees.	0X42
	BIT[5:0]	ZCIGNORETIME [13:8]	Connect to 0x47 Bit[7:0]	
0X49	BIT[7:4]	RESERVED		0X01
	BIT[3]	ZCIGNORESELECT	When the motor is commutating, the ZC signal is unstable at this time, and it is necessary to avoid this time. The PT2522 provides two formula options to set the blanking time, Default : 0.	
	BIT[2:0]	ZCIGNOREPHASE [2:0]	Ignore to detection ZC in angle, default: 1 => 3.75 degrees. Set 0: 1.875 degrees, Set 1: 3.75 degrees, Set 2: 7.5 degrees, Set 3: 11.25 degrees, Set 4:15 degrees, Set 5: 18.75 degrees, Set 6: 20.625 degrees, Set 7: 22.5 degrees.	

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max.	Unit
V _{DD} supply voltage	V _{DD}	5	28	V
High-side floating supply voltage	V _{B1,2,3}	-0.3	90	V
High-side floating supply offset voltage	V _{S1,2,3}	V _{B1,2,3} -20	V _{B1,2,3} +0.3	V
High-side gate driver output voltage	V _{HO1,2,3}	V _{S1,2,3} -0.3	V _{B1,2,3} +0.3	V
Low-side gate driver output voltage	V _{LO1,2,3}	COM-0.3	VCC+0.3	V
Low-side supply voltage	V _{CC}	-0.3	20	V
Allowable offset voltage slew rate	dV/dt	—	50	V/ns
Input/Output voltage	-	-0.3	6	V
Operating temperature	T _A	-40	+ 85	°C
Storage temperature	T _{STG}	-40	+150	°C

ELECTRICAL CHARACTERISTIC

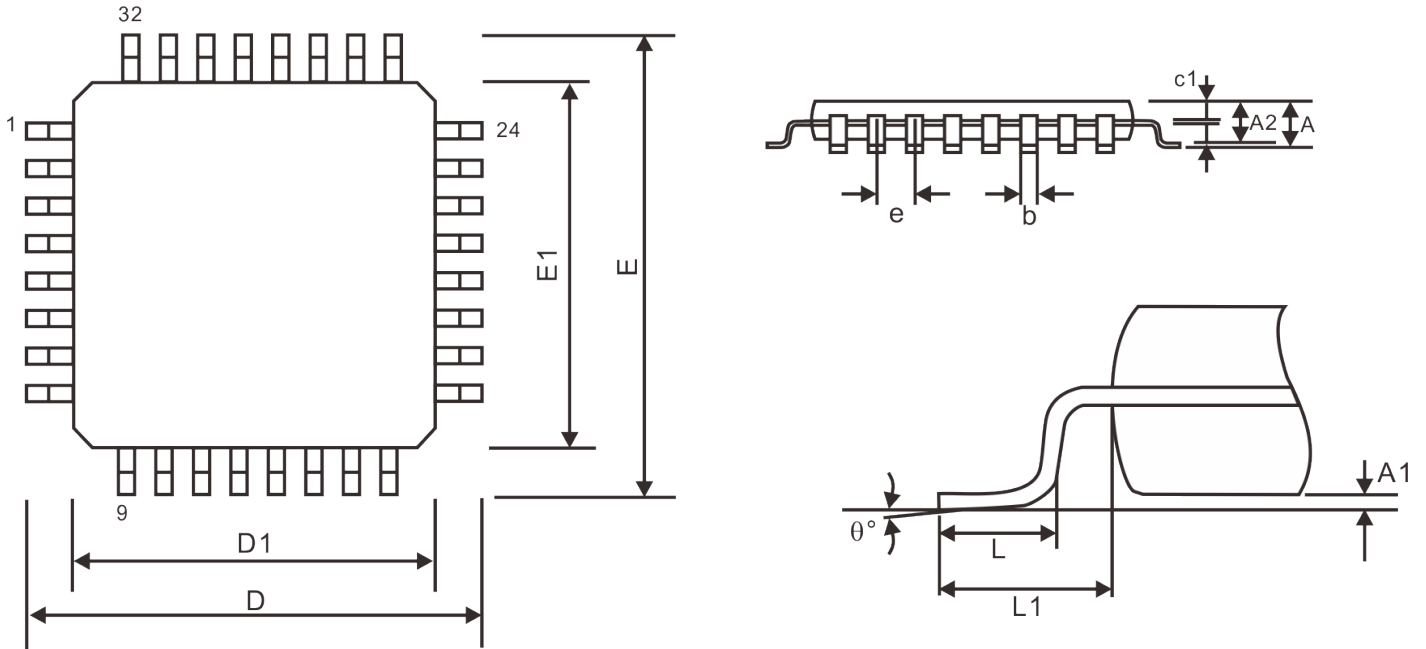
VCC=VDD = 12.0V, GND = VSS=0V, T_A = + 27°C unless otherwise specified

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
General						
VDD supply voltage	V _{DD}	VDD input	6	12	24	V
Low-side supply voltage	V _{CC}		5.5	—	18	V
High-side floating supply offset voltage	V _{S1,2,3}		COM-6	—	60	V
High-side floating supply voltage	V _{B1,2,3}		V _{S1,2,3} +5.5	—	V _{B1,2,3} +18	V
High-side gate driver output voltage	V _{HO1,2,3}		VS	—	VB	V
Low-side gate driver output voltage	V _{LO1,2,3}		COM	—	VCC	V
VDD power supply current	I _{DD}	VDD = 12V	4	5	7	mA
VCC power supply current	I _{CC}	PWM off	0.2	0.3	0.5	mA
Regulator output voltage	V _{REG}		4.75	5	5.25	V
Regulator output current	I _{REG}		10	20		mA
Pin parameter setting						
Over current protection voltage	V _{OCP}	RF pin		0.3		V
External oscillator	F _{OSC_1K}	OSC_C= 470pF		1		KHz
External oscillator frequency range	F _{OSC_C}	OSC_C pin	0.1	-	10	KHz
Operation Characteristics						
PWM switching frequency	F _{SW}			20		KHz
I/O interface						
Logic output high level	V _{OH}	FG, RD	4.0	4.5	5.5	V
Logic output low level	V _{OL}	FG, RD		0	0.3	V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Logic input pull high current	I _{source}	FR			10	μA
VSP DC for control range	VSP _{DC}	DC input	0.3		3.0	V
VSP input high level for PWM	VSP _H	PWM & CLK input	3.3			V
VSP input low level for PWM	VSP _L	PWM & CLK input			0.3	V
VSP input frequency range for PWM	VSP _F	PWM input	15		25	KHz
RSEN internal pull high resistance	R _{SEN}	RSEN pin, connect to V _{REG}		47		KΩ
Over temperature protection trigger level	V _{OTP}	RSEN pin	—	0.6	—	V
Over temperature protection reset level	V _{REL}	RSEN pin	—	1.2	—	V
Gate Driver Low Side Power Supply Characteristics						
VCC supply under-voltage positive going threshold	V _{CCUV+}	—	2.9	4.2	5.5	V
VCC supply under-voltage negative going threshold	V _{CCUV-}	—	2.5	3.8	5.1	V
VCC supply under-voltage lockout hysteresis	V _{CCHYS}	—	—	0.4	—	V
Gate Driver High Side Floating Power Supply Characteristics						
High side VBS supply under-voltage positive going threshold	V _{BSUV+}	—	2.5	3.8	5.5	V
High side VBS supply under-voltage negative going threshold	V _{BSUV-}	—	2.2	3.5	4.8	V
High side VBS supply under-voltage lockout hysteresis	V _{BSUVHYS}	—	—	0.3	—	V
Gate Driver Characteristics						
High side output HIGH short-circuit pulse current	I _{HO+}	V _{HO} =V _S =0	—	1.2	—	A
High side output LOW short-circuit pulse current	I _{HO-}	V _{HO} =V _B =15V	—	2.0	—	A
Low side output HIGH short-circuit pulse current	I _{LO+}	V _{LO} =0	—	1.2	—	A
Low side output LOW short-circuit pulse current	I _{LO-}	V _{LO} =V _{CC} =15V	—	2.0	—	A
Gate driver dead time	DT	without external dead time	300	500	700	ns

PACKAGE INFORMATION

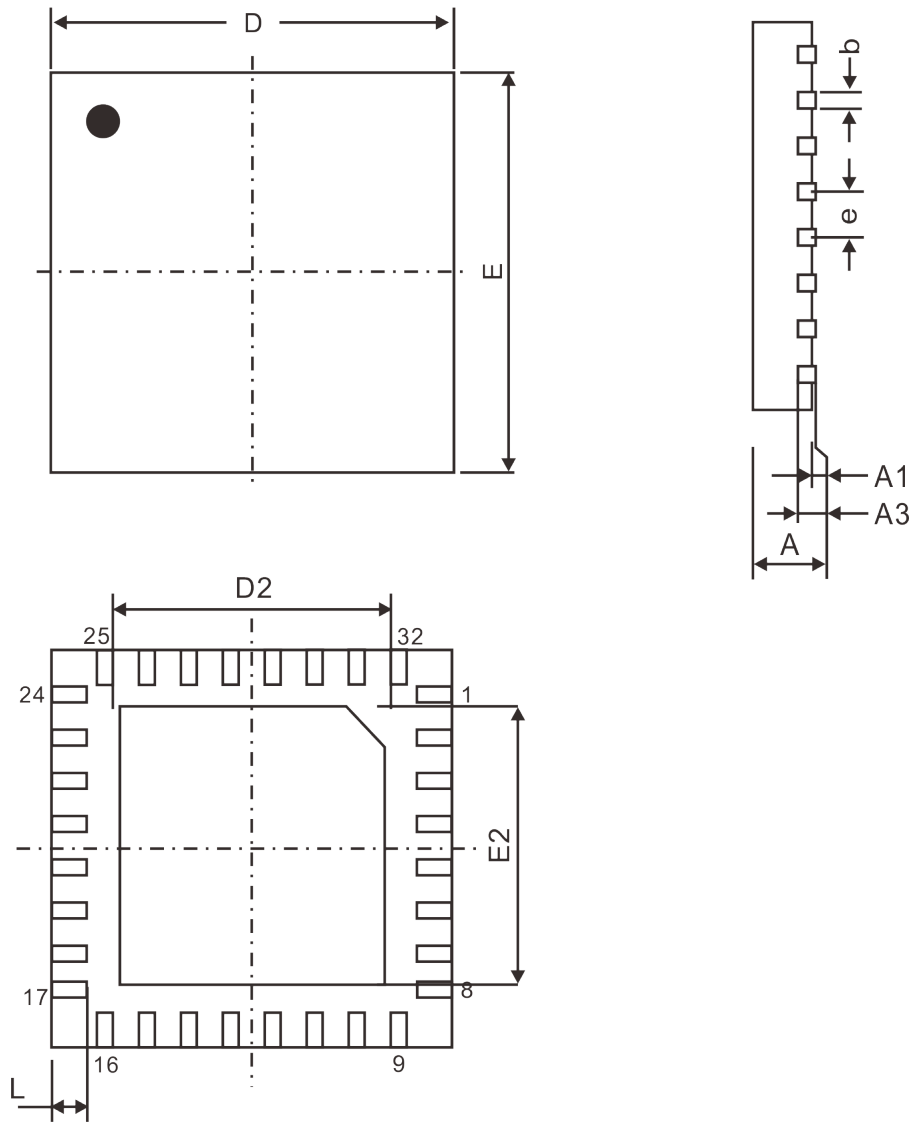
32 PINS, LQFP, 7X7 MM



Symbol	Dimensions(mm)		
	Min.	Nom.	Max.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c1	0.09	-	0.20
D	9.00 BSC.		
D1	7.00 BSC.		
E	9.00 BSC.		
E1	7.00 BSC.		
e	0.80 BSC.		
L	0.45	0.60	0.75
L1	1.00 REF.		
θ	0°	3.5°	7°

NOTES: REFER TO JEDEC MS-026 BBA

32 Pins, QFN, 5X5 MM



Symbol	Dimensions(mm)		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20 REF		
b	0.18	0.25	0.30
D	5.00 BSC		
D2	3.15	-	3.30
E	5.00BSC		
E2	3.15	-	3.30
e	0.50 BSC.		
L	0.35	0.40	0.45

NOTES: REFER TO JEDEC MO-220 WHHD-5

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Princeton Technology Corp.
2F, No. 233-1, Baociao Road,
Sindian Dist., New Taipei City 23145, Taiwan
Tel : 886-2-66296288
Fax: 886-2-29174598
<http://www.princeton.com.tw/>