

## FEATURES

- **Core**
  - ARM® 32-bit Cortex®-M0 MCU
  - Frequency up to 48MHz
- **Storage unit**
  - 32K bytes Flash
  - 4K bytes SRAM
- **Reset and power management**
  - Digital and I/O supply :  $V_{DD33}=2.7 \sim 3.6V$
  - Analog supply :  $V_{DDA}=2.7 \sim 3.6V$
  - POR/PDR
  - Programmable voltage detector (PVD)
  - Low power modes : SLEEP、STOP and STANDBY
- **Clock source management**
  - 4 to 32 MHz crystal oscillator
  - Internal 4MHz RC oscillator
  - Internal 32 ~40 kHz RC oscillator
  - PLL phase-locked loop with fractional frequency setting up to a maximum of 48MHz
- **Interface resources**
  - Up to 43 GPIOs
- **Up to 6 timers**
  - Three 16 /32 bits Timers
  - One-Shot/Periodic mode counting function
  - Input capture
  - Output comparison
  - Three Pulse Width Modulation (PWM)
  - One Real Time Clock (RTC)
- **Communication Interface**
  - One I2C
  - One SPI
  - Two UARTs, Auto-Baud rate detection and Auto-Flow control
- **Analog control unit**
  - One 12-bit ADC, 1MSPS, up to 16 external channels
  - Four CMPs, analog comparators
- **Serial wire debug (SWD)**
  - One watchdog timer (WDT)
- **Operating temperatures: -40°C to +105°C**
- **Three-Phase Gate Driver**
  - 90V half-bridge high side driver
  - Driver up to 3-phase half-bridge gates
  - Built-in dead time control 0.5 $\mu$ s (typ.)
  - Shoot-through protection
  - Common-mode dV/dt noise cancellation circuit
  - Tolerant of negative transient voltage
- **Package type**
  - LQFP48 ( 7x7mm )

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# 1 Introduction

The datasheet for the PT32M625 series microcontrollers provides information on resource allocation and physical characteristics of the device. When reading the datasheet, it is recommended to refer to the 《PT32U301 Reference Manual》 for further details. For information on the Cortex-M0, you can refer to the 《Cortex-M0 Technical Reference Manual》, which is available from the ARM official website (<http://infocenter.arm.com>).

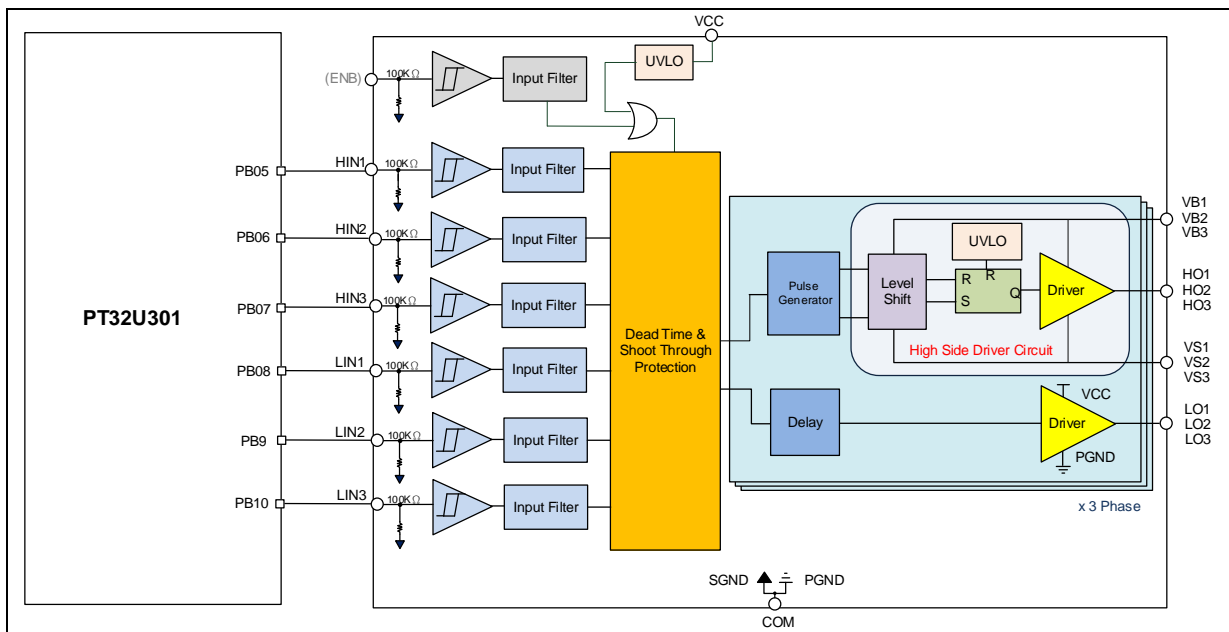
Datasheet : PT32M625\_DS\_E.pdf

Reference Manual : PT32U301\_RM\_E.pdf

## 2 Description

The PT32M625 is a SiP (System in Package) with MCU PT32U301 and a motor gate driver. The PT32M625 microcontroller is a series of low-power microcontroller incorporating a high-performance ARM Cortex™-M0 32-bit RISC core. It operates at a maximum 48Mhz frequency and features up to 32Kbytes of Flash and up to 4Kbytes of SRAM. The motor gate driver is a high-speed 3-phase gate driver for power MOSFET and IGBT devices with three independent high and low side referenced output channels. Built-in dead time protection and shoot-through protection prevent damage to the half-bridge.

Figure 2-1 PT32M625 SiP block diagram



## 2.1 Device features and peripheral counts

Table 2-1 PT32M625 Device features and peripheral counts

Peripheral		PT32M625
Flash (Kbytes)		32
SRAM (Kbytes)		4
GPIO		Max: 43
12-bit ADC		1 (8channels)
CMP		4
Timers	GP Timer	3
	PWM	3
	RTC	1
	WWDT	1
Communications	I2C	1
	SPI	1
	UART	2
CPU Operating Frequency		Max. 48 MHz
Digital operating voltage ( $V_{DD33}$ )		2.7V – 3.6V
Analog operating voltage ( $V_{DDA}$ )		2.7V – 3.6V
Package Type		LQFP48

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## 2.2 MCU Functional Overview

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### 2.2.1 MCU Core

#### 2.2.1.1 ARMCortex-M0 Core

This processor is configured with the following functions :

- ◇ Built-in vectored interrupt controller (NVIC): 32 external interrupts
- ◇ Little endian mode
- ◇ Integrated system timer - SysTick
- ◇ Supports debug halt
- ◇ Accelerated multiplier
- ◇ Support serial wire debug (SWD) connection

This chapter provides basic information about the following processor peripherals.

- ◇ CPU system timer controller (SysTick)
- ◇ CPU nested vectored interrupt controller (NVIC)
- ◇ CPU system control

#### 2.2.1.2 Nested Vectored Interrupt Controller (NVIC)

- ◇ 32 maskable interrupt channels (not including 16 interrupt lines)
- ◇ Programmable priority (using 2-bit interrupt priority)
- ◇ Low latency exception and interrupt processing
- ◇ Power management control
- ◇ System control register implementation

NVIC and the processor core interface are tightly coupled to achieve low-latency interrupt processing and efficient processing of late arrival interrupts. NVIC controls all the core exceptions and all interrupts.

#### 2.2.1.3 SysTick Timer

Includes an integrated system timer-SysTick, which provides a simple 24-bit clear, decrement, zero wrap counter and flexible control mechanism. This counter can be used as a real-time operating system (RTOS) timer or simple counter.

## 2.2.2 Memories

Embedded flash memory allows users to store application code or data and enables users to modify data on chips soldered onto the PCB via SWD.

### 2.2.2.1 Static Random Access Memory

Supports up to 4 KByte SRAM and single-cycle access to the core.

### 2.2.2.2 FLASH

The maximum 32 KByte FLASH storage space is used to store programs and data

## 2.2.3 System Management

### 2.2.3.1 Power Supply

2.0V~3.6V power supply, supplies power to all IOs and internal regulators through pin  $V_{DD33}$ .

### 2.2.3.2 Power Monitoring

- ◇ Power-on reset (POR) occurs when the power supply voltage falls below  $V_{POR}$ , the system enters a reset state.
- ◇ Power-down reset (PDR) occurs when the power supply voltage falls below  $V_{PDR}$ , the system enters a reset state.

Programmable low voltage detector (PVD): When the power supply voltage reaches the configured VLVD threshold, an interrupt event is generated.

### 2.2.3.3 Low Power Mode

PT32U301 provides three low-power modes:

- ◇ SLEEP Mode
- ◇ STOP Mode
- ◇ STANDBY Mode

### 2.2.3.4 Clock Management

- ◇ HSI : Internal high-speed RC oscillator with a frequency of 4 MHz.
- ◇ HSE : External high-speed crystal oscillator, supporting 4 MHz to 32 MHz.
- ◇ LSI : Internal low-speed RC oscillator, with a frequency of 32k to 40k Hz.
- ◇ PLL : The phase-locked loop (PLL) can multiply the frequency up to 48 MHz, supports fractional frequency settings, and allows the selection of HSI or HSE as the reference clock source.

### 2.2.3.5 Watchdog Timer

The WWDT (Windowed Watchdog Timer) uses either the system clock PCLK or LSE as its counting clock. Its function is to detect situations where the software fails to refresh the watchdog (too late) or refreshes it too early. If either occurs, it triggers a system reset to prevent the program from entering an uncontrolled state.

## 2.2.4 External Interface

### 2.2.4.1 General Inputs/Outputs (GPIO)

Each GPIO pin can be individually configured as input or output, with independent open-drain or push-pull output control, and options for pull-up or pull-down selection. Each port also provides independent, configurable edge or level detection, capable of generating interrupt or event requests.

### 2.2.5 Timer

The PT32U301 includes three timers with the following functions:

- ◇ 16/32-bit timer
- ◇ 1-shot and periodic mode counting functions
- ◇ Output compare
- ◇ Input capture

## 2.2.6 Communications

### 2.2.6.1 Universal Asynchronous Receiver Transmitter (UART)

UART provides a flexible way for MCU to realize full-duplex asynchronous serial data communication with external devices in the form of industry standard NRZ. UART can use fractional baud rate generator to provide ultra-wide baud rate setting range.

UART supports asynchronous communication mode and modem flow control operations (CTS/RTS), while also supporting multi-device communication.

Table 2-2 UART0/1 specific function configuration

UART modes/feature	UART1/2
Auto-Flow Control	v
IrDA SIR module	v
Auto baud rate detection mode	v
The 9-bit mode in RS485	v
UART data length	5, 6, 7, 8, 9

### 2.2.6.2 Inter-Integrated Circuit (I2C)

I2C is a two-wire bidirectional serial transmission bus that provides a simple and effective method to realize data exchange between devices.

The I2C standard is that a multi-master bus includes collision detection and arbitration. If two or more masters try to control the bus at the same time, the arbitration can prevent data corruption. Standard mode (Sm), fast mode (Fm) and very fast mode (Fm+) are provided here for users to choose.

### 2.2.6.3 Serial Peripheral Interface (SPI)

Serial Peripheral Interface (SPI) can carry out half-duplex or full-duplex synchronous serial communication with external SPI devices. The interface can be configured as master mode or slave mode. When configured as master mode, it can provide communication clock (SCK) for external SPI slave device.

## 2.2.7 Analog

### 2.2.7.1 Analog Comparator (CMP)

It supports two independent analog comparators (CMP1 and CMP2), offering positive and negative input selection for comparing analog signal voltages.

- ◇ Two independent analog comparators
- ◇ Shared internal reference voltage
- ◇ CMP1 and CMP2 can be configured as a window comparator for monitoring
- ◇ Blanking source comparator output
- ◇ Each comparator has a positive input and a configurable negative input, with the configurable negative input options being:
  - I/O input pin
  - Internal reference voltage (VREFINT)
- ◇ Provides triggers for other IPs to use (e.g., Timer)
- ◇ Each comparator can generate an interrupt (through the EXTI controller)

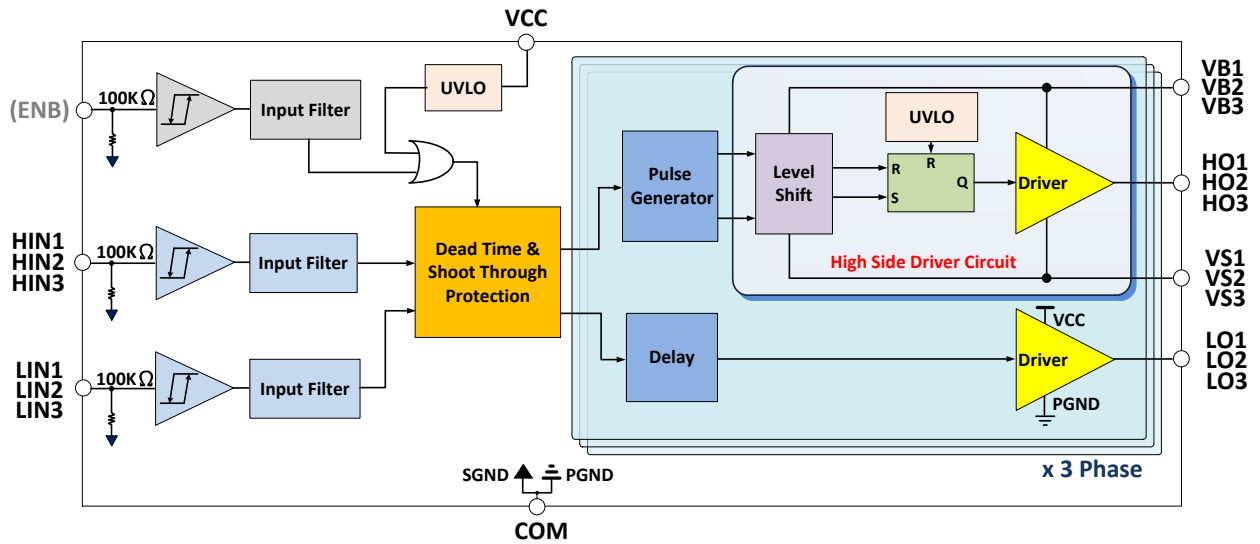
### 2.2.7.2 Analog-to-digital conversion (ADC)

It supports a 12-bit analog-to-digital converter (ADC) with a Successive Approximation Register (SAR) architecture. There are a total of 9 channels, supporting up to 8 external signal inputs and a temperature sensor input.

## 2.3 Three-phase gate driver Functional Description

### 2.3.1 Three-phase gate driver Block Diagram

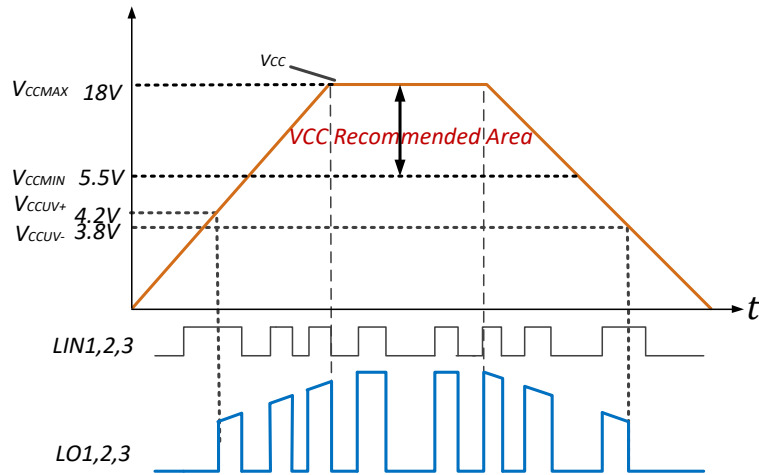
Figure 2-2 Block Diagram of Three-phase gate driver



### 2.3.2 Low Side Power Supply: VCC

VCC is the low side supply and it provides power to both input logic and low side output power stage. The built-in under-voltage lockout circuit enables the device to operate at sufficient power when a typical VCC supply voltage higher than  $V_{CCUV+} = 4.2V$  is present, shown Figure 2-3. The IC shuts down all the gate driver outputs, when the VCC supply voltage is below  $V_{CCUV-} = 3.8 V$ , shown as Figure.2-3. This prevents the external power devices against extremely low gate voltage levels during on-state which may result in excessive power dissipation.

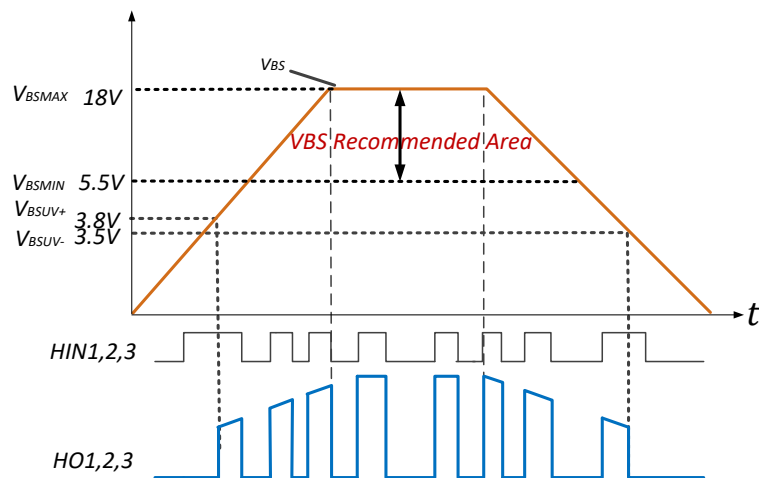
Figure 2-3 VCC Supply UVLO Operating Area



### 2.3.3 HIGH Side Power Supply: VBS (VBU-VSU, VBV-VS, VBW-VSW)

VBS is the high side supply voltage. The total high side circuitry may float with respect to COM following the external high side power device emitter/source voltage. Due to the internal low power consumption, the entire high side circuitry may be supplied by bootstrap topology connected to VCC, and it may be powered with small bootstrap capacitors. The device operating area as a function of the supply voltage is given in Figure 2-4

Figure 2-4 VBS supply UVLO operating area

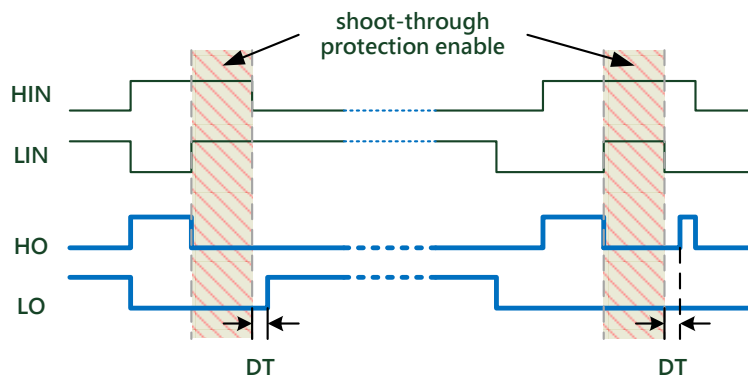


### 2.3.4 Shoot-through prevention

The IC is equipped with shoot-through protection circuitry (also known as cross conduction prevention circuitry).

Figure 2-5 shows how this protection circuitry prevents both the high- and low-side switches from conducting at the same time. When the inputs controlling both high-side and low-side drivers are both logic HIGH, then both driver outputs are pulled down to logic LOW to shut down two power devices in the same bridge.

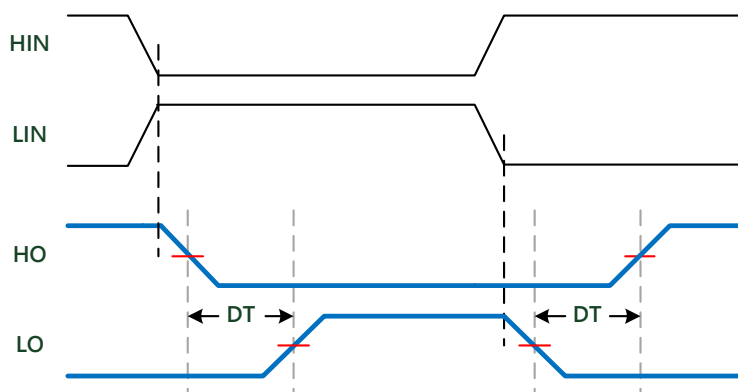
Figure 2-5 Shoot-through Prevention



### 2.3.5 DEAD TIME PROTECTION

The IC features integrated fixed dead time protection circuitry. The dead time feature inserts a time period (a minimum dead time) in which both the high- and low-side power switches are held off. This is done to ensure that the power switch has fully turned off before the second power switch is turned on. This minimum dead time is automatically inserted whenever the external dead time is shorter than DT. External dead times larger than DT are not modified by the gate driver. Figure 2-6 illustrates the dead time period and the relationship between the output gate signals.

Figure 2-6 Dead time protection



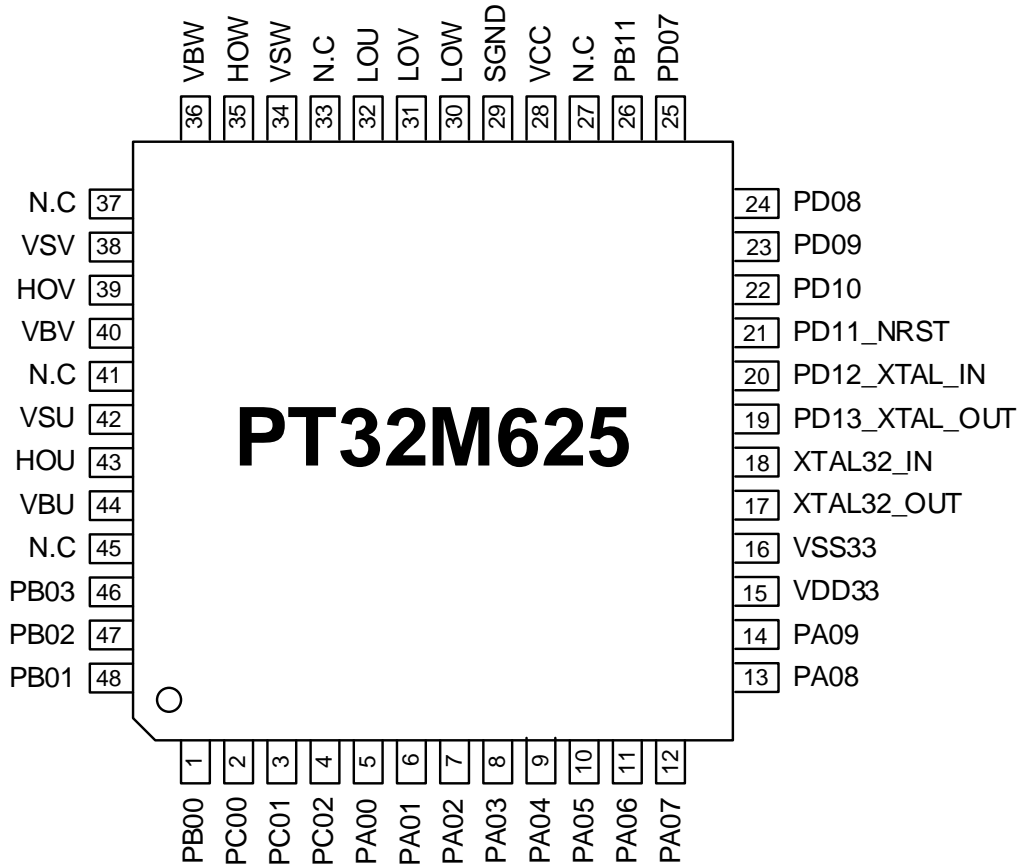
### 2.3.6 GATE DRIVER (HOU,V,W/ LOU,V,W)

Low side and high side driver outputs are specifically designed for pulse operation and dedicated to drive power devices such as IGBT and power MOSFET. Low side outputs (i.e. LOU,V,W) are state triggered by the respective inputs, while high side outputs (i.e. HOU,V,W) are only changed at the edge of the respective inputs. After releasing from an under-voltage condition of the VBS supply, a new turn-on signal (edge) is necessary to activate the respective high side output. In contrast, after releasing from an under-voltage condition of the VCC supply, the low side outputs may directly switch to the state of their respective inputs without the additional constraints of the high side driver.

### 3 PIN CONFIGURATION

#### 3.1 LQFP48 (7x7 mm) Pin Diagram

Figure 3-1 PT32M625 48-Pin (7x7mm) LQFP diagram



## 4 PIN DESCRIPTION

### 4.1 Pin Definition

Each GPIO line can be assigned to one of the peripheral functions. The following table lists out the pin name of all packages and its respective available alternate function.

Table 4-1 Pin definition

Pin No.	Pin Name	Pin Type	Description
1	PB00	I/O	General Purpose Digital I/O Pin
2	PC00	I/O	General Purpose Digital I/O Pin
3	PC01	I/O	General Purpose Digital I/O Pin
4	PC02	I/O	General Purpose Digital I/O Pin
5	PA00	I/O	General Purpose Digital I/O Pin
6	PA01	I/O	General Purpose Digital I/O Pin
7	PA02	I/O	General Purpose Digital I/O Pin
8	PA03	I/O	General Purpose Digital I/O Pin
9	PA04	I/O	General Purpose Digital I/O Pin
10	PA05	I/O	General Purpose Digital I/O Pin
11	PA06	I/O	General Purpose Digital I/O Pin
12	PA07	I/O	General Purpose Digital I/O Pin
13	PA08	I/O	General Purpose Digital I/O Pin
14	PA09	I/O	General Purpose Digital I/O Pin
15	VDD33	Supply	3.3V Voltage Supply
16	VSS33	Ground	Ground
17	XTAL32_OUT	I/O	Crystal Output
18	XTAL32_IN	I/O	Crystal Input
19	PD13_XTAL_OUT	I/O	General Purpose Digital I/O Pin/ Crystal Output
20	PD12_XTAL_IN	I/O	General Purpose Digital I/O Pin/ Crystal Input
21	PD11_NRST	I/O	General Purpose Digital I/O Pin/ Reset
22	PD10	I/O	General Purpose Digital I/O Pin
23	PD09	I/O	General Purpose Digital I/O Pin
24	PD08	I/O	General Purpose Digital I/O Pin
25	PD07	I/O	General Purpose Digital I/O Pin
26	PB11	I/O	General Purpose Digital I/O Pin
27	N.C.	-	No Connection
28	VCC	Supply	Gate Driver Voltage Supply
29	SGND	Ground	Logic Ground And Low-Side Gate Drivers Ground

Pin No.	Pin Name	Pin Type	Description
30	LOW	O	Phase-W Low-Side Gate Driver Output
31	LOV	O	Phase-V Low-Side Gate Driver Output
32	LOU	O	Phase-U Low-Side Gate Driver Output
33	N.C.	-	No Connection
34	VSW	Supply	Phase-W High-Side Driver Floating Supply Offset Voltage
35	HOW	O	Phase-W High-Side Driver Output
36	VBW	Supply	Phase-W High-Side Driver Floating Supply
37	N.C.	-	No Connection
38	VSV	Supply	Phase-V High-Side Driver Floating Supply Offset Voltage
39	HOV	O	Phase-V High-Side Driver Output
40	VBV	Supply	Phase-V High-Side Driver Floating Supply
41	N.C.	-	No Connection
42	VSU	Supply	Phase-U High-Side Driver Floating Supply Offset Voltage
43	HOU	O	Phase-U High-Side Driver Output
44	VBU	Supply	Phase-U High-Side Driver Floating Supply
45	N.C.	-	No Connection
46	PB03	I/O	General Purpose Digital I/O Pin
47	PB02	I/O	General Purpose Digital I/O Pin
48	PB01	I/O	General Purpose Digital I/O Pin

## 4.2 Signal Description

The following table describes the details on signals names classified by peripheral, some pins are not used in PT32M625.

Table 4-2 Alternate Function Description

Function Name	I/O	Function Description
<b>Universal Asynchronous Receiver/Transmitter (UART0, UART1), x = 0, 1</b>		
UARTx_TXD	O	UART x Data output pins
UARTx_RXD	I	UART x Data Input pins
UARTx_CTSn	I/O	UART x Clear to Send pins
UARTx_RTSn	I/O	UART x Request to Send pins
<b>Serial Wire Debug (SWD)</b>		
SWCLK	I	SWD Clock
SWDA	I/O	SWD Data Input/Output
<b>Inter Intergrated Circuit (I2C)</b>		
I2C_SDA	I/O	I2C Data
I2C_SCK	I/O	I2C Clock
<b>Serial Peripheral Interface (SPI)</b>		
SPI_MISO	I/O	SPI Master Input Slave Output
SPI_MOSI	I/O	SPI Master Output Slave Input
SPI_SCSN	I/O	SPI Chip Select
SPI_SCLK	I/O	SPI Clock
<b>General Purpose Input/Output (GPIO)</b>		
PA11-PA00	I/O	GPIO Port A
PB11-PB00	I/O	GPIO Port B
PC11-PC00	I/O	GPIO Port C
PD15-PD04	I/O	GPIO Port D
<b>Pulse Width Modulation (PWM0, PWM1, PWM2), x = 0, 1, 2</b>		
PWMx_A	O	PWM x Signals
PWMx_B	O	PWM x Signals
PWM_FAULT	I	PWM Fault Input
<b>General-Purpose Timer (GPT0, GPT1, GPT2), x = 0, 1, 2</b>		
CCPx_A	I/O	GPTimer x Compare and Capture A
CCPx_B	I/O	GPTimer x Compare and Capture B
<b>Analog to Digital Converter (ADC)</b>		
AD[7:0]	I	ADC Single End Channel Input / *ADC Differential Channel Input Positive or Negative Input

Function Name	I/O	Function Description
<b>Analog Comparator (AC0, AC1, AC2, AC3), x=0, 1, 2, 3</b>		
CAIPx	I	Comparator x Positive Input
CAINx	I	Comparator x Negative Input
<b>System Control (SC)</b>		
XTAL32_IN	I	32.768K RTC Clock Input
XTAL32_OUT	O	32.768K RTC Clock Output
XTAL_IN	I	High Speed 8MHZ Crystal Clock Input
XTAL_OUT	O	High Speed 8MHZ Crystal Clock Output
NRST	I	System Reset
WKUP	I	Wakeup
MCO	O	Microcontroller Clock Output
RTC_1HZ	O	RTC 1 Second Output

### 4.3 Multiplexing Pins Function Selection

The following tables describes PT32M625's microcontroller's available pin and its corresponding alternate function. The peripheral signals multiplexed to the GPIO lines. Alternate Function (AF) is enabled by configuring the **GPIOx\_AFRL** and **GPIOx\_AFRH** registers.

Note: In the microcontroller, all pins are in AF0 mode by default, with the exception of following cases:

- (1) Crystal Oscillator Pinout: Respective pins PD [15:11] are defaulted to the AF8 functionality.
- (2) Serial Wire Debug Interface Pinout: Respective PB [3:2] are defaulted to the AF6 functionality;
- (3) To enable PT32M625 gate driver functionality, PB [10:5] must be configured to AF7 (PWM signal).
- (4) Some pins are not available in PT32M625.

Table 4-3 Multiplexing Pins Function Selection

Pin Name	Alternate Functions								
	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8
PC06									
PC07									
PC08									
PC09									
PC10									
PC11									
PA00	PA00			SPI_MISO	PWM1_A	CCP1_A			AD0_CAIP0
PA01	PA01	UART0_RTS	I2C_SDA	SPI_MOSI	PWM1_B	CCP1_B	UART1_RXD		AD1_CAIN0
PA02	PA02		UART1_TXD	SPI_MISO	PWM2_A	CCP2_A			AD2_CAIP1
PA03	PA03		UART1_RXD	SPI_MOSI	PWM2_B	CCP2_B			AD3_CAIN1
PA04	PA04	UART1_TXD			PWM1_A	CCP1_A			AD4
PA05	PA05	UART1_RXD			PWM1_B	CCP1_B			AD5
PA06	PA06	UART1_CTS			PWM2_A	CCP2_A			AD6
PA07	PA07	UART1_RTS			PWM2_B	CCP2_B			AD7
PA08	PA08	UART1_TXD	I2C_SDA		PWM0_A	CCP0_A			CAIP2
PA09	PA09		UART1_RTS	SPI_SCSN	PWM0_B	CCP0_B			CAIN2
PA10	PA10								CAIP3
PA11	PA11								CAIN3
VDDA									
VSSA									
XTAL32_OUT									
XTAL32_IN									
PD13_XTAL_OUT	PD13								XTAL_OUT

Pin Name	Alternate Functions								
	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8
PD12_ XTAL_IN	PD12								XTAL_IN
PD11_NRST	PD11			SPI_SCSN	PWM_FALT	CCP1_B	PWM1_B		NRST
PD10	PD10				PWM_FALT				WKUP_V33
PD09	PD09			SPI_SCSN					
PD08	PD08			SPI_SCKK					
PD07	PD07								
PB11	PB11								
PB10	PB10			SPI_SCLK				PWM2_B*	
PB09	PB09			SPI_MISO				PWM1_B*	
PB08	PB08		UART1_TXD	SPI_MOSI	PWM_FALT			PWM0_B*	
PB07	PB07	I <sup>2</sup> C_SDA	UART1_RXD	SPI_SCSN	PWM2_B			PWM2_A*	
PB06	PB06	UART0_CTS	UART1_CTS	SPI_MOSI	PWM2_A	UART0_TXD	SWCLK	PWM1_A*	
PB05	PB05	UART0_RTS	UART1_RTS	SPI_MISO	PWM1_B	UART0_RXD	SWDA	PWM0_A*	
VDD33									
PB04									
PB03	PB03			SPI_MOSI		UART0_RXD	SWCLK		
PB02	PB02	UART0_CTS	I <sup>2</sup> C_SCK	SPI_SCKK	PWM1_A	CCP1_A	SWDA	MCO	
PB01	PB01	UART0_TXD	I <sup>2</sup> C_SCK	SPI_SCSN	PWM0_B	CCP0_B			
PB00	PB00	UART0_RXD	I <sup>2</sup> C_SDA	SPI_MISO	PWM0_A	CCP0_A			
PC00	PC00				PWM_FALT		RTC_1HZ	PWM2_B	
PC01	PC01							PWM1_B	
PC02	PC02							PWM0_B	
PC03									
PC04									
PC05									

Table 4-4 MCU-Driver internal connections

MCU PAD	I/O	Function	Gate Driver IC PAD	I/O	Function
PB05	I/O	PWM0_A	HIN1	I	1-Phase high-side gate driver input
PB06	I/O	PWM1_A	HIN2	I	2-Phase high-side gate driver input
PB07	I/O	PWM2_A	HIN3	I	3-Phase high-side gate driver input
PB08	I/O	PWM0_B	LIN1	I	1-Phase low-side gate driver input
PB09	I/O	PWM1_B	LIN2	I	2-Phase low-side gate driver input
PB10	I/O	PWM2_B	LIN3	I	3-Phase low-side gate driver input

## 5 Electrical Characteristics

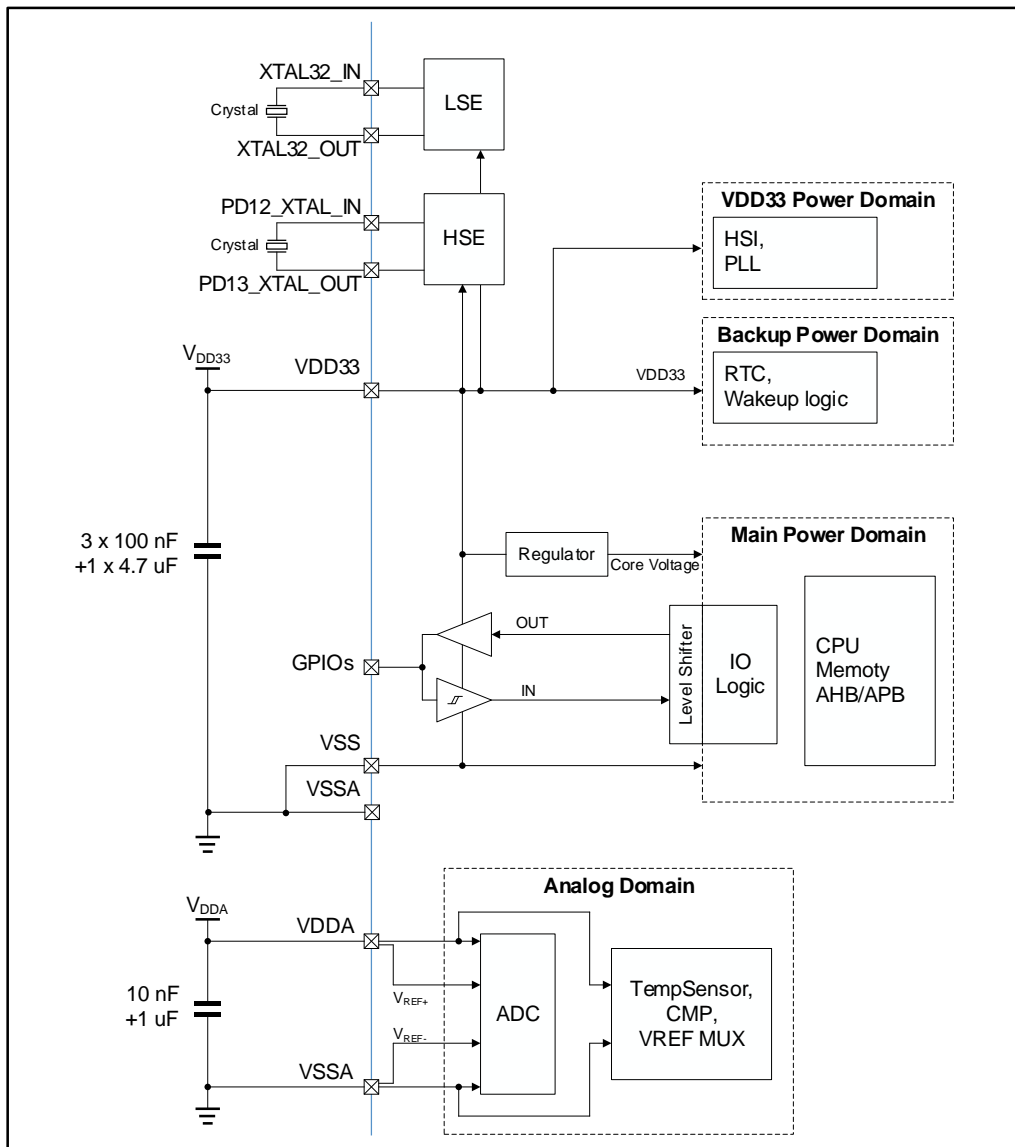
### 5.1 Parameter Conditions

#### 5.1.1 Minimum and Maximum Values, Typical Values

The minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at  $T_A = 25^\circ\text{C}$  and  $T_A = T_{A\text{MAX}}$  (given by the selected temperature range). Unless otherwise specified, typical data are based on  $T_A = 25^\circ\text{C}$ ,  $V_{\text{DD33}} = 3.3\text{V}(2.7\text{V} \leq V_{\text{DD33}} \leq 3.6\text{V})$ . They are given only as design guidelines and are not tested.

#### 5.1.2 Power Supply Scheme

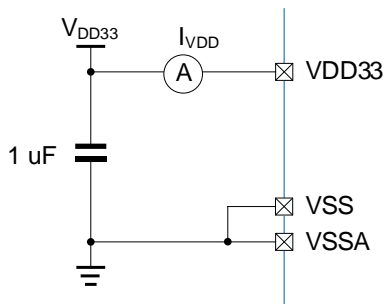
Figure 5-1 Power supply diagram



### 5.1.3 Current Consumption Measurement

When measuring the chip current, an ammeter can be connected in series between the VDD33 pin and the V<sub>DD33</sub> power supply for measurement. The wiring method is shown in the figure below. Before performing the measurement, you must turn off the all peripherals and ensure that the GPIO pin is not set to output mode. At the same time, remove all the loads of the chip including LED components, pull-up and pull-down resistors.

Figure 5-2 Current measurement method



## 5.2 Absolute Maximum Ratings

### 5.2.1 Ratings

Operation outside the Absolute Maximum Ratings may cause permanent device damage. These ratings are stress limits only, and functional operation of the device at these or any other conditions beyond those specified under Recommended Operating Conditions is not guaranteed. Operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings may impair device functionality, reliability, or longevity. All the voltage parameters are absolute voltages referenced to IC COM unless otherwise stated in the table.

Symbol	Parameter	Min.	Max.	Unit
$V_{DD}-V_{SS}$	$V_{DD}$ Supply Voltage	-0.3	3.6	V
$V_{IN}$	Input Voltage	-0.3	3.6	V
$ \Delta V_{DDH} $	Variations between different $V_{DDX}$ power pins of the same domain	—	50	mV
$ \Delta V_{SSH} $	Variations between all the different ground pins	—	50	
$I_{VDD}$	Total current into sum of all $V_{DD}$ power line	—	200	mA
$I_{VSS}$	Total current into sum of all $V_{SS}$ power line	—	200	
$I_{IO}$	Output current sunk by any I/O	—	15	
	Output current sourced by any I/O	—	15	
$T_{STG}$	Storage Temperature	-40	150	°C
$T_J$	Maximum junction temperature	—	150	
$V_{Bx}$	High-side floating supply voltage	$V_{Sx}-0.3$	$V_{Sx}+20$	V
$V_{Sx}$	High-side offset voltage	COM-6	COM+90	
$V_{HOx}$	High-side gate driver output voltage	$V_{Sx}-0.3$	$V_{Bx}+0.3$	
$V_{LOx}$	Low-side gate driver output voltage	COM-0.3	$V_{DD12}+0.3$	
$V_{HINx}$ $V_{LINx}$	Logic input voltage	-0.3	20	
$V_{DD12}$	Gate Driver supply voltage	-0.3	20	
$dV/dt$	Allowable offset voltage slew rate	—	50	

### 5.2.2 Electrical sensitivity

Based on three different tests (HBM, CDM, and LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

#### Electrostatic discharge (ESD)

Electrostatic discharges are applied to the pins of each sample according to each pin combination.

Symbol	Parameter	Conditions	Class	Max	unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	$T_A = +25\text{ }^\circ\text{C}$ , conforming to JEDEC EIA/JESD22-A114B	2	$\pm 2000$	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	$T_A = +25\text{ }^\circ\text{C}$ , conforms to JS-002-2018	C2b	$\pm 750$	

#### Static latch-up

Tests compliant with EIA/JESD78E latch-up standard are required to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin;
- A current injection is applied to each input, output and configurable GPIO pin.

Symbol	Parameter	Conditions	Level/Class
LU	Static latch-up	$T_A = +25\text{ }^\circ\text{C}$ , conforms to EIA/JESD78E	I level A ( $\pm 125\text{ mA}$ )

## 5.3 Operating Condition

### 5.3.1 General Operating Condition

All the electrical characteristics are applicable to the following conditions unless otherwise specified:

Symbol	Parameter	Conditions	Min.	Max.	Unit
f <sub>HCLK</sub>	Internal AHB clock frequency	—	0	48	MHz
f <sub>PCLK1</sub>	Internal APB1 clock frequency	—	0	48	
f <sub>PCLK2</sub>	Internal APB2 clock frequency	—	0	48	
V <sub>DD33</sub>	Standard operating voltage	—	2.7	3.6	V
V <sub>CC</sub>	Gate Driver supply voltage	—	5.5	18	V
V <sub>Sx</sub> <sup>(1)</sup>	High-side floating supply offset voltage	—	COM-6	60	V
V <sub>Bx</sub>	High-side floating supply voltage	—	V <sub>Sx</sub> +5.5	V <sub>Sx</sub> +18	V
V <sub>HOx</sub>	High-side gate driver output voltage	—	V <sub>S</sub>	V <sub>B</sub>	V
V <sub>LOx</sub>	Low-side gate driver output voltage	—	COM	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Ambient Temperature	—	-40	105	°C
T <sub>J</sub>	Junction temperature	—	-40	125	°C

Note(1): For V<sub>BS</sub>=15V, normal logic operation for V<sub>S</sub> is between COM-6V to 90V. High-side circuitry will sustain current state if V<sub>S</sub> is between COM-6V to COM-V<sub>BS</sub>. The parameter is only guaranteed by design.

Note: Functional operation is guaranteed only within the Recommended Operating Conditions. Operation outside this range may result in degraded performance, reduced reliability, or shortened lifetime of the device.

### 5.3.2 Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min.	Max.	Unit
t <sub>VDD</sub>	V <sub>DD</sub> rise time rate	Without capacity	0.5	∞	us/V
	V <sub>DD</sub> fall time rate		25	∞	

### 5.3.3 Power-on reset Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{PDR}/V_{POR}$	Power on/Power down reset threshold	Falling edge	1.88	1.888	1.9	V
		Rising edge	1.92	1.925	1.93	V
$V_{PDRhyst}$	PDR hysteresis	—	—	50	—	mV
$T_{RSTTEMPO}$	Reset temporization	—	1.5	2.2	4.7	mS
$V_{PVD}$	Programmable voltage detector (PVD) level selection	PLS[2:0]=000-110 (rising edge)	Reserved			V
		PLS[2:0]=000-110 (falling edge)	Reserved			V
		PLS[2:0]=111 (rising edge)	2.83	2.9	2.97	V
		PLS[2:0]=111 (falling edge)	2.73	2.8	2.87	V
$V_{PVDhyst}$	PVD hysteresis	—	—	100	—	mV

### 5.3.4 Supply current characteristics

This table shows the power consumption data under three different modes: Standby Mode, Sleep Mode, and Normal Mode.

Clock Enable	Frequency	Normal		Sleep Mode, LDO ON		Unit
		All IP Clock ON	All IP Clock OFF	All IP Clock ON	All IP Clock OFF	
LSI+HSI		1.819	1.393	1.343	0.858	mA
LSE+HSI		1.784	1.361	1.352	0.852	mA
HSI		1.779	1.352	1.368	0.864	mA
HSE+HSI		1.771	1.345	1.370	0.863	mA
PLL+HSI	4 MHz	2.357	1.949	1.951	1.447	mA
	8 MHz	3.413	2.575	2.559	1.550	mA
	16 MHz	5.502	3.835	3.767	1.753	mA
	32 MHz	8.947	5.596	6.184	2.156	mA
	48 MHz	12.608	7.625	8.428	2.448	mA
PLL+HSE	4 MHz	2.706	2.296	2.318	1.805	mA
	8 MHz	3.774	2.939	2.932	1.915	mA
	16 MHz	5.879	4.198	4.143	2.123	mA
	32 MHz	9.333	5.968	6.559	2.528	mA
	48 MHz	13.030	8.004	8.857	2.829	mA

Clock enable	Standby Mode, LDO OFF			unit
	RTC enable	RTC disable	All clock off	
LSI	2.959	2.877	2.140	mA
LSE	4.920	3.960		mA

### 5.3.5 Wakeup time from low-power modes and voltage scaling transition times

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t <sub>SLEEP</sub>	Wakeup time from Sleep mode	f <sub>HCLK</sub> = 16 MHz	—	129	—	μs
t <sub>STOP</sub>	Wakeup time from Stop1 mode	f <sub>HCLK</sub> = 16 MHz	—	153.3	—	μs
t <sub>STANDBY</sub>	Wakeup time from Standby mode	f <sub>HCLK</sub> = 16 MHz	—	158.3	—	us
t <sub>SHUTDOWN</sub>	Wakeup time from Shutdown mode	f <sub>HCLK</sub> = 16 MHz	—	4.96	—	ms

### 5.3.6 HSE 8 MHz XTAL Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f <sub>HSE</sub>	XTAL_IN frequency	—	4	8	24	MHz
V <sub>HSEH</sub>	XTAL_IN input pin high level voltage	—	0.7* V <sub>DD</sub>	—	V <sub>DD</sub>	V
V <sub>HSEL</sub>	XTAL_IN input pin low level voltage	—	V <sub>SS</sub>	—	0.3* V <sub>DD</sub>	V
t <sub>WIDTH(HSE)</sub>	XTAL_IN high level or low level time	8 MHz	—	62.5	—	ns
C <sub>in(HSE)</sub>	XTAL_IN input capacitance	8 MHz	—	5	—	pF
DUTY <sub>(HSE)</sub>	Duty cycle	—	40	—	60	%
I <sub>L</sub>	XTAL_IN Input leakage current	V <sub>SS</sub> ≤ V <sub>IN</sub> ≤ V <sub>DD</sub>	—	—	±1	μA

### 5.3.7 LSE 32 KHz XTAL Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f <sub>LSE</sub>	XTAL32_IN frequency	—	—	32.768	—	MHz
V <sub>LSEH</sub>	XTAL32_IN input pin high level voltage	—	0.7* V <sub>DD</sub>	—	V <sub>DD</sub>	V
V <sub>LSEL</sub>	XTAL32_IN input pin low level voltage	—	V <sub>SS</sub>	—	0.3*V <sub>DD</sub>	V
t <sub>WIDTH(LSE)</sub>	XTAL32_IN high level or low level time	—	12.2	—	18.3	ns
C <sub>in(LSE)</sub>	XTAL32_IN input capacitance	—	—	5	—	pF
DUTY <sub>(LSE)</sub>	Duty cycle	—	30	—	70	%

$I_L$	XTAL32_IN Input leakage current	$V_{SS} \leq V_{IN} \leq V_{DD}$	—	—	$\pm 1$	$\mu A$
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### 5.3.8 HSI 4 MHz RCOSC Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$f_{HSI}$	HSI CLK Frequency	$V_{DD} = 3.3V$ $T_A = 25^\circ C$	3.968	4	4.008	MHz
$ACC_{HSI}$	HSI accuracy	$V_{DD} = 3.3V$ $T_A = 25^\circ C$	-0.8	—	0.2	%
		$V_{DD} = 3.3V$ $T_A = -10^\circ C$ to $70^\circ C$	-1.4	—	0.2	%
		$V_{DD} = 3.3V$ $T_A = -40^\circ C$ to $85^\circ C$	-1.4	—	0.4	%
$D_{VDDH(HSI)}$	HSI oscillator frequency drift over VDD	$V_{DD} = 2.7$ to $3.3V$	-0.67	—	0.39	%
$t_{START(HSI)}$	HSI startup time	—	—	3.3	—	$\mu s$
$I_{DD}$	Power consumption	$V_{DD} = 3.3V$	91	92	94	$\mu A$

### 5.3.9 LSI 32 KHz RCOSC Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$f_{LSI}$	LSI CLK Frequency	$V_{DD} = 3.3V$ $T_A = 25^\circ C$	29.554	30	30.725	kHz
$ACC_{LSI}$	LSI accuracy	$T_A = 25^\circ C$	-2.7	—	2.4	%
		$T_A = -40$ to $105^\circ C$	-13.1	—	33.73	%
$t_{START(LSI)}$	LSI startup time	$V_{DD} = 3.3V$	—	73	—	$\mu s$
$I_{DD}$	Power consumption	$V_{DD} = 3.3V$	1	1.033	1.1	mA

### 5.3.10 Phase Locked Loop Characteristic

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$f_{PLL\_IN}$	PLL input clock	—	—	4	—	MHz
$f_{PLL\_OUT}$	PLL output clock	—	4	—	48	MHz
$t_{START(PLL)}$	PLL startup time	—	—	—	29.017	$\mu s$
$t_{LOCK}^{(1)}$	PLL lock time	—	—	—	30	$\mu s$
Jitter	PLL Period Jitter	$f_{PLL\_OUT} = 48MHz$ , RMS	—	88.8	—	ps
		$f_{PLL\_OUT} = 48MHz$ , P-P	—	0.564	—	ns
$I_{DD}$	Power consumption	—	7.094	7.347	7.186	mA

(1). Guaranteed by design.

## 5.3.11 I/O Pin Characteristics

## ◆ I/O static characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V <sub>IL</sub>	I/O Input low-level voltage	—	-0.3	—	0.8	V
V <sub>IH</sub>	I/O Input high-level voltage	—	2	—	3.6	V
I <sub>LOLEAK</sub>	I/O Input leakage current	—	—	—	±1	nA
R <sub>PU</sub>	Pull-up resistor	Weak pull-up equivalent resistor	34K	40K	77K	Ω
R <sub>PD</sub>	Pull-down resistor	Weak pull-down equivalent resistor	44K	54K	114K	Ω
V <sub>OL(DSR0)</sub>	Output low-level voltage	I <sub>IO</sub>  =3mA, V <sub>DD</sub> = 3.3V	—	—	0.4	V
V <sub>OH(DSR0)</sub>	Output high-level voltage	I <sub>IO</sub>  =3.2mA, V <sub>DD</sub> = 3.3V	V <sub>DD</sub> -0.4	—	—	V
V <sub>OL(DSR1)</sub>	Output low-level voltage	I <sub>IO</sub>  =6.12mA, V <sub>DD</sub> = 3.3V	—	—	0.4	V
V <sub>OH(DSR1)</sub>	Output high-level voltage	I <sub>IO</sub>  =6.2mA, V <sub>DD</sub> = 3.3V	V <sub>DD</sub> -0.4	—	—	V
V <sub>OL(DSR1)</sub>	Output low-level voltage	I <sub>IO</sub>  =15mA, V <sub>DD</sub> = 3.3V	—	—	2.4	V
V <sub>OH(DSR1)</sub>	Output high-level voltage	I <sub>IO</sub>  =19mA, V <sub>DD</sub> = 3.3V	V <sub>DD</sub> -2.4	—	—	V

## ◆ I/O AC characteristics

Symbol	Parameter	DS	Load	Condition	Typ.	Max.	Unit
f <sub>IOOUT_MAX</sub>	Maximum frequency	DS=0	C <sub>L</sub> =50pF	2.7V ≤ V <sub>DD</sub> < 3.3V	—	12	MHz
			C <sub>L</sub> =10pF	2.7V ≤ V <sub>DD</sub> < 3.3V	—	28	
		DS=1	C <sub>L</sub> =50pF	2.7V ≤ V <sub>DD</sub> < 3.3V	—	24	
			C <sub>L</sub> =10pF	2.7V ≤ V <sub>DD</sub> < 3.3V	—	48	
t <sub>ORISE</sub>	Output rise time	DS=0	C <sub>L</sub> =50pF	2.7V ≤ V <sub>DD</sub> < 3.3V	—	26.25	ns
			C <sub>L</sub> =10pF	2.7V ≤ V <sub>DD</sub> < 3.3V	—	9.96	
		DS=1	C <sub>L</sub> =50pF	2.7V ≤ V <sub>DD</sub> < 3.3V	—	12.24	
			C <sub>L</sub> =10pF	2.7V ≤ V <sub>DD</sub> < 3.3V	—	5.1	
t <sub>OFALL</sub>	Output fall time	DS=0	C <sub>L</sub> =50pF	2.7V ≤ V <sub>DD</sub> < 3.3V	—	27.65	ns
			C <sub>L</sub> =10pF	2.7V ≤ V <sub>DD</sub> < 3.3V	—	11.36	
		DS=1	C <sub>L</sub> =50pF	2.7V ≤ V <sub>DD</sub> < 3.3V	—	13.64	
			C <sub>L</sub> =10pF	2.7V ≤ V <sub>DD</sub> < 3.3V	—	5.7	
t <sub>OPULSE</sub>	Detects the pulse width EXTI			f <sub>HCLK</sub> = 48 MHz	41.67	—	ns

5.3.11.1 I/O output current (DS = 0)

Figure 5.3-1  $I_{OL}$  and  $V_{OL}$  @  $V_{DDH} = 3.3V, 3.6V, IO Drive = 2mA$

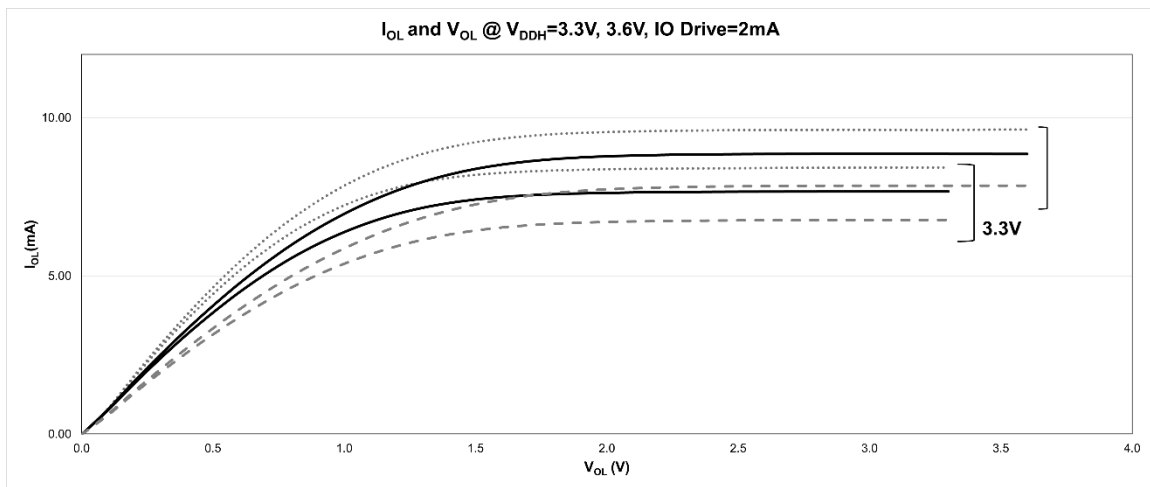
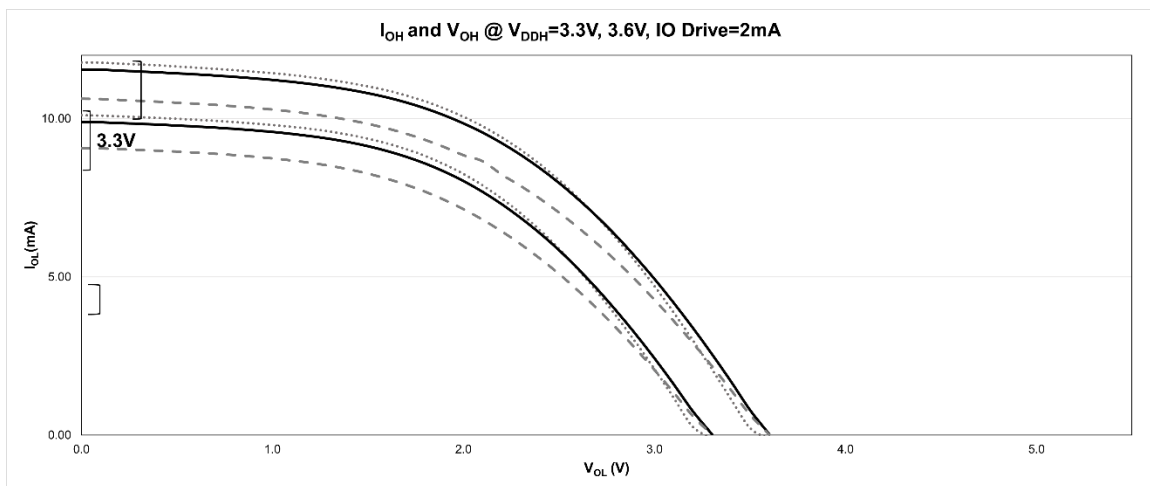


Figure 5.3-2  $I_{OH}$  and  $V_{OH}$  @  $V_{DDH} = 3.3V, 3.6V, IO Drive = 2mA$



5.3.11.2 I/O output current (DS = 1)

Figure 5.3-3  $I_{OL}$  and  $V_{OL}$  @  $V_{DDH} = 2.2V, 3.3V, 3.6V, IO Drive = 4 mA$

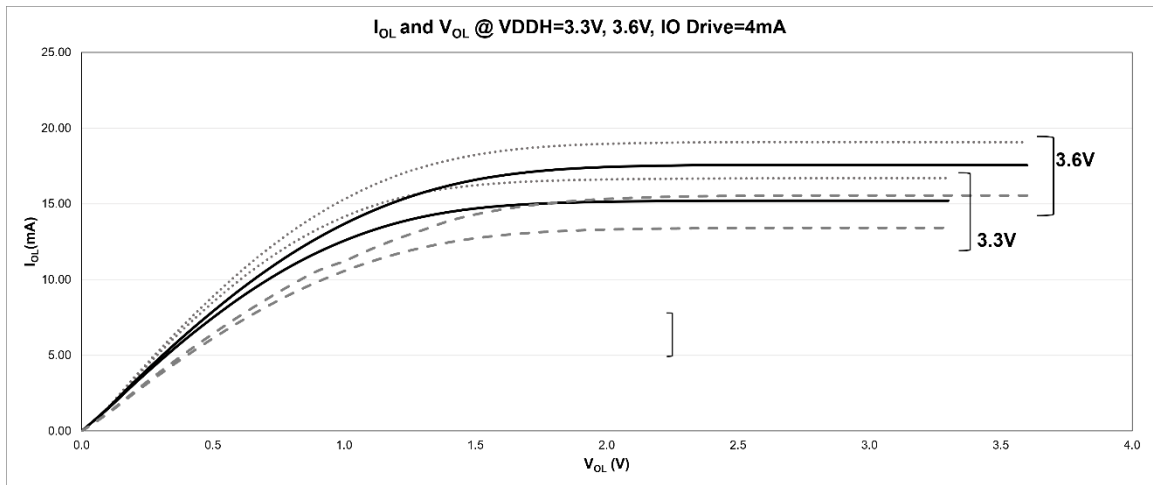
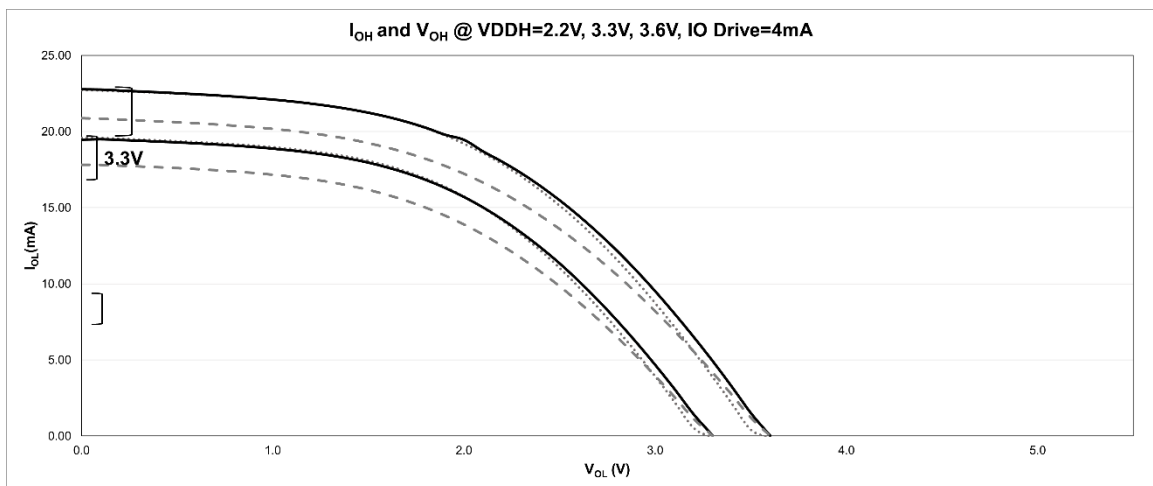


Figure 5.3-4  $I_{OH}$  and  $V_{OH}$  @  $V_{DDH} = 3.3V, 3.6V, IO Drive = 4mA$



## 5.3.12 NRST Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{IL(NRST)}^{(1)}$	NRST Input low level voltage	—	-0.5	—	0.8	V
$V_{IH(NRST)}$	NRST Input high level voltage	—	2	—	$V_{DD} + 0.5$	
$V_{hys(NRST)}^{(1)}$	NRST Schmitt trigger voltage hysteresis	—	—	200	—	mV
$R_{PU}$	Weak pull-up equivalent resistor <sup>(1)</sup>	$V_{IN} = V_{SS}$	30	40	50	k $\Omega$
$V_{F(NRST)}^{(1)}$	NRST Input filtered pulse	—	—	—	100	ns
$V_{NF(NRST)}^{(1)}$	NRST Input not filtered pulse	—	300	—	—	ns
$t_{NRSTPL}$	NRST internal reset pulse duration	$C_L = 0.1\mu$	—	2.7	—	ms

(1). The pull-up is designed with a true resistance in series with a switchable PMOS. THSI PMOS contribution to the series resistance must be minimum (~10% order)

## 5.3.13 Timer Characteristics

Symbol	Parameter	Conditions	Min.	Max.	Unit
$t_{RES(TIMER)}$	Timer resolution	$f_{APB1}$ prescaler = 1	1	—	$f_{TIMERCLK}$
		$f_{TIMERCLK} = 48$ MHz	20.83	—	ns
$t_{EXT(TIMER)}$	Timer input signal frequency	—	—	$f_{TIMERCLK}/2$	MHz
		$f_{TIMERCLK} = 48$ MHz	0	48	MHz
$t_{COUNTER}$	16 bit counter	—	1	$2^{16}$	$f_{TIMERCLK}$
		$f_{TIMERCLK} = 48$ MHz	—	1.365	ms
	32 bit counter	—	1	$2^{32}$	$f_{TIMERCLK}$
		$f_{TIMERCLK} = 48$ MHz	—	89.48	s

## 5.3.14 ADC Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V <sub>DDA</sub>	Analog supply voltage	—	2.7	—	3.6	V
V <sub>REFP</sub>	Reference voltage		V <sub>SSA</sub>	—	V <sub>DDA</sub>	V
I <sub>ADC</sub>	Supply current (ADC+PGA)	—	—	3.5	—	mA
f <sub>ADC</sub>	ADC Clock frequency	—	—	24	48	MHz
f <sub>s</sub>	Sample rate	—	—	1.2	2.4	MHz
V <sub>AIN</sub>	ADC input voltage	—	0	—	V <sub>REFP</sub>	V
R <sub>AIN</sub>	External input impedance	—	—	—	240	Ω
R <sub>ADC</sub> <sup>(1)</sup>	Sample switch impedance	f <sub>ADC</sub> = 24 MHz	—	—	1.507	KΩ
C <sub>ADC</sub>	Internal sample and hold capacitor	—	—	15.88	—	pF
t <sub>START</sub> <sup>(2)</sup>	ADC startup time	—	1			Conversion On cycle
t <sub>s</sub>	Sample time	f <sub>ADC</sub> = 24 MHz	—	0.25	—	us
		—	—	6	—	1/f <sub>ADC</sub>
t <sub>conv</sub>	Total conversion time (include sample time)	f <sub>ADC</sub> = 24 MHz	—	0.083	—	us
ERR <sub>DNL</sub>	Differential nonlinearity error	f <sub>ADC</sub> = 24 MHz V <sub>DDA</sub> = 3.3V	—	±1.5	—	LSB
ERR <sub>INL</sub>	Integral nonlinearity error	f <sub>ADC</sub> = 24 MHz V <sub>DDA</sub> = 3.3V	—	±4.7	—	LSB

$$(1) R_{AIN} = \frac{T_s}{f_{ADC} \times C_{ADC} \times \ln(2^{N+1})} - R_{ADC}$$

(2) Guaranteed by design.

## 5.3.15 Comparator Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V <sub>DDA</sub>	Analog supply voltage	—	2.7	—	3.6	V
V <sub>IN</sub>	Analog supply voltage	—	0	—	V <sub>DDA</sub>	V
t <sub>START</sub>	Startup time	—	—	1.02	—	μs
V <sub>OFFSET</sub>	Comparator offset	AC1, V <sub>DDA</sub> =3.3V	-8	—	8	mV
		AC2, V <sub>DDA</sub> =3.3V	-1	—	6	mV
		AC3, V <sub>DDA</sub> =3.3V	-5	—	10	mV
		AC4, V <sub>DDA</sub> =3.3V	6	—	10	mV
t <sub>d</sub>	Propagation Delay	—	—	1.2	—	μs
I <sub>CMP</sub>	Current Consumption	CAON<3:0> = 1111	456	488	550	μA

## 5.3.16 Temperature Sensor Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V <sub>DDA</sub>	Analog supply voltage	—	2.7	—	3.6	V
T <sub>L</sub>	Linearity of temperature	—	—	—	±7	°C
Avg_Slope	Average slope	—	3.663	—	3.868	mV
V <sub>TSENSE30</sub>	Voltage at 30°C (±7 °C)	—	1.051	1.094	1.117	V
T <sub>START</sub>	Start-Up Time	—	—	—	50	μs
t <sub>s_TSENSE</sub>	ADC sampling time when reading the temperature	—	5	—	—	μs
I <sub>TENSE</sub>	Current Consumption	—	70	100	160	μA

### 5.3.17 3-Phase Gate Driver Static Electrical Characteristics

(VCC-COM)= (VB-VS) =15V. Ambient temperature TA=25°C unless otherwise specified. The VIN, TH, VI, and IIN Parameters are reference to COM and are applicable to all channels. The VO and IO parameters are referenced to COM and are applicable to the respective output leads. The VCCUV parameters are referenced to COM. The VBSUV parameters are referenced to VS.

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
<b>Low Side Power Supply Characteristics</b>						
Quiescent VCC supply current	I <sub>QVCC1</sub>	V <sub>HIN1,2,3</sub> =V <sub>LIN1,2,3</sub> =0 or 5V, V <sub>ENB</sub> =0	210	330	450	μA
Quiescent VCC supply current in standby mode	I <sub>QVCC2</sub>	V <sub>HIN1,2,3</sub> =V <sub>LIN1,2,3</sub> =0 or 5V, V <sub>ENB</sub> =5	-	46	80	
operating VCC supply current	I <sub>VCCOP</sub>	f <sub>LIN1,2,3</sub> =20KHz, f <sub>HIN1,2,3</sub> =20KHz,	-	1500	-	
VCC supply under-voltage positive going threshold	V <sub>CCUV+</sub>	-	2.9	4.2	5.5	V
VCC supply under-voltage negative going threshold	V <sub>CCUV-</sub>	-	2.5	3.8	5.1	
VCC supply under-voltage lockout hysteresis	V <sub>CCHYS</sub>	-	-	0.4	-	
<b>High Side Floating Power Supply Characteristics</b>						
High side VBS supply under-voltage positive going threshold	V <sub>B SUV+</sub>	-	2.5	3.8	5.5	V
High side VBS supply under-voltage negative going threshold	V <sub>B SUV-</sub>	-	2.2	3.5	4.8	
High side VBS supply under-voltage lockout hysteresis	V <sub>B SUVHYS</sub>	-	-	0.3	-	
High side quiescent VBS supply current	I <sub>QBS</sub>	V <sub>BS</sub> =15V	25	45	65	μA
Offset supply leakage current	I <sub>LK</sub>	V <sub>B</sub> =V <sub>S</sub> =100V V <sub>CC</sub> =0V	-	-	10	
<b>Gate Driver Output Section</b>						
High side output HIGH short-circuit pulse current	I <sub>HO+</sub>	V <sub>HO</sub> =V <sub>S</sub> =0	-	1.2	-	A
High side output LOW short-circuit pulse current	I <sub>HO-</sub>	V <sub>HO</sub> =V <sub>B</sub> =15V	-	2.0	-	
Low side output HIGH short-circuit pulse current	I <sub>LO+</sub>	V <sub>LO</sub> =0	-	1.2	-	
Low side output LOW short-circuit pulse current	I <sub>LO-</sub>	V <sub>LO</sub> =V <sub>CC</sub> =15V	-	2.0	-	
Allowable negative VS voltage for HIN1,2,3 signal propagation to HO1,2,3	V <sub>SN</sub>	V <sub>BS</sub> =15V	-	-8	-	V

Note: V<sub>IH1,2,3</sub> and V<sub>LIN1,2,3</sub> are SIP connected internally, V<sub>ENB</sub> is internal pull low.

### 5.3.18 3-Phase Gate Driver Dynamic Electrical Characteristics

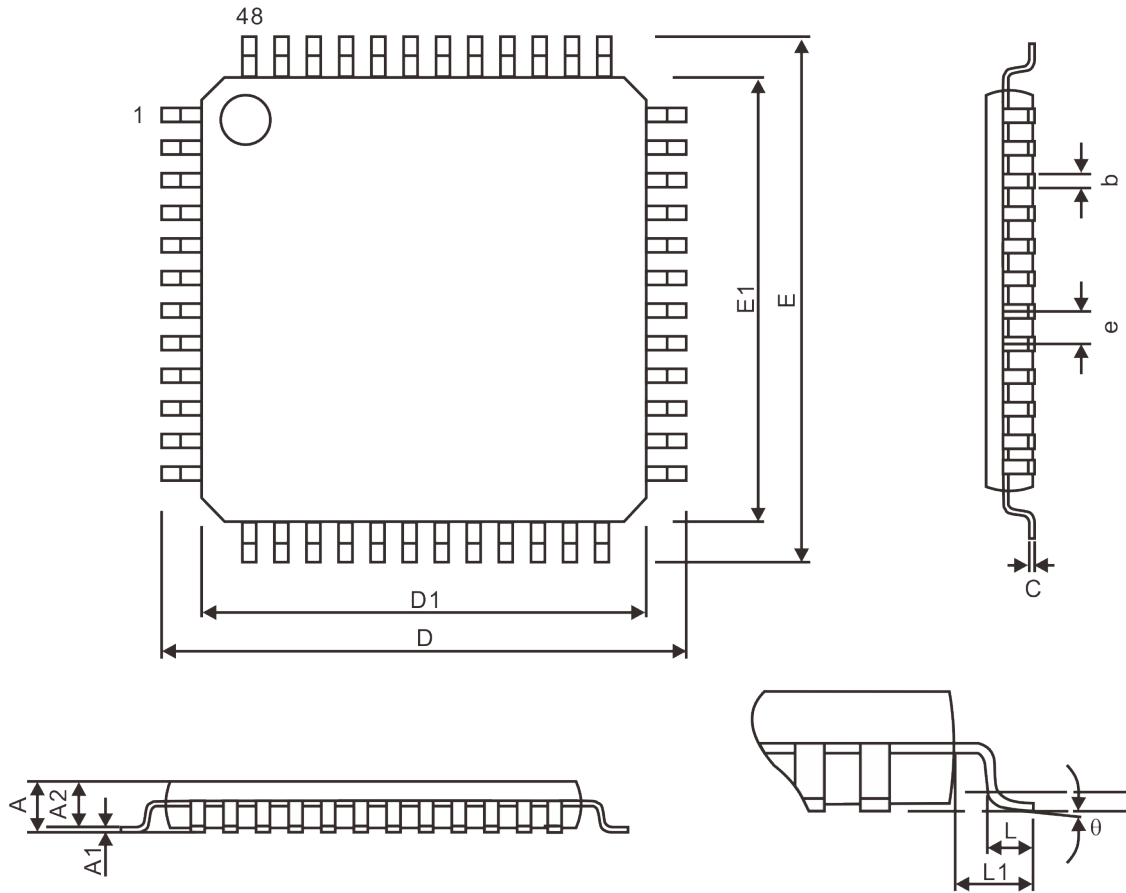
(VCC-COM)= (VB-VS) =15V , $V_{SU,V,W}=COM$ , and  $C_{load}=1nF$  unless otherwise specified, ambient temperature  $T_A=25^{\circ}C$ .

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Turn-on propagation delay	$t_{on}$	$V_{HIN1,2,3}$ or $V_{LIN1,2,3}=5V$ , $V_{SU,V,W}=0$	-	120	200	ns
Turn-off propagation delay	$t_{off}$	$V_{HIN1,2,3}$ or $V_{LIN1,2,3}=0$ , $V_{SU,V,W}=0$	-	120	200	
Turn-on rise time	$t_r$	$V_{HIN1,2,3}$ or $V_{LIN1,2,3}=5V$ , $V_{SU,V,W}=0$	-	37	-	
Turn-off fall time	$t_f$	$V_{HIN1,2,3}$ or $V_{LIN1,2,3}=0$ , $V_{SU,V,W}=0$	-	30	-	
Dead time	DT	$V_{HIN1,2,3}$ or $V_{LIN1,2,3}=0$ and 5V, without external dead time	300	500	700	
Dead time matching (all six channels)	MDT	without external dead time	-	-	50	
Delay matching (all six channels)	MT	external dead time > 1000ns	-	-	50	
Output pulse-width matching	PM	external dead time > 1000ns, $PW_{IN}=10\mu s$ , $PM=PW_{OUT}-PW_{IN}$	-	-	50	

## 6 PACKAGE INFORMATION

### 6.1 LQFP48 (7x7 mm) Package information

Figure 6-1 LQFP48 (7x 7mm) package outline

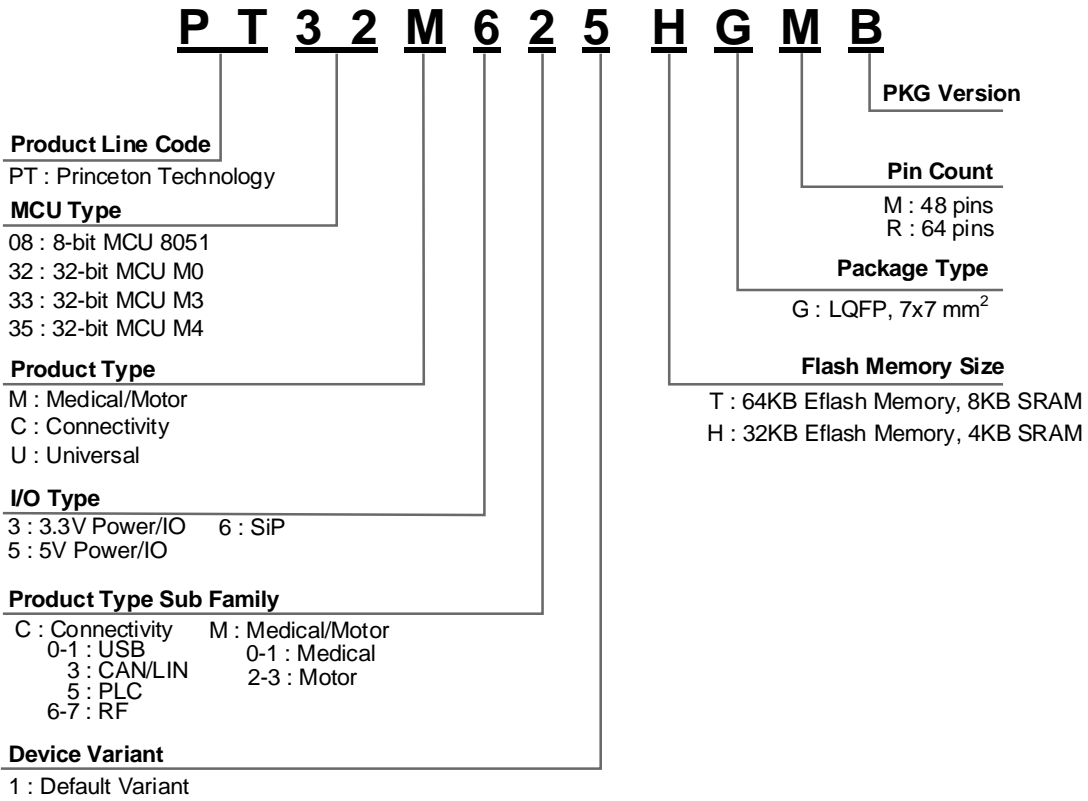


Symbol	Dimensions (mm)		
	Min.	Nom.	Max.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	-	0.20
D	9.00 BSC		
D1	7.00 BSC		
E	9.00 BSC		
E1	7.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

Note: Refer to JEDEC MS-026 BBC

# 7 ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT32M625	LQFP 48	PT32M625 HGMB



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## 8 REVISION HISTORY

Date	Revision	Reference No.	Modification
	PT32M625 PRE1.0	MAC1712001	Initial Version
2020/04/20	PT32M625 V1.0	MAC2004005	
2022/06/10	PT32M625 V1.1	MAC2207019	<ol style="list-style-type: none"> <li>1. Page5: modified Serial Wire Debug Interface Pinout: Respective PB [3:2] are defaulted to the AF6 functionality</li> <li>2. update page.306 block diagram.</li> <li>3. Remove page.308 4.15.1.6 STANDBY MODE</li> <li>4. update page.274 4.14.2.1 SCKDV from 4 to 2. And Register SPI_BR_SL</li> <li>5. Modified page 218 CLKSEL and MODSEL data.</li> <li>6. Modified page 219 watch dog address error.</li> <li>7. Modified page 43/ page 309 Operating Ambient Temperature from 85 to 105</li> </ol>
2024/10/17	PT32M625 V1.2	MAC2410004	<ol style="list-style-type: none"> <li>1. Modified the title of <a href="#">Section 4.15</a></li> <li>2. Modified the title of <a href="#">chapter 5</a> and <a href="#">chapter 6</a></li> <li>3. Modified the typo error in <a href="#">Section4</a></li> </ol>
2025/6/19	PT32M625 V1.3	MAC2506007	<ol style="list-style-type: none"> <li>1. Adjust the document content to separate the datasheet and reference manual data into two separate documents.</li> <li>2. Modified CH5 Electrical Characteristics to match actual test values.</li> </ol>