DESCRIPTION

The PT4304 is a fully integrated OOK/ASK receiver for the 315 / 433.92 MHz frequency bands requiring few external components. The PT4304 receiver chain consists of a low-noise amplifier (LNA), image-rejection mixer (IRM), built-in channel-select filter (CSF), OOK/ASK demodulator, data filter, and data slicing comparator. The local oscillator (LO) sub-system incorporates a monolithic VCO, ÷ 32 feedback divider, loop filter and fast start-up reference oscillator to form a complete phase-locked loop-based frequency synthesizer for single channel applications. The PT4304 also includes an on-chip voltage regulator.

The PT4304 is available in a 16-pin SSOP package and is specified over the temperature range from –40 to +85 °C.

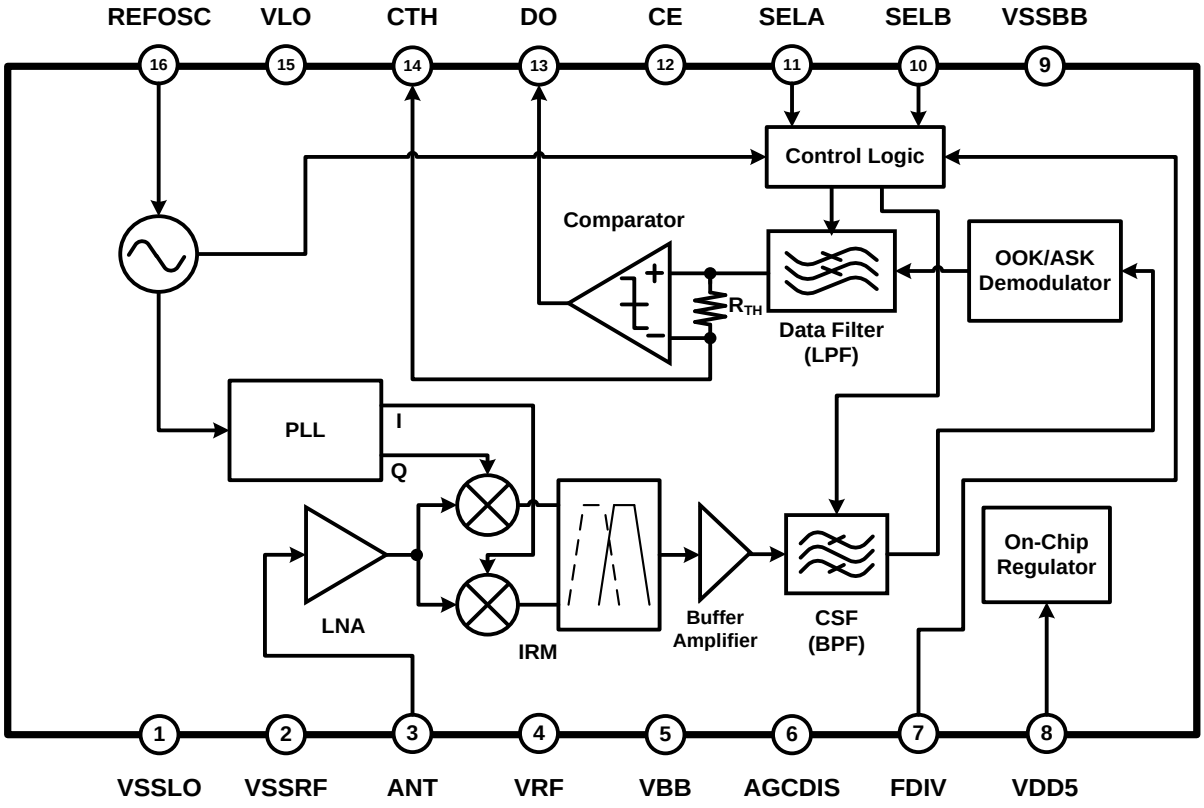
FEATURES

- Covers 315 and 433.92 MHz frequency bands
- Low power consumption: 4.3 mA for 315 MHz band and 4.6 mA for 433.92 MHz band under normal operating conditions
- Requires few external components
- Achieves excellent sensitivity on the order of –114 dBm for 315 MHz band and –112 dBm for 433.92 MHz band (peak ASK signal level)
- Supply voltage range: 2.4 to 5.5 V
- Supports data rates up to 10 Kb/s
- Wide input dynamic range with automatic gain control handling

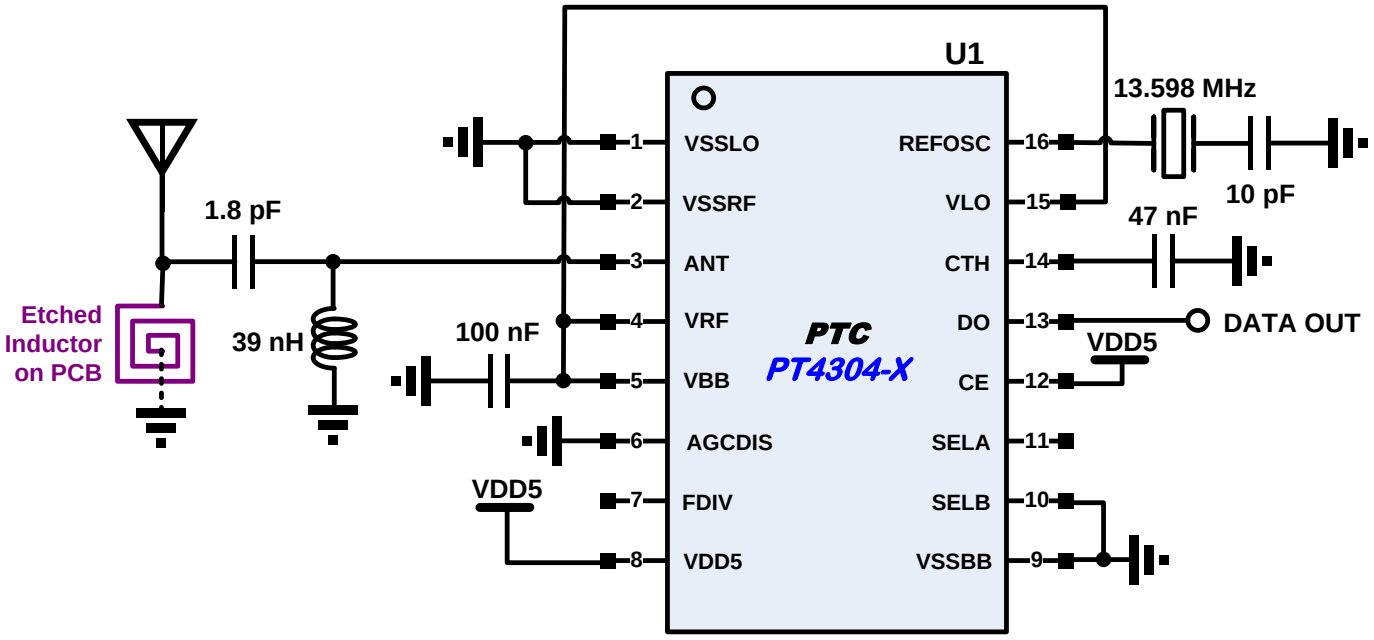
APPLICATIONS

- Automotive Remote Keyless Entry (RKE)
- Remote control
- Garage door and gate openers
- Suitable for applications that must adhere to either the European ETSI-300-220 or the North American FCC (Part 15) regulatory standards

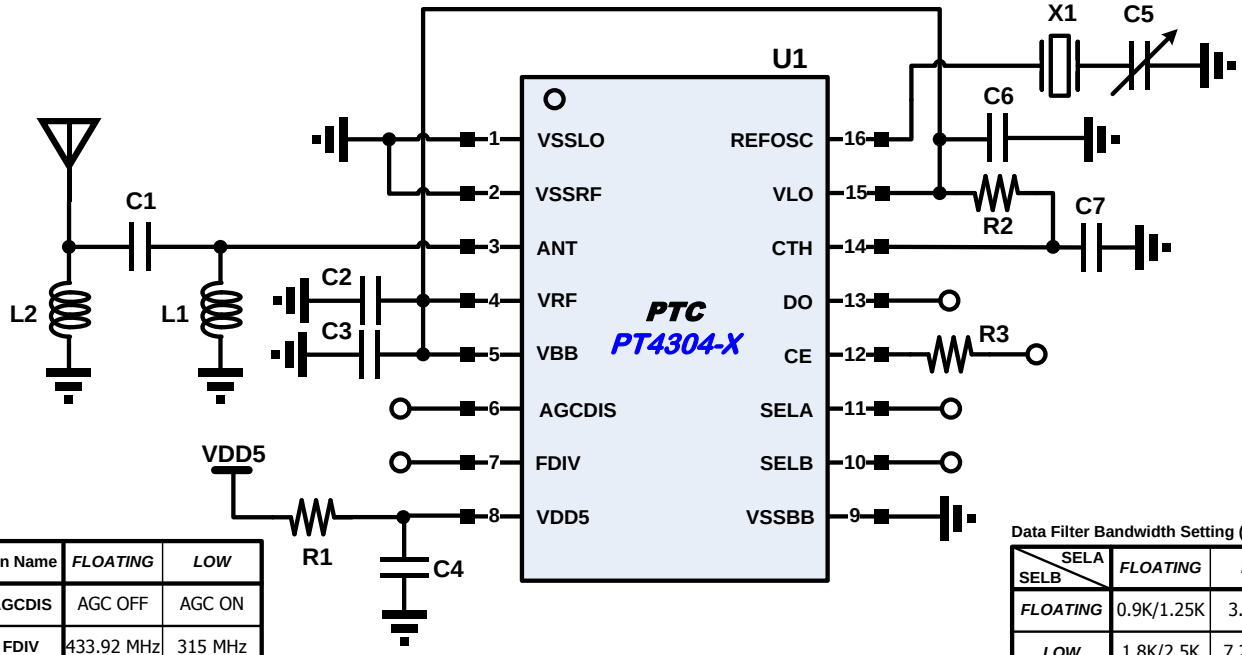
BLOCK DIAGRAM



433.92 MHZ APPLICATION EXAMPLE



EVALUATION BOARD SCHEMATIC



Pin #	Pin Name	*FLOATING*	*LOW*
6	AGCDIS	AGC OFF	AGC ON
7	FDIV	433.92 MHz	315 MHz

Data Filter Bandwidth Setting (Unit: Hz)

SELB \ SELA	*FLOATING*	*LOW*
FLOATING	0.9K/1.25K	3.6K/5K
LOW	1.8K/2.5K	7.2K/10K

BILL OF MATERIALS

Part	Value		Unit	Description
	315 MHz	433.92 MHz		
L1	68 n	39 n	H	Antenna input matching, coil inductor
L2	82 n	56 n	H	Antenna ESD protection, coil inductor (optional)
C1	1.8 p	1.5 p	F	Antenna input matching
C2/C3/C4/C6	100 n	100 n	F	Power supply de-coupling capacitor
C5	10 p	10 p	F	Dependent upon crystal oscillator vendor; for frequency fine-tuning (optional)
C7	47 n	47 n	F	C_{TH}, affects coding type and start-up time
R1	10	10	Ω	Power supply de-coupling resistor (optional)
R2	8.2 M	8.2 M	Ω	For reducing data output noise (optional)
R3	10 K	10 K	Ω	MCU interface resistor (optional)
X1	9.882	13.598	MHz	Crystal with C_{Load} = *10 pF*, for reference oscillator
U1	PT4304 IC	PT4304 IC	U1	Receiver chip

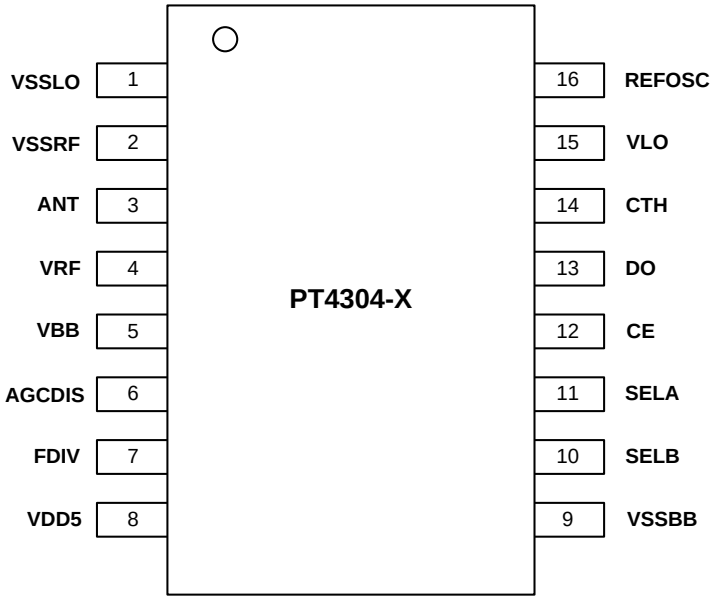
Notes:

1. L1 and C1 are the components for input matching network. They may need to be adjusted for different PCB layout and antenna requirements.
2. The value of C7 depends upon the data rate and coding pattern.
3. The *optional* components may be used depending upon specific application requirements.

ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT4304-X	16 Pins, SSOP, 150 mil	PT4304-X

PIN CONFIGURATION



PIN DESCRIPTION

Pin No.	Pin Name	I/O	Description
1	VSSLO	G	Ground for LO sub-system
2	VSSRF	G	Ground for RF front-end
3	ANT	I	RF input connected to antenna via a matching network
4	VRF	P	Supply voltage for RF front-end
5	VBB	P	Supply voltage for baseband chain
6	AGCDIS	I	AGC control pin (tie LOW to enable AGC)
7	FDIV	I	RF frequency band select
8	VDD5	P	5 V regulator input
9	VSSBB	G	Ground for baseband chain
10	SELB	I	Data filter bandwidth select (pin B)
11	SELA	I	Data filter bandwidth select (pin A)
12	CE	I	Chip enable (tie HIGH to enable the chip)
13	DO	O	Data output
14	CTH	I/O	Connection for data slicing threshold capacitor
15	VLO	P	Supply voltage for LO sub-system
16	REFOSC	I	Reference oscillator input

FUNCTION DESCRIPTION

POWER SUPPLY

The PT4304 provides an internal voltage regulator to supply all receiver blocks. Hence, all the supply voltage pins, except VDD5, are to be connected together. Bypass capacitors should be placed as close as possible to the supply voltage pins. The VDD5 pin (pin 8) should connect to the external supply voltage and should incorporate series-R, shunt-C filtering. The PT4304 chip can operate in the supply voltage range from 2.4 V to 5.5 V.

RF FRONT-END

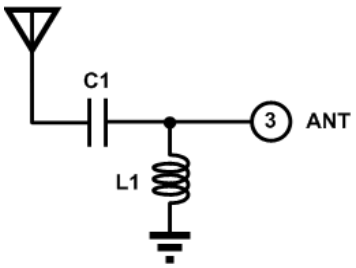
The RF front-end of the receiver employs a super-heterodyne configuration that down-converts the input radio frequency (RF) signal to an intermediate frequency (IF) signal. According to the block diagram, the RF front-end consists of an LNA and an image rejection down-conversion mixer, and the in-phase (I) and quadrature (Q) local oscillator (LO) signals for the mixer are generated from the PLL frequency synthesizer.

A special feature of the PT4304 is its integrated double-balanced image-rejection mixer (IRM), which eliminates the need for a costly front-end SAW filter for many applications. The advantages of not using a SAW filter include simplified antenna matching, less board space, and lower BOM cost. The mixer cell consists of a pair of double-balanced mixers that perform an I-Q down-conversion of the RF input to the IF band with high-side injection (i.e. $f_{RF} = f_{LO} - f_{IF}$). The image-rejection circuit then combines these signals to achieve an image-rejection ratio typically over 30 dB. High-side injection is mandatory (e.g. low-side injection may not be selected) due to the nature of the on-chip image rejection implementation. The IF output of IRM is connected to a buffer amplifier to drive the succeeding IF-band, channel-select filter (CSF).

The RF front-end provides the good low-noise performance (NF < 5 dB), high voltage conversion gain (> 45 dB), and excellent reversion isolation.

The ANT pin can be matched to 50 Ohm with an L-type circuit shown in the figure below. Inductor and capacitor values may be different from table depending on PCB material, PCB thickness, ground configuration, and the length of traces used in the layout.

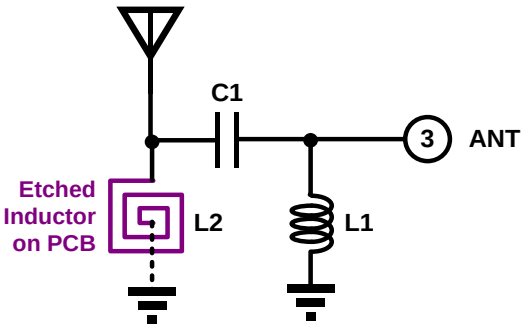
Example of the input-matching network is shown in the following figure and the input impedances of the PT4304 for 315/433.92 MHz frequency bands are listed in the right-hand side table. Please note that the component values given in the BOM for the application circuit shown on Page 3 are nominal values only.



RF Frequency f_{RF}	ANT Input Impedance (Pin 3)
315 MHz	2.404 − j256.59 Ω
433.92 MHz	3.096 − j181.16 Ω

ANTENNA PIN ESD PROTECTION

The PT4304 IC provides the ESD protection level (Human Body Mode) better than 4 KV at the ANT pin. However, higher ESD protection level may still be required at the system level for some applications. Achieving an enhanced ESD protection level may need to rely on the external components. Changing L1 from SMD type to coil type could enhance ESD protection level up to 1 KV, and adding a shunt coil inductor L2 (can either use an etched inductor on PCB) in front of C1 may help to further improve ESD protection.



RF Frequency f_{RF}	Suggestion value of L2
315 MHz	82 nH
433.92 MHz	56 nH

REFERENCE OSCILLATOR

All timing and tuning operations on the PT4304 are derived from the internal one-pin Colpitts reference oscillator. Timing and tuning functions are provided by the REFOSC pin in one of two ways:

1. Connect a crystal
2. Drive this pin with an external timing signal

When a crystal is used, the minimum oscillation voltage swing is 300 mV_{PP}. If using an externally applied signal, the signal source should be AC-coupled and its input swing should be limited to the operating range from 0.6 V_{PP} to 2.0 V_{PP}.

As with any super-heterodyne receiver, the mixing product between the internal LO (local oscillator) frequency, f_{LO}, and the incoming transmit frequency, f_{TX}, must ideally equal the IF center frequency, f_{IF}. The following equations may be used to compute the appropriate f_{LO} for a given f_{TX}:

$f_{LO} = f_{TX} \times (352 / 351)$ for 433.92 MHz band and $f_{LO} = f_{TX} \times (256 / 255)$ for 315 MHz band.

Hence, $f_{IF} = f_{TX} \div 351$ for 433.92 MHz band and $f_{IF} = f_{TX} \div 255$ for 315 MHz band.

Using the above equations, frequencies f_{TX} and f_{LO} are computed in MHz. High-side LO injection results in an image frequency above the frequency of interest. For a given value of f_{LO}, the equation below may be used to compute the reference oscillator frequency, f_{REFOSC}:

$f_{REFOSC} = f_{LO} \div 32$.

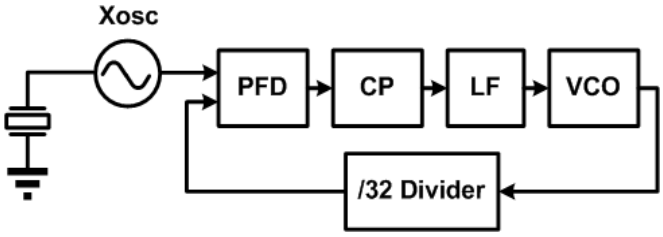
The following table specifies f_{REFOSC} for two common transmit frequencies for the PT4304 chip (high-side LO mixing).

Transmit Frequency f_{TX}	FDIV	Reference Oscillator Frequency f_{REFOSC}
315 MHz	LOW	9.882 MHz
433.92 MHz	FLOATING	13.598 MHz

PHASE-LOCKED LOOP (PLL)

The PT4304 utilizes an integer-N PLL to generate the receiver LO. The PLL consists of a voltage-controlled oscillator (VCO), reference crystal oscillator, asynchronous ÷ 32 fixed-modulus divider, charge pump, loop filter and phase-frequency detector (PFD). All components are integrated on-chip. The PFD compares two signals and produces an error signal that is proportional to the difference between the input signal phases. The error signal passes through a loop filter that provides a loop bandwidth of approximately 200 KHz, and is used to control the VCO. The VCO output frequency is fed back through the fixed-modulus frequency divider to one input of the PFD. The other input to the PFD comes directly from the reference crystal oscillator. Thus, the VCO output frequency, which is used as the LO frequency, is phase-locked to the reference frequency and $f_{REFOSC} = (f_{TX} + f_{IF}) \div 32 = f_{LO} \div 32$.

The block diagram below illustrates the basic elements of the PLL.



CHANNEL-SELECT FILTER

PT4304 embeds a channel-select filter (CSF) with a bandwidth of approximately 380 KHz. The CSF utilizes a sixth-order active filter for the low-IF architecture. An automatic frequency tuning circuit is also included on-chip and its absolute reference clock is derived from the reference crystal oscillator. The automatic frequency tuning circuit centers the pass-band of the CSF at the IF frequency (f_{IF}).

ASK DEMODULATOR

The OOK/ASK demodulation is done by comparing the received signal strength indicator (RSSI) signal level. The RSSI signal is decimated and filtered in the data filter and the data decision is then completed by the slicing comparator.

The RSSI is implemented as a successive compression log amplifier following by the internal CSF. The log amplifier achieves ±3 dB log linearity; the RSSI output level has the dynamic range of around 60 dB without turning on the automatic gain control (AGC) circuitry and of over 85 dB when the AGC circuitry is turned-on. The RSSI slope is approximately 11 mV /dB.

DATA FILTER

The data filter (post-demodulator filter) is utilized to remove additional unwanted spurious signals after the OOK/ASK demodulator. The data filter is implemented as a 2nd-order low-pass Sallen-Key filter. The data filter bandwidth (BW_{DF}) must be selected according to the application requirement, and should be set according to the equation

BW_{DF} = 0.65 / Shortest pulse-width

The input pins of SELA and SELB control the data filter bandwidth in four binary steps as shown in the table below. Please note that the values indicated in this table are nominal values. The filter bandwidth scales linearly with frequency so the exact value will depend on the operating frequency.

SELA	SELB	Data Filter Bandwidth BW_{DF}	
		f_{RF} = 315 MHz	f_{RF} = 433.92 MHz
FLOATING	FLOATING	900 Hz	1250 Hz
FLOATING	LOW	1800 Hz	2500 Hz
LOW	FLOATING	3600 Hz	5000 Hz
LOW	LOW	7200 Hz	10000 Hz

DATA SLICER

The purpose of the data slicer is to take the analog output of the data filter and convert it to a digital signal. Extraction of the DC value of the demodulated signal for purposes of logic-level data slicing is accomplished using the external threshold capacitor C_{TH} and the on-chip resistor R_{TH}, shown in the block diagram. Slicing level time constant values vary somewhat with decoder type, data pattern, and data rate, but typical values range from 2 ms to 20 ms. Optimization of the value of C_{TH} is required to maximize range.

The first step in the process is selection of a data-slicing-level time constant. This selection is strongly dependent on system issues including system decode response time and data code structure. The effective resistance of R_{TH} is 32.5 KΩ and a τ of 3x the period of longest "LOW" or "HIGH" bit stream is recommended. Assuming that a slicing level time constant τ has been established, capacitor C_{TH} may be computed using equation

$C_{TH} = \tau / R_{TH}$

A standard ±20 % X7R ceramic capacitor is generally sufficient.

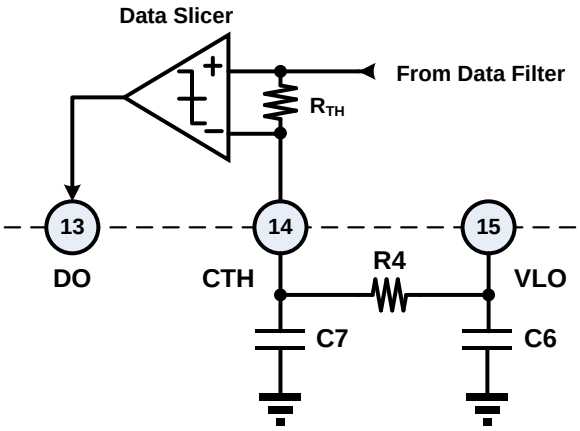
DATA SQUELCHING

During quiet periods (no signal), the data output (DO pin) varies randomly with noise. Most decoders can discriminate between this random noise and actual data, but for some systems, the random toggling does present a problem. There are two possible approaches to reduce this output noise:

1. Implement analog squelch by raising the demodulator threshold.
2. Add an output filter in order to filter the (high frequency) noise glitches on the data output pin.

The simplest solution is add analog squelch by introducing a small offset, or squelch voltage, on the CTH pin so that noise does not trigger the internal slicer. Usually 20 mV to 30 mV is sufficient and may be achieved by connecting a several mega-Ohm resistor from the CTH pin to the internal supply voltage. The squelch-offset requirement does not change as the local noise strength changes from installation to installation. Introducing squelch will reduce both sensitivity and the receiving dynamic range. Only an amount of offset sufficient to quiet the output should be introduced. Typical squelch resistor values range from 5.1 MΩ to 8.2 MΩ.

The circuit drawn below shows an application example of analog squelch, where R4 is the squelch resistor. The demodulated data then enters into a quasi-mute state as the RF input signal becomes very small (when there is no RF signal received or the RF signal is too small) and the DO output remains mostly at a logic "LOW" level. If the environment is very noisy, the value of R4 may be reduced to achieve better immunity against noise, but at the cost of loss of sensitivity.



SENSITIVITY AND SELECTIVITY

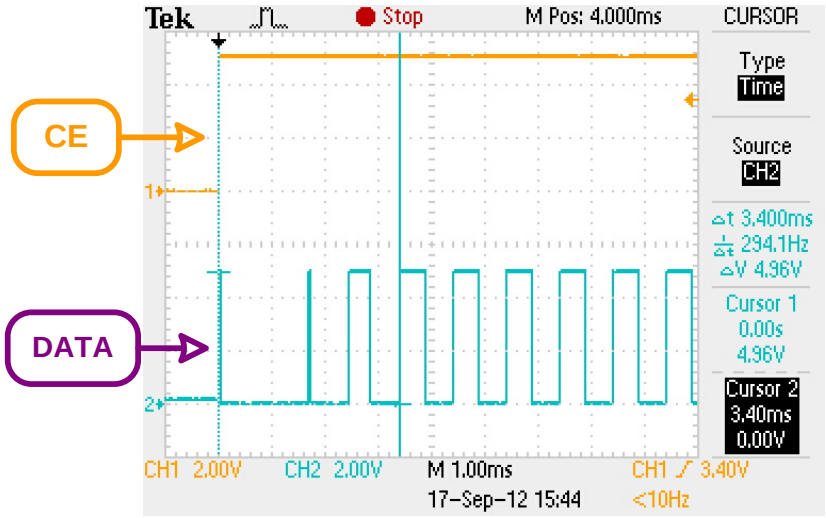
In digital radio systems, sensitivity is often defined as the lowest signal level at the receiver input that will achieve a specified bit error ratio (BER) at the output. The sensitivity of the PT4304 receiver, when used in the 315 MHz application, is typically –114 dBm (ASK modulated with 2 Kb/s, 50% duty cycle square wave) to achieve a 0.1% BER (with input was matched to a 50 Ω signal source). At 433.92 MHz, –112 dBm sensitivity is typically achievable.

The selectivity is governed by the response of the receiver front-end circuitry, the CSF (on-chip active IF filter), and the data filter. Note that the CSF provides not only channel selectivity, but also the interference rejection. Within the pass band of the receiver, no rejection for interfering signals is provided.

POWER-DOWN CONTROL

The chip enable (CE) pin controls the power on/off behavior of the PT4304. Connecting CE to "HIGH" sets the PT4304 to its normal operation mode; connecting CE to "LOW" sets the PT4304 to standby mode. The chip consumption current will be lower than 1 μA in standby mode. Once enabled, the PT4304 relies on an internal fast start-up circuit to achieve a start-up time of around 4 ms to recover received data at 3-dB above the minimum received RF input level.

The following figure exhibits the system start-up time in the conditions of Temp=27ºC, f_{RF} = 433.92 MHz, P_{RF} = –109 dBm, C_{TH} = 47 nF and D_{RATE} = 2 Kb/s. The CE pin is triggered every 500 mS.



ANTENNA DESIGN

For a λ/4 dipole antenna and operating frequency, f (in MHz), the required antenna length, L (in cm), may be calculated by using the formula

$$L = \frac{7132}{f}$$

For example, if the frequency is 315 MHz, then the length of a λ/4 antenna is 22.6 cm. If the calculated antenna length is too long for the application, then it may be reduced to λ/8, λ/16, etc. without degrading the input return loss. However, the RF input matching circuit may need to be re-optimized. Note that in general, the shorter the antenna, the worse the receiver sensitivity and the shorter the detection distance. Usually, when designing a λ/4 dipole antenna, it is better to use a single conductive wire (diameter about 0.8 mm to 1.6 mm) rather than a multiple core wire.

If the antenna is printed on the PCB, ensure there is neither any component nor ground plane underneath the antenna on the backside of PCB. For an FR4 PCB (ε_r = 4.7) and a strip-width of 30 mil, the length of the antenna, L (in cm), is calculated by

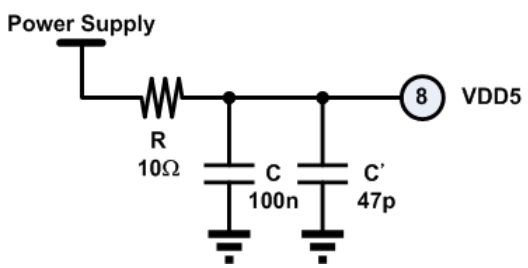
$$L = \frac{c}{4 \times f \times \sqrt{\varepsilon_r}}$$

where "c" is the speed of light (3 x10^{10} cm/s).

PCB LAYOUT CONSIDERATION

Proper PCB layout is extremely critical in achieving good RF performance. At the very least, using a two-layer PCB is strongly recommended, so that one layer may incorporate a continuous ground plane. A large number of via holes should connect the ground plane areas between the top and bottom layers. Note that if the PCB design incorporates a printed loop antenna, there should be no ground plane beneath the antenna.

Careful consideration must also be paid to the supply power and ground at the board level. The larger ground area plane should be placed as close as possible to all the VSS pins. To reduce supply bus noise coupling, the power supply trace should be incorporate series-R, shunt-C filtering as shown below.

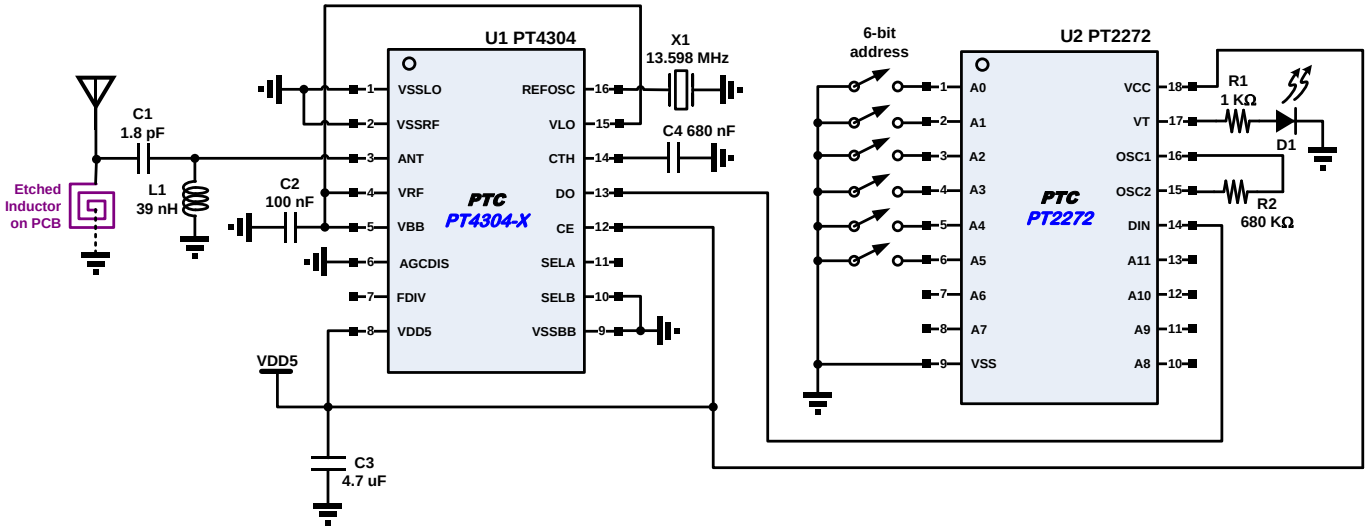


APPLICATION EXAMPLE

433.92 MHz Receiver / Decoder Application

The following schematic illustrates a typical application at the 433.92 MHz frequency band for the PT4304 receiver IC. This receiver operates continuously (not duty cycled) in the enable (active) mode, and features 6-bit address decoding.

The value of C4 may need to be increased if the idle time is too long between each data frame. Changes from the 1 Kb/s data rate may require a change in the value of R2. A bill of materials accompanies the schematic.



Part	Part Number	Manufacturer	Description
U1	PT4304-X	Princeton Technology Corp.	UHF OOK/ASK receiver
U2	PT2272	Princeton Technology Corp.	Remote control decoder
C1	-	-	1.8 pF SMD capacitor
C2	-	-	100 nF SMD capacitor
C3	-	-	4.7 μF SMD capacitor
C4	-	-	680 nF SMD capacitor
D1	-	-	Red LED
L1	-	-	39 nH SMD inductor
R1	-	-	1 KΩ SMD resistor with 5% tolerance
R2	-	-	680 KΩ SMD resistor with 5% tolerance
X1	-	-	13.598 MHz crystal with maximum 80 Ω ESR

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage Range	V_{DD5}	–0.3	6	V
Analog I/O Voltage	—	–0.3	3	V
Digital I/O Voltage	—	–0.3	6	V
Operating Temperature Range	T_A	–40	+85	°C
Storage Temperature Range	T_{STG}	–40	+125	°C

PACKAGE THERMAL CHARACTERISTIC

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
From Chip Conjunction Dissipation to External Environment	Rja	T_A = 27 °C	—	37.15	—	°C/W
From Chip Conjunction Dissipation to Package Surface	Rjc		—	1	1.8	

ELECTRICAL CHARACTERISTICS

Nominal conditions: V_{DD5} = 5.0 V, V_{SS} = 0 V, CE = HIGH, T_A = +27°C.

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
General Characteristics						
Supply Voltage	V_{DD5}	Supply voltage applied to VDD5 pin only	2.4	5.0	5.5	V
Current Consumption	I_{DD5}	f_{RF} = 315 MHz	3.9	4.3	4.7	mA
		f_{RF} = 433.92 MHz	4.2	4.6	5.0	
Standby Current	I_{STBY}	CE = LOW	—	—	1	μA
Operating Frequency Range	f_{RF}	FDIV = LOW	300	—	320	MHz
		FDIV = FLOATING	410	—	450	
Maximum Receiver Input Level	$P_{RF,MAX}$		–20	–15	—	dBm
Sensitivity[1]	S_{IN}	ASK[2], D_{RATE} = 2 Kb/s, Peak power level at 315 MHz	—	–114	–111	dBm
		OOK, D_{RATE} = 2 Kb/s, Peak power level at 315 MHz	—	–108	–105	
		ASK[2], D_{RATE} = 2 Kb/s, Peak power level at 434 MHz	—	–112	–109	dBm
		OOK, D_{RATE} = 2 Kb/s, Peak power level at 434 MHz	—	–106	–103	
Data Rate	D_{RATE}		—	2	10	Kb/s
System Start-Up Time	T_{STUP}		2	4	6	ms
RF Front-End						
Image Rejection Ratio	IRR		20	25	—	dB
LO Leakage	L_{LO}	Measured at antenna input	—	—	–80	dBm
IF Section						
IF Center Frequency	f_{IF}	f_{RF} = 315 MHz	—	1.235	—	MHz
		f_{RF} = 433.92 MHz	—	1.236	—	
IF Bandwidth	BW_{IF}		—	380	—	KHz
RSSI Slope	SL_{RSSI}		9	10.5	12	mV/dB
Receive Modulation Duty Cycle	DUTY		20	—	80	%
Demodulator						
Post-Demodulator Filter Bandwidth (f_{RF} = 315 MHz)	BW_{DF}	SELA = SELB = FLOATING	—	0.9	—	KHz
		SELA = FLOATING; SELB = LOW	—	1.8	—	
		SELA = LOW; SELB = FLOATING	—	3.6	—	
		SELA = SELB = LOW	—	7.2	—	
Post-Demodulator Filter Bandwidth (f_{RF} = 433.92 MHz)	BW_{DF}	SELA = SELB = FLOATING	—	1.25	—	KHz
		SELA = FLOATING; SELB = LOW	—	2.5	—	
		SELA = LOW; SELB = FLOATING	—	5.0	—	
		SELA = SELB = LOW	—	10	—	
CTH Leakage Current	I_{ZCTH}	T_A = +85 °C	—	±100	—	nA

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Phase-Locked Loop						
Reference Frequency	f_{REFOSC}		9	—	15	MHz
Reference Signal Voltage Swing[3]	V_{REF}	Peak-to-peak voltage (V_{PP})	0.6	—	2	V
VCO Frequency Range	f_{VCO}		250	—	500	MHz
Divider Ratio	DIV		—	32	—	—
Digital/Control Interface						
Input-High Voltage	V_{IH}	For CE pin	0.8 × V_{DD5}	—	—	V
Input-Low Voltage	V_{IL}	For AGCDIS, CE, FDIV, SELA and SELB pins	—	—	0.2 × V_{DD5}	V
Output Current	I_{OUT}	Source current at 0.8 × V_{DD5}	—	480	—	μA
		Sink current at 0.2 × V_{DD5}	—	600	—	
Output-High Voltage	V_{OH}	DO pin, I_{OUT} = –1 μA	0.9 × V_{DD5}	—	—	V
Output-Low Voltage	V_{OL}	DO pin, I_{OUT} = +1 μA	—	—	0.1 × V_{DD5}	V
Output Rise/Fall Times	t_R / t_F	DO pin, C_{LOAD} = 15 pF	—	2	—	μs

Notes:
1. Packet Error Rate (PER) < 1e-2 with one byte packet of $A5_{hex}$.
2. AM 99% with square-wave modulation
3. Depends on the ESR of crystal

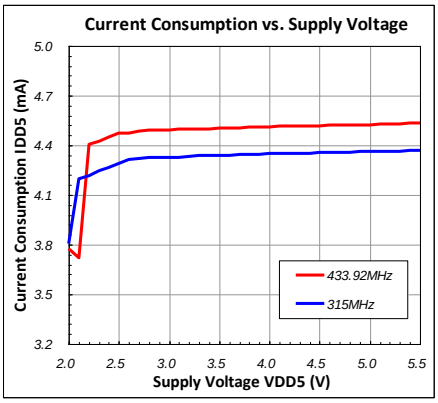


Figure 1. Current Consumption vs. Supply Voltage

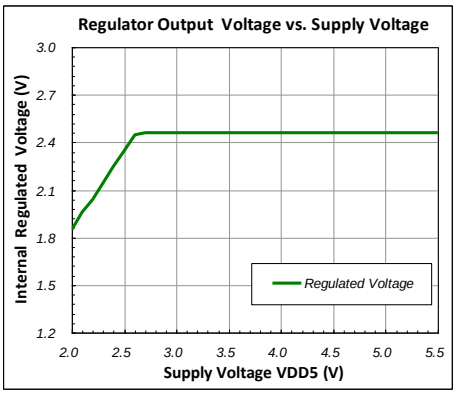


Figure 2. Voltage Regulator Characteristic

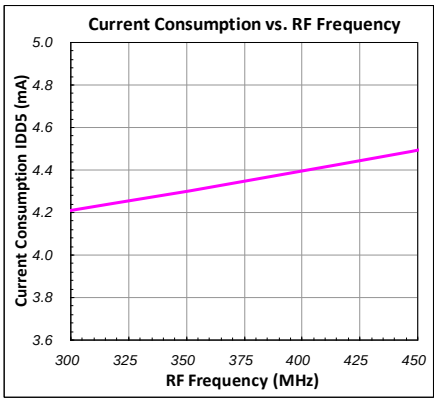


Figure 3. Current Consumption vs. RF Frequency

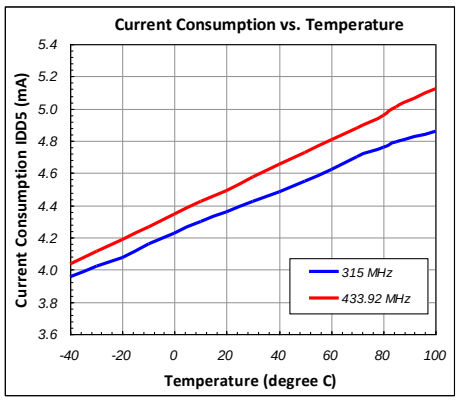


Figure 4. Current Consumption vs. Temperature

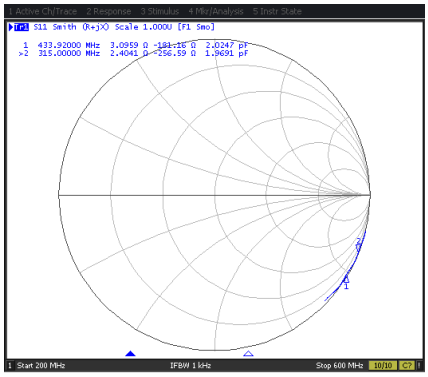


Figure 5. Smith Plot of ANT

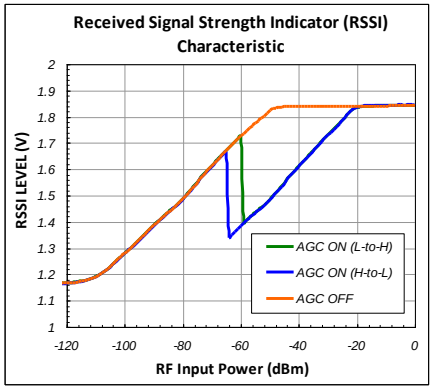


Figure 6. RSSI Characteristic

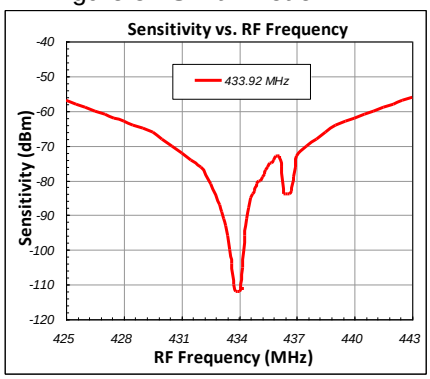


Figure 7. Sensitivity vs. RF Frequency for 433.92 MHz Band

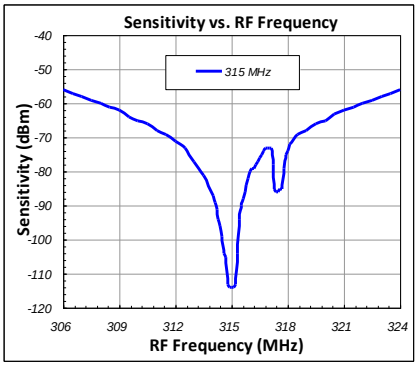
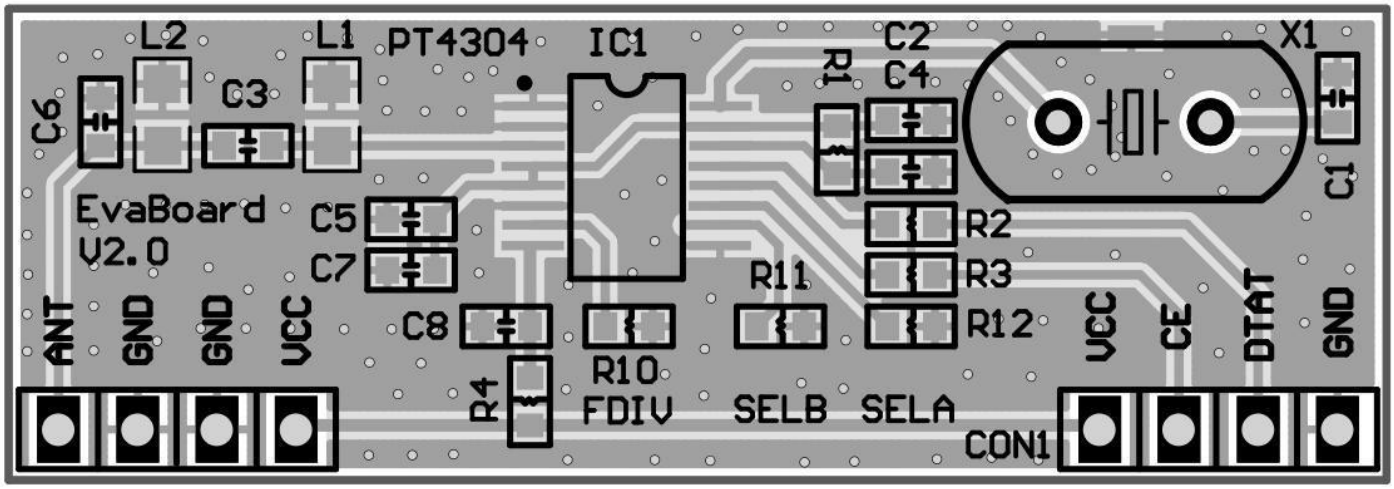


Figure 8. Sensitivity vs. RF Frequency for 315 MHz Band

EVALUATION BOARD LAYOUT



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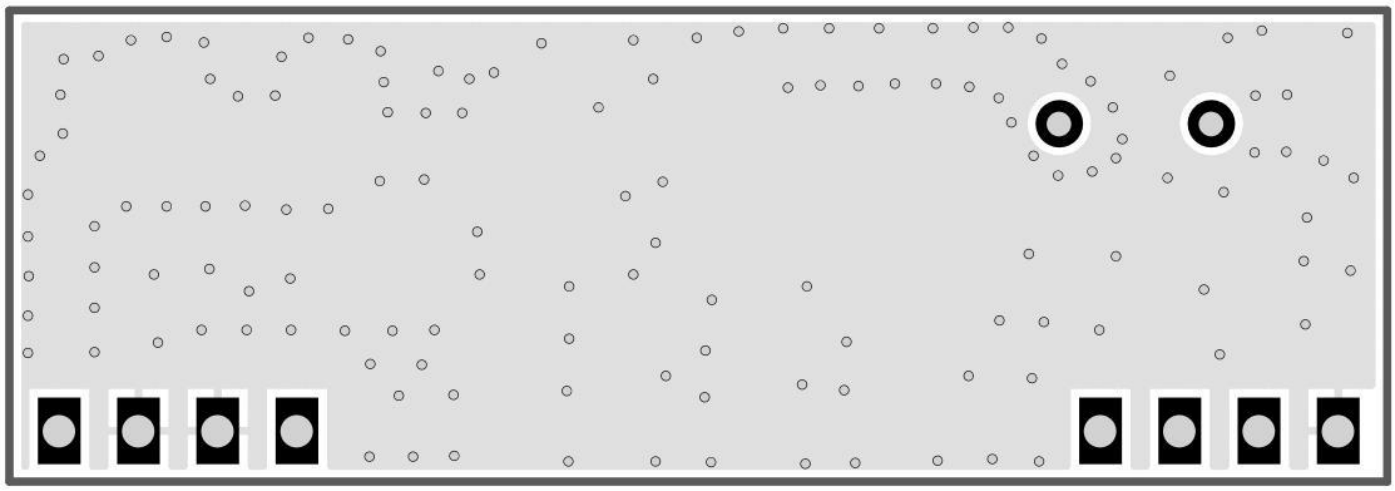
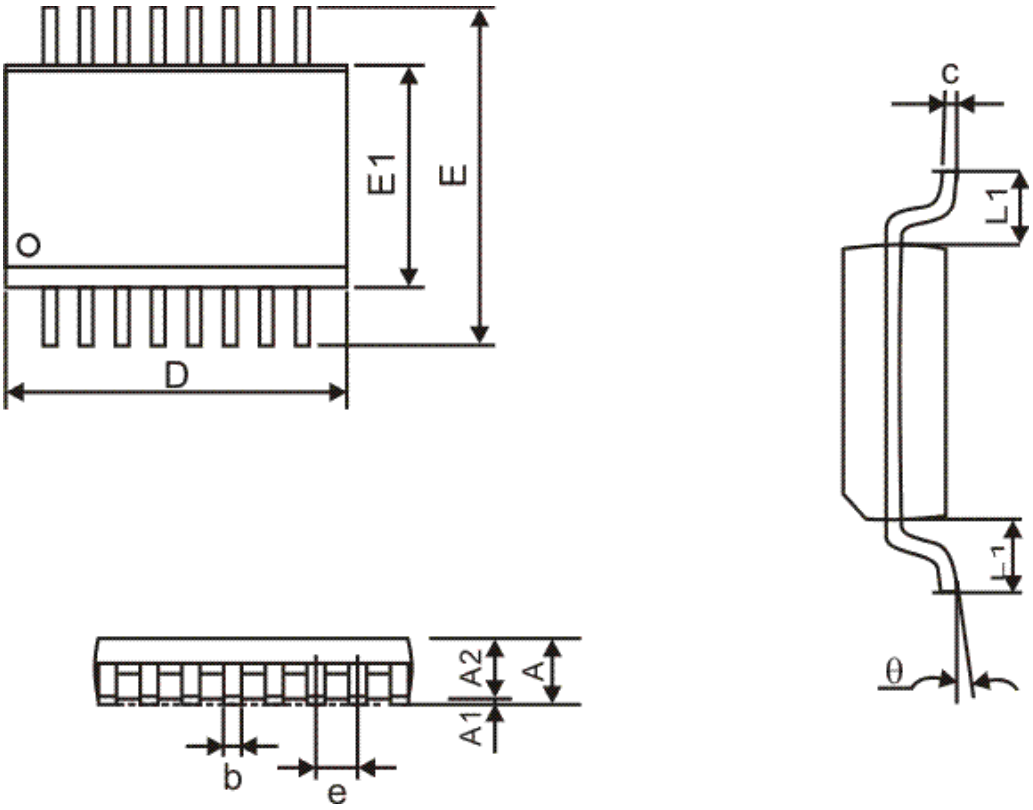


<Bottom Side>

PACKAGE INFORMATION

16 Pins, SSOP (Shrink Small Outline Package with 3.9 × 4.9 mm Body Size, 0.64 mm Pitch Size and 1.6 mm Thick Body)



Symbol	Min.	Nom.	Max.
A	-	-	1.750
A1	0.100	-	-
A2	1.245	-	-
b	0.203	-	0.305
c	0.102	-	0.254
D	4.90 BSC		
e	0.635 BSC		
E	6.00 BSC		
E1	3.90 BSC		
L1	1.04 REF		
	0º	-	8º

Notes:

1. Refer to JEDEC MO-137AB
2. Unit: mm

IMPORTANT NOTICE

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