

DESCRIPTION

PT4452 is a high performance OOK/ASK/FSK transmitter for the Remote Keyless Entry (RKE) systems. It consists of a power amplifier, one-shot circuit and phase-locked loop with internal voltage controlled oscillator and loop filter. The one-shot circuit controls the phase-locked loop and power amplifier to have fast start-up time in operation.

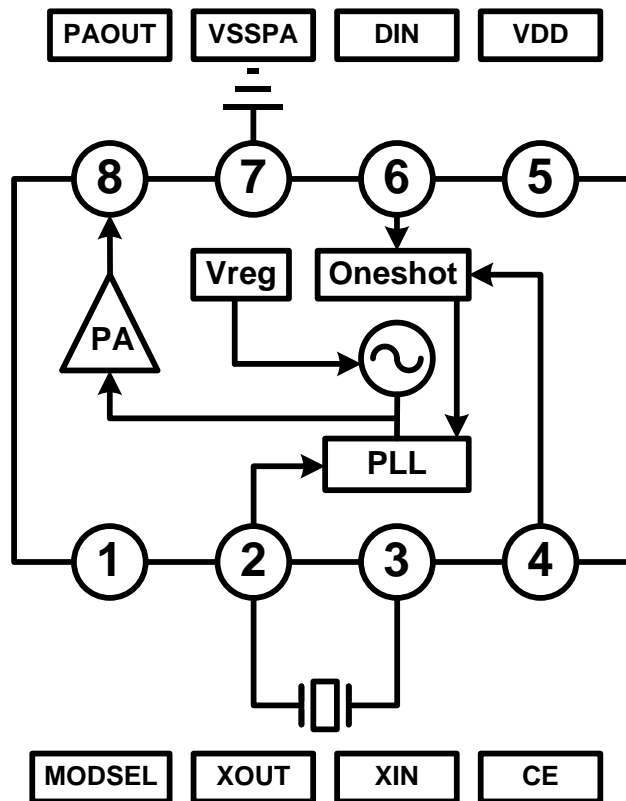
APPLICATIONS

- Keyless entry systems
- Remote control systems
- Garage door openers
- Alarm systems
- Security systems
- Wireless sensors

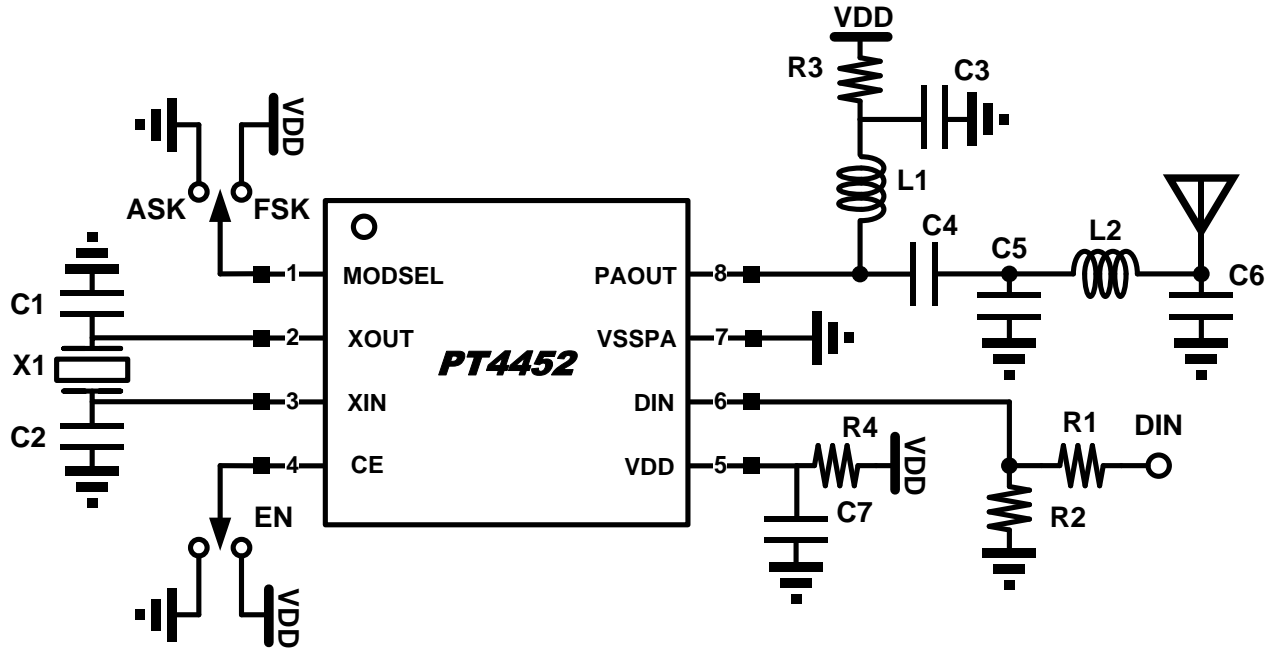
FEATURES

- Highly integrated OOK/ASK/FSK transmitter
- High output power, 3V/+11dBm/17mA
- Low supply voltage, 2.4V to 3.6V operation range
- Low external component cost.
- PLL-based transmitter with frequency range from 300MHz to 450MHz
- On-chip one-shot circuit
- 60 dB RF on-off ratio for OOK/ASK modulation
- SOP8 package

BLOCK DIAGRAM



APPLICATION CIRCUIT



BILL OF MATERIALS

Part	Value		Unit
	315MHz	433.92MHz	
X1	9.844M	13.56M	Hz
R1	10K	10K	Ohm
R2	100K	100K	Ohm
R3	0	0	Ohm
R4	0	0	Ohm
C1	22p	18p	F
C2	22p	18p	F
C3	1 μ	1u	F
C4	220p	220p	F
C5	8.2p	4.7p	F
C6	18p	10p	F
C7	2.2 μ	2.2 μ	F
L1	180n	180n	H
L2	33n	27n	H

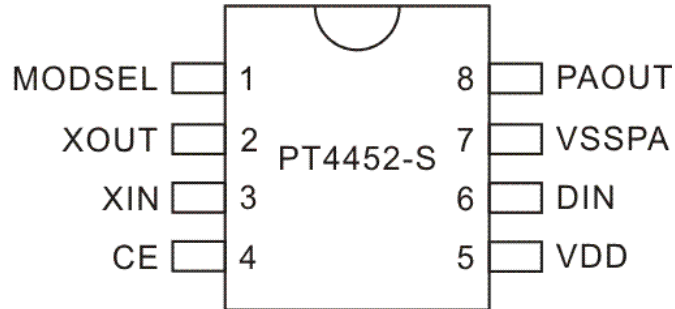
Notes:

1. C1/C2 can be used to trim the transmitted signal frequency for matching the specified value.
2. For FSK application to have adequate frequency deviation, and accurate carrier frequency, the crystal resonator frequency will be lower than the specified value. The recommended crystal resonator frequency is 9.8388MHz and 13.5545MHz for 315MHz and 433.92MHz band. The loading capacitor C1/C2 will put below 20pF to have ± 50 KHz pulling frequency deviation at least.
3. L2/C5/C6 value will depend on PCB layout.
4. The recommend maximum ESR value of X1 is 40 Ω .

ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT4452-S	8-Pin, SOP, 150MIL	PT4452-S

PIN CONFIGURATION



PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
MODSEL	I	ASK/FSK modulation selection. "0"=ASK, "1"=FSK	1
XOUT	O	Oscillator output	2
XIN	I	Oscillator input	3
CE	I	Chip enables. "1" to enable the chip	4
VDD	P	Power supply	5
DIN	I	Data input	6
VSSPA	G	Power amplifier ground	7
PAOUT	O	Power amplifier output	8

FUNCTION DESCRIPTION

PA OUTPUT MATCHING

The PA output is an open-drain structure. Its output connects a large choke inductor to supply voltage and follows by a DC block capacitor. After the DC block capacitor, a C-L-C π -type matching network is used to tune with the antenna impedance. The inductor and capacitor values may be different from the suggestion value depending on PCB material, PCB thickness, ground configuration, and the layout traces length.

For the open-drain structure in PA, the HBM (Human Body Mode) and MM (Machine Mode) ESD strength is 4KV and 400V.

REFERENCE OSCILLATOR

For a quartz crystal to oscillate in the specified frequency, it should work with vendor provided load capacitor value, called C_L . The load capacitor is about 12pF to 18pF in general. In PT4452, the Pierce type crystal oscillator is used, and the shunt capacitor over XIN and XOUT is in series together equivalently. The shunt capacitor should be placed as $2x C_L$ to oscillate with specified frequency. The temperature coefficient of quartz crystal will cause the VCO output frequency drift in high/low temperature range.

In the FSK mode, the DIN signal will connect/disconnect the internal shunt capacitor over XIN and XOUT. The shunt capacitor connected inside the chip is about 7pF.

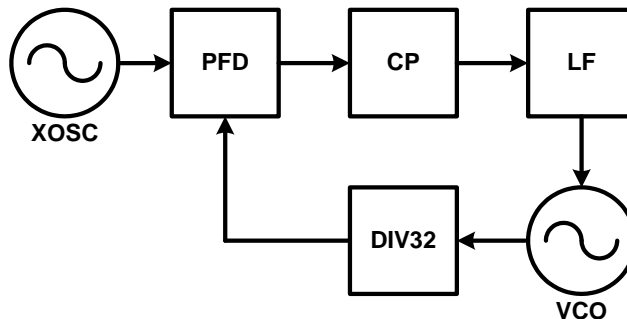
With a fixed divided-by-32 PLL, the $f_{REFOSC} = f_{TX} / 32$. The following table list f_{REFOSC} for some common transmit frequencies

Transmit Frequency f_{TX}	Reference Oscillator Frequency f_{REFOSC}
315MHz	9.844MHz
340MHz	10.625MHz
390MHz	12.188MHz
433.92MHz	13.56MHz

The recommend maximum ESR value of reference oscillator is 40 Ω .

PHASE-LOCKED LOOP (PLL)

The PT4452 own a fixed divided-by-32 PLL to generate the transmitter signal. The PLL consists of the voltage-controlled oscillator (VCO), crystal oscillator, asynchronous $\div 32$ divider, charge pump, loop filter and phase-frequency detector (PFD). All these circuits are integrated on-chip. The PFD compares two signals and produces an error signal which is proportional to the difference between the input phases. The error signal passes through a loop filter with an approximately 180KHz bandwidth, and is used to control the VCO. A frequency divider placed after the VCO and it will feedback the divided signal to PFD. In the final the VCO will get locked to reference signal as $f_{VCO} = f_{REFOSC} \times 32$. The block diagram below shows the basic elements of the PLL.



The PLL chain circuit is supplied by internal voltage regulator to ease the PA pulling and crystal spur issue

ONE-SHOT CIRCUIT AND POWER-DOWN CONTROL

During the signal transmission, the crystal oscillator start-up time will limit its wake-up time to work. A one-shot circuit is used to solve this problem by turning on/off the power amplifier and PLL circuit separately.

In OOK/ASK mode, applied "HIGH" to DIN, will enable the PLL chain and PA. When applied "LOW" to DIN, the PA will be turn-off immediately, and the PLL chain will be turn-off after one-shot period about 50ms.

In FSK mode, "HIGH" and "LOW" signal in DIN will pull the VCO to higher or lower frequency. To enter the power-down mode, CE needs to tie "LOW". A summary table below to state the relationship between them,

CE	MODSEL	DIN	MODE	PLL	PA
1	0	0	ASK	Off, after one-shot delay	Off
1	0	1	ASK	On	On
1	1	0	FSK	On, VCO to lower frequency	On
1	1	1	FSK	On, VCO to higher frequency	On
0	X	X	X	Off	Off
0	X	X	X	Off	Off
0	X	X	X	Off	Off
0	X	X	X	Off	Off

To calculate the re-triggerable one-shot delay time, it can be counted as $688128 / f_{REFOSC}$. For $f_{REFOSC} = 9.844\text{MHz}$ and 13.56MHz , the delay time is about 70ms and 50ms.

ANTENNA DESIGN AND PCB LAYOUT CONSIDERATION

For a $\lambda/4$ dipole antenna and operating frequency, f (in MHz), the required antenna length, L (in cm), may be calculated by using the formula

$$L = \frac{7132}{f}$$

For example, if the frequency is 315 MHz, then the length of a $\lambda/4$ antenna is 22.6cm. If the calculated antenna length is too long for the application, then it may be reduced to $\lambda/8$, $\lambda/16$, etc. without degrading the input return loss. Usually, when designing a $\lambda/4$ dipole antenna, it is better to use a single conductive wire (diameter about 0.8mm to 1.6mm) rather than a multiple core wire.

If the antenna is printed on the PCB, ensure there is neither any component nor ground plane underneath the antenna on the backside of PCB. For an FR4 PCB ($\epsilon_r = 4.7$) and a strip-width of 30 mil, the length of the antenna, L (in cm), is calculated by

$$L = \frac{c}{4 \times f \times \sqrt{\epsilon_r}} \quad \text{where "c" is the speed of light (3 x10}^{10} \text{ cm/s)}$$

Proper PCB layout is extremely critical in achieving good RF performance. At the very least, using a two-layer PCB is strongly recommended, so that one layer may incorporate a continuous ground plane. A large number of via holes should connect the ground plane areas between the top and bottom layers.

Careful consideration must also be paid to the supply power and ground at the board level. The larger ground area plane should be placed as close as possible to all the VSS pins. Grounding the metal case of quartz crystal and isolate the XIN/XOUT trace to other can suppress the crystal spur signal over PA output.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min.	Max.	Unit
Supply Voltage Range	V _{DD5}	-0.3	5	V
I/O Voltage	-	-0.3	5	V
Operating Temperature Range	T _{OPR}	-40	+85	°C
Storage Temperature Range	T _{STG}	-55	+125	°C

ELECTRICAL CHARACTERISTICS

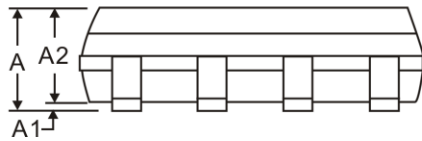
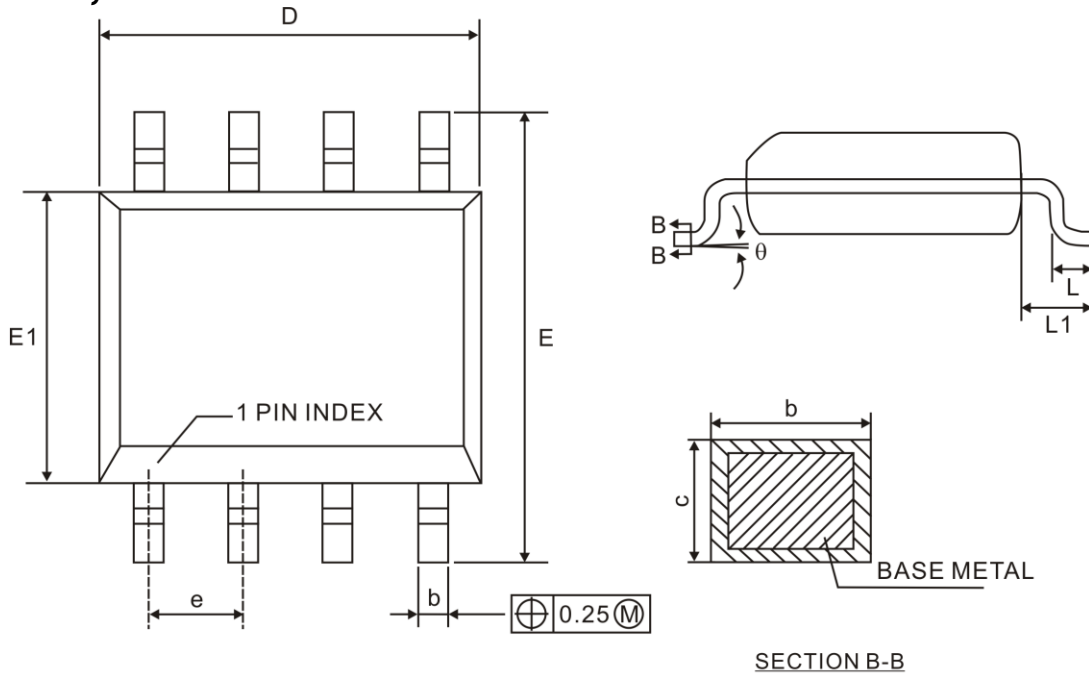
 Nominal conditions: V_{DD}=3.0V, V_{SS}=0V, CE="High", T_A=+27°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
General Characteristics						
Supply Voltage	V _{DD}		2.4	3.0	3.6	V
Operating Current (Note)	I _{DD}	DIN=High(CW mode); P _{OUT} =11dBm, f _{RF} =315MHz	-	17	-	mA
		DIN=High(CW mode); P _{OUT} =10dBm, f _{RF} =434MHz	-	19	-	mA
Standby Current	I _{standby}	DIN=LOW; T _{DELAY} >50ms	-	-	1	μA
RF						
Frequency Range	f _{RF}		300	-	450	MHz
Power Amplifier Output Power (Note)	P _{out}	f _{RF} =315MHz	-	11	-	dBm
		f _{RF} =434MHz	-	10	-	dBm
RF Power On / Off Ratio	P _{EXT}		-	60	-	dB
Phase Noise	P _{NOISE}	315MHz, 10KHz offset	-	-75	-	dBc/Hz
Harmonics (Note)	P _{HARM}	2x/3x f _{RF}	-	-40	-	dBc
Crystal Spur	P _{SPUR}	f _{RF} =315MHz	-	-40	-	dBc
		f _{RF} =434MHz	-	-40	-	dBc
Data Input and One-Shot						
Data Rate	D _{RATE}	OOK/ASK mode	0.5	2	50	Kbps
		FSK mode	-	1	10	Kbps
Frequency Deviation	F _{DEV}	FSK mode, C _L not connected	-	110	150	KHz
Crystal Oscillator Start-up Time	T _{ON}	C _L not connected	-	1	-	ms
One-shot Delay Time	T _{DELAY}	f _{RF} =434MHz	-	50	-	ms

Note: Depend on power amplifier output matching

PACKAGE INFORMATION

8 Pins, SOP, 150MIL



Symbol	Min.	Nom.	Max.
A	1.35	1.60	1.75
A1	0.10	0.15	0.25
A2	1.25	1.40	1.65
b	0.33	-	0.51
c	0.170	-	0.250
e	1.27 BSC.		
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
L	0.40	0.60	1.27
L1	1.04 REF.		
θ	0°	-	8°

Notes:

1. Refer to JEDEC MS-012 AA
2. Unit: mm

IMPORTANT NOTICE

Princeton Technology Corporation (PTC) reserves the right to make corrections, modifications, enhancements, improvements, and other changes to its products and to discontinue any product without notice at any time.

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