DESCRIPTION

The PT5139 is a dual H-bridge motor driver which can drives two brushed DC motors or a single bipolar stepper motor, solenoids or other inductive loads. Each bridge driver includes a PWM current regulation circuitry to limit the winding current. The H-bridge driver is consists by all of N-channel MOSFETs.

The device have built-in protection features, includes under-voltage lockout (UVLO), over current protection (OCP) and thermal shutdown (TSD). A fault flag output is available to indicates the OCP or TSD conditions is happens.

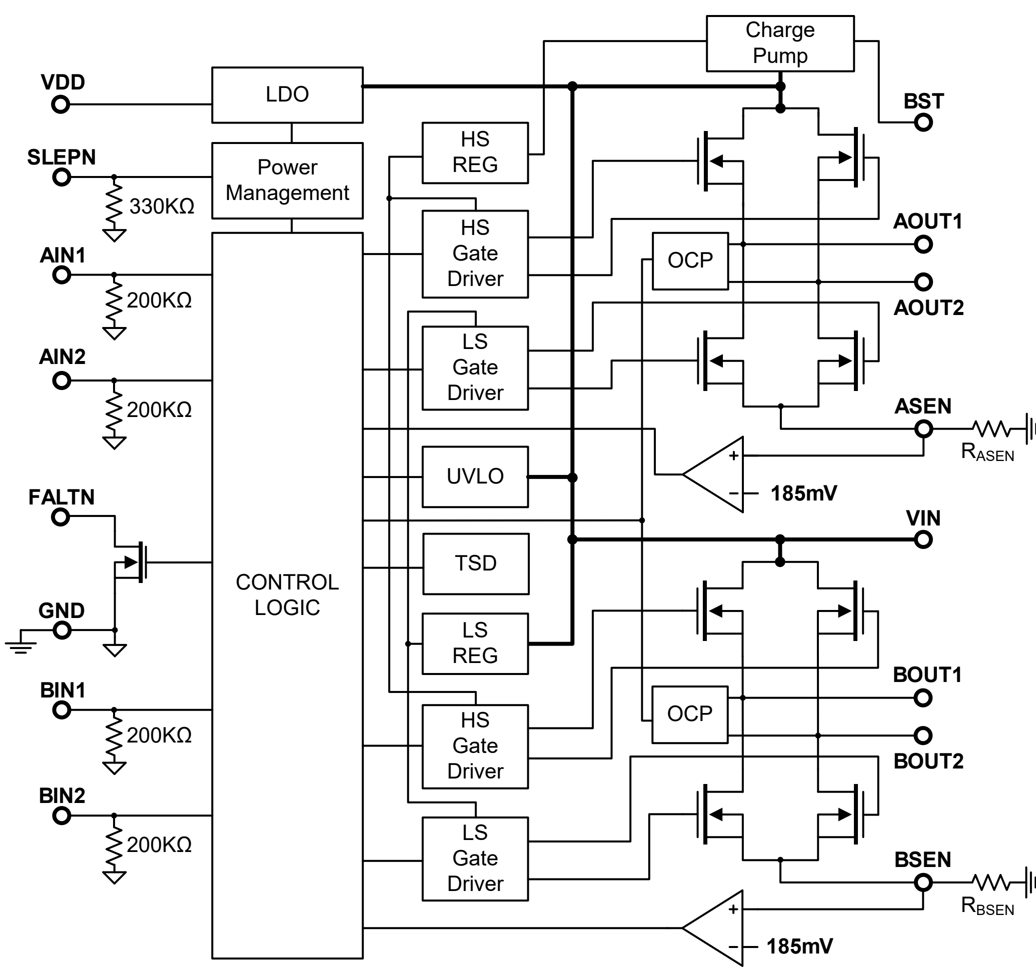
APPLICATIONS

- POS Printers
- Video Security Camera
- Robotics
- Battery Powered Toys

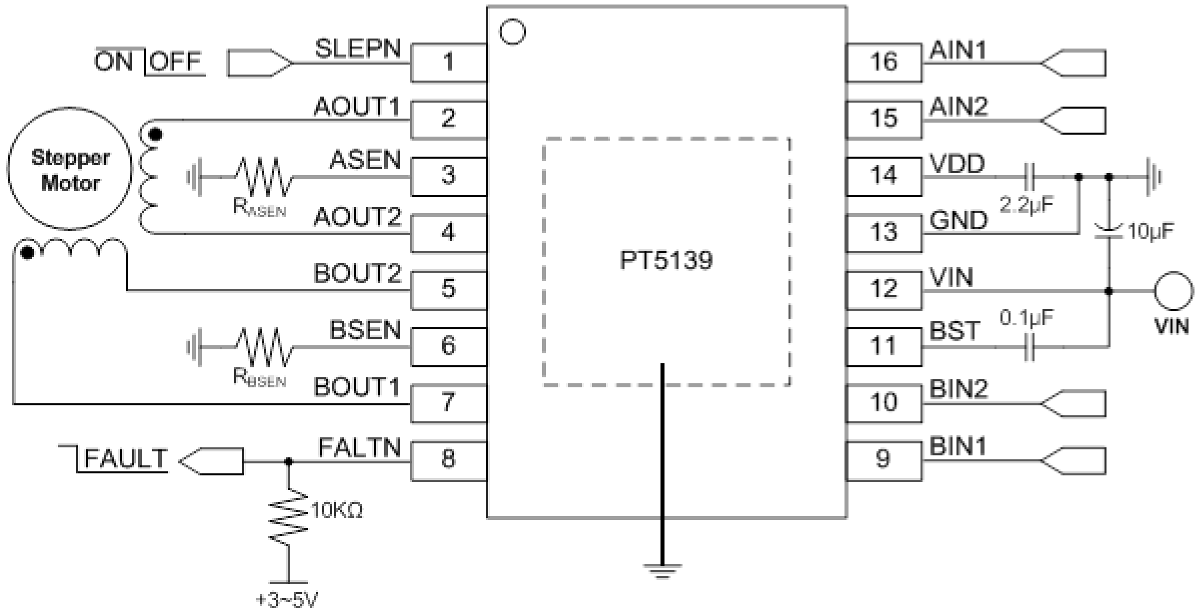
FEATURES

- Wide Supply Voltage Range: 2.7V to 15V
- Dual H-bridge Drivers, drivers two brushed dc motor or single bipolar stepping motor
- MOSFET RDS(on) Resistance HS + LS = 1060mΩ
- Output Current : 700mA (HTSSOP package)
- Internal PWM Current Regulation Function
- Low Quiescent Current : 1.5mA
- Low Sleep Current: <1μA
- Built-in Protection Circuits; Thermal Shutdown (TSD), Under Voltage Lock-Out (UVLO) and Over Current Protection (OCP) functions.
- Fault Indicates Output (FALTN)
- Multiple Packages Available:
  - 16 pins QFN, 4.0mm × 4.0mm with thermal pad.
  - 16 pins HTSSOP, 5.0mm × 6.4mm with thermal pad.
  - 16 pins TSSOP, 5.0mm × 6.4mm

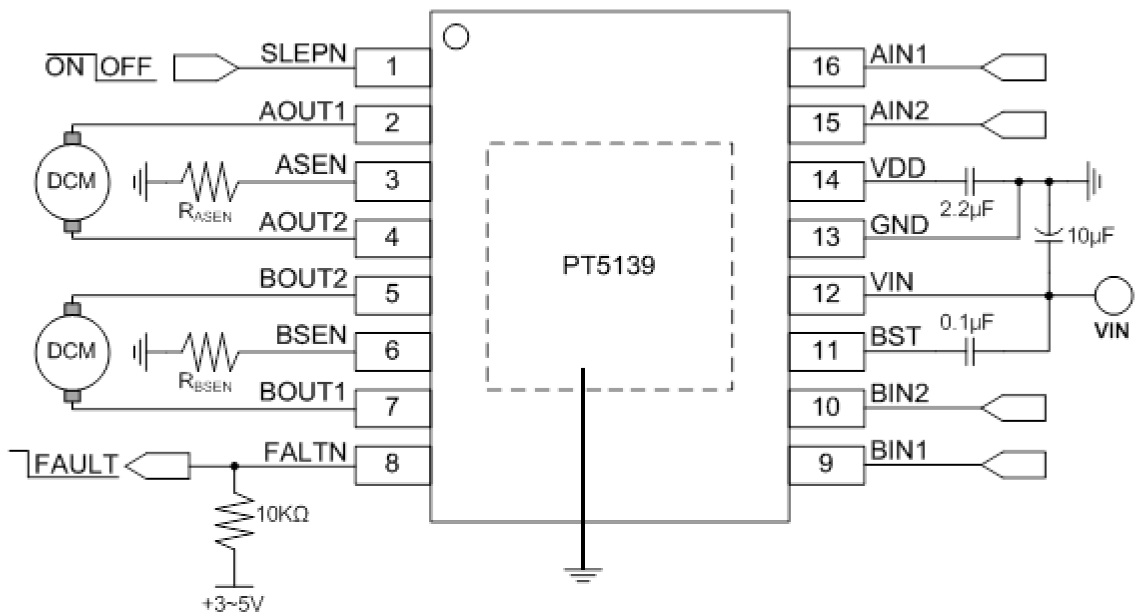
BLOCK DIAGRAM



APPLICATION CIRCUIT



Drives a bipolar stepping motor



Drives two brushed DC motors

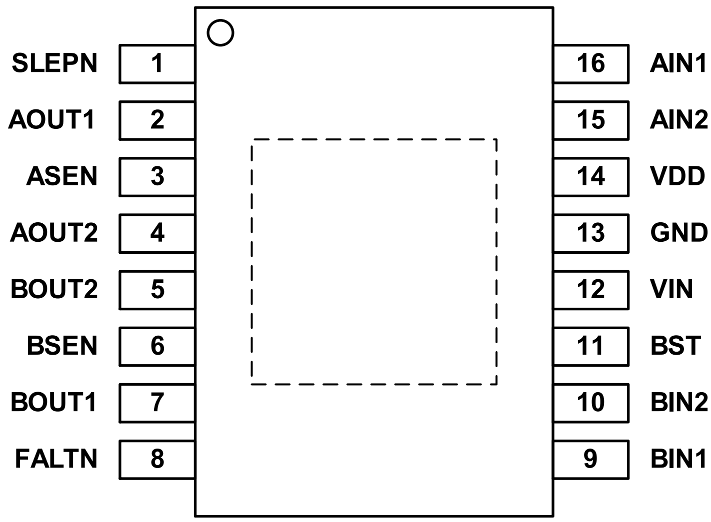
ORDER INFORMATION

Part Number	Package Type	Top Code
PT5139-HT	16-Pin, HTSSOP, 5.0mm × 6.4mm	PT5139-HT
PT5139-TX	16-Pin, TSSOP, 5.0mm × 6.4mm	PT5139-TX
PT5139	16-Pin, QFN, 4.0mm × 4.0mm	PT5139

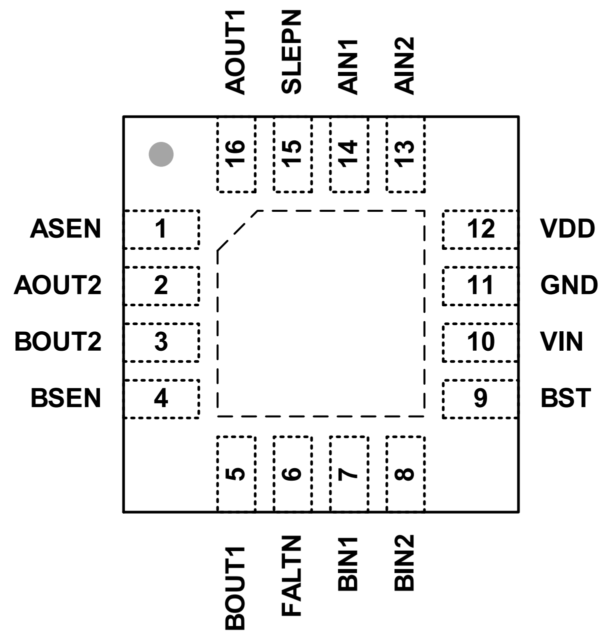
PIN CONFIGURATION

Top View

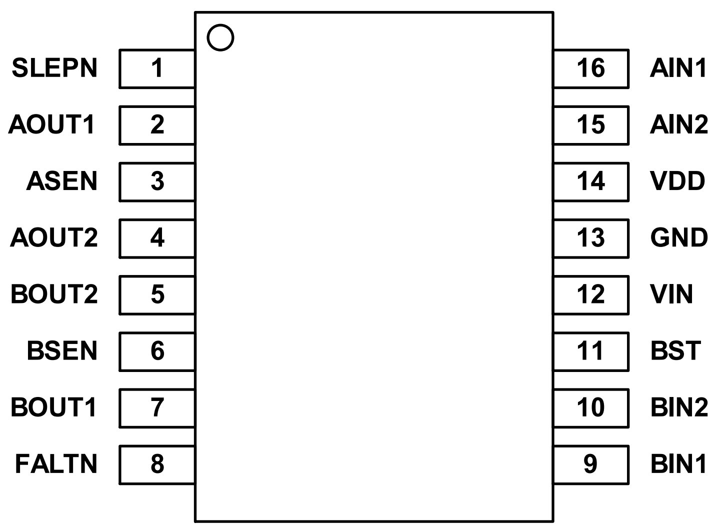
PT5139, HTSSOP



PT5139, QFN, 4mm × 4mm



PT5139, TSSOP



The exposed thermal pad should be connected to GND.

PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.		
			QFN-16, 4×4	HTSSOP-16	TSSOP-16
ASEN	I/O	H-bridge driver A channel current sense, connects a current sensor resistor to GND.	1	3	3
AOUT2	O	H-bridge driver A channel output 2.	2	4	4
BOUT2	O	H-bridge driver B channel output 2.	3	5	5
BSEN	I/O	H-bridge driver B channel current sense, connects a current sensor resistor to GND.	4	6	6
BOUT1	O	H-bridge driver B channel output 1.	5	7	7
FALTN	OD	Fault, Logic low when fault condition appear (OCP, OTP)	6	8	8
BIN1	I	H-bridge driver B channel input 1, internal 200KΩ pull down resistor to GND.	7	9	9
BIN2	I	H-bridge driver B channel input 2, internal 200KΩ pull down resistor to GND.	8	10	10
BST	Power	Charge pump output, connects a 0.01μF ~ 0.1μF ceramic capacitor to VIN.	9	11	11
VIN	Power	Device power supply input, connects a 10μF (at least) bypass capacitor to GND is recommended.	10	12	12
GND	GND	Device ground. The GND pin and thermal pad both must be connected to ground.	11	13	13
VDD	Power	Bypassing pin for Internal LDO output; connects a 2.2μF capacitor to GND. Do not connect any external load to VDD pin.	12	14	14
AIN2	I	H-bridge driver A channel input 2, internal 200KΩ pull down resistor to GND.	13	15	15
AIN1	I	H-bridge driver A channel input 1, internal 200KΩ pull down resistor to GND.	14	16	16
SLEPN	I	Sleep mode input, with internal 330KΩ pull down resistor to GND. H=device enable, L=low-power sleep mode,	15	1	1
AOUT1	O	H-bridge driver A channel output 1.	16	2	2
PGND	GND	Connect to GND.	Thermal Pad	Thermal Pad	-

FUNCTION DESCRIPTION

The PT5139 is a motor driver chip designs to driving the brushed dc or bipolar stepping motor. The device integrates two H-bridges consist by al of N channel MOSFET and current regulation circuitry. The PT5139 is powered by a supply voltage from 2.7V to 15V, and also delivery output current up to 700mA. The PT5139 has low power sleep mode, it could reduce the stand-by current under 1μA to extend battery operation time

The motor output current either controlled by an external applied PWM pulse signal, or by the internal PWM current controller. The internal PWM current regulation scheme is a fixed off time with slow decay.

H-BRIDGE OUTPUT CONFIGURATION

The motor winding current direction is determinate by H-bridge output configuration, and it is maniples by control logic interface. Please refer to Table 1 for corresponds between input and output.

SLEPN	VIN	AIN1/ BIN1	AIN2/ BIN2	AOUT1/ BOUT	AOUT2/ BOUT2	DESCRIPTION
H	<UVLO	x	x	Hi-Z	Hi-Z	All of outputs in high impedance.
H		L	L	Hi-Z	Hi-Z	Coast mode, all of outputs in high impedance. Also as fast decay mode during the external PWM signal is applied.
H		L	H	L	H	Reverse mode (Output current from OUT2 to OUT1)
H	>UVLO	H	L	H	L	Forward mode (Output current from OUT1 to OUT2)
H		H	H	L	L	Brake mode; motor current flowing in between both low side MOSFETs. Also as slow decay mode during the external PWM signal is applied.
L		x	x	Hi-Z	Hi-Z	Low power sleep mode, I_{IN}<1μA.

Table 1. H-Bridge Output Operation

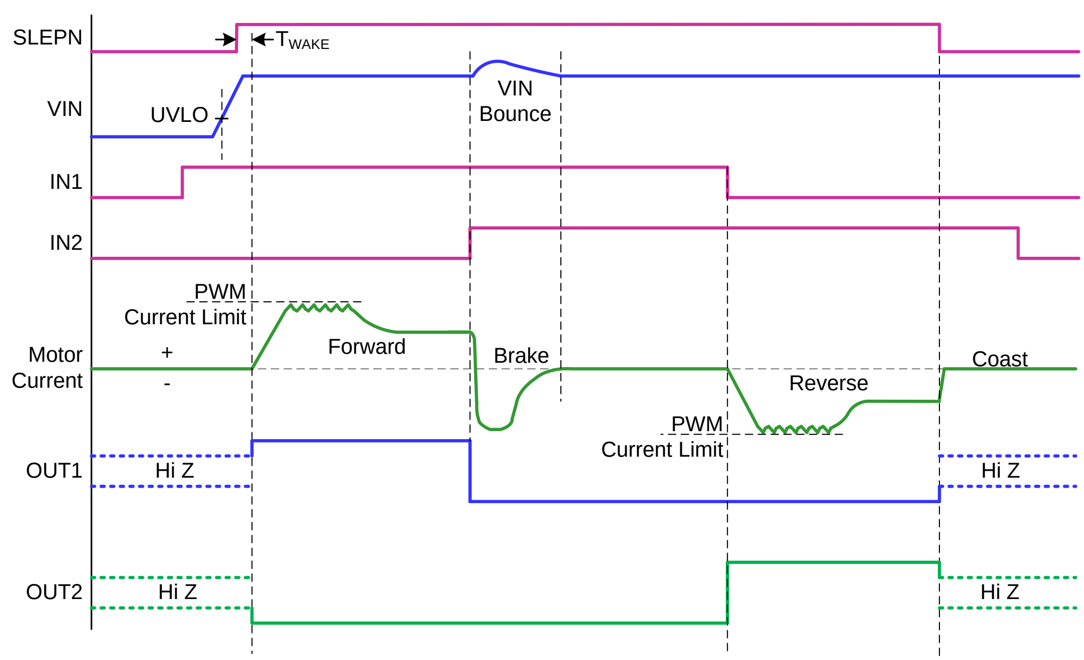


Figure 1. H-Bridge Output Mode and Control Logic Timing

INTERNAL PWM CURRENT REGULATION CONTROL

An internal fixed off-time PWM current control circuit will regulate the motor current as the following:
When an H-bridge is enabled, the winging current ramps up corresponds the VIN DC voltage and winding inductance, and this period is realized as charge time. The winding current will measured by external current sense resistors (R_{SENSE}) on the ASEN and BSEN pins. The current sensing signal (V_{SENSE}) will applies to the PWM comparator input and compares with an internal reference voltage (V_{TRIP}, normally 185mV) to determinate the H-bridge regulated output current (I_{TRIP}).

After the V_{SENSE} exceeds the V_{TRIP} voltage, a short blanking time T_{BLANK} (4μs) is applied to prevent fault current signal interference the PWM circuit. This blanking time also sets the minimum on time of pulse width when operating in current regulation mode. After the blanking time, if the V_{SENSE} still exceeds the V_{TRIP} level, the charge mode will be transit to slow decay mode. The winding current is decreases and recirculated by enabling both of the low-side FETs in the H-bridge. The slow decay time is determinate by internal fixed off time (typically 25μs) timer, after the fixed off time the high-side MOSFET is enable and the motor winding current will charge again.

The PWM regulated current level as: $$I_{TRIP} = \frac{V_{TRIP}}{R_{SENSE}}$$

For example: If a 1.0Ω sense resistor is used, the PWM regulated current will be 185 mV/1.0Ω = 185mA.
If PWM current regulation function is not be used, the ASEN and BSEN pins should be connected to ground.

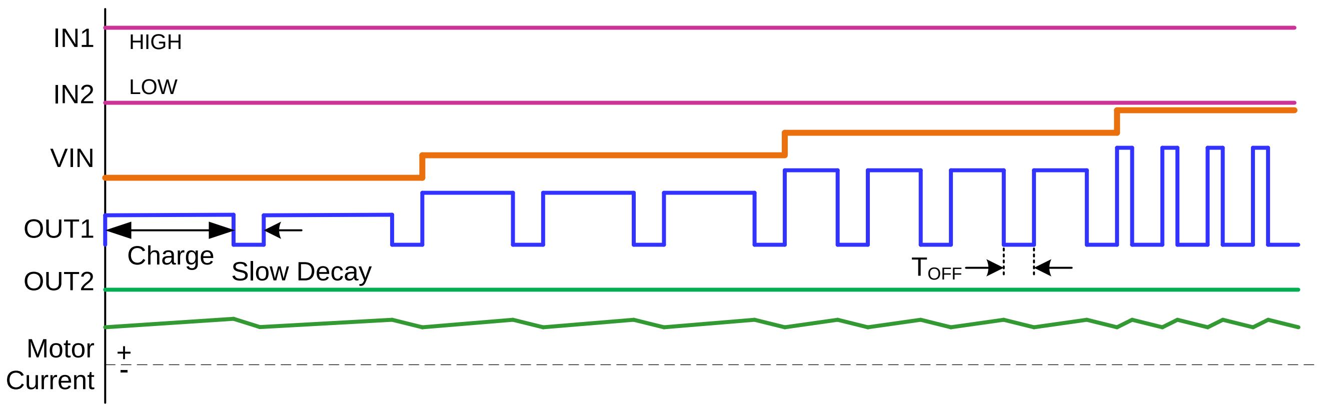


Figure 2. Fixed-off time Internal PWM Current Regulation Waveform and Timing

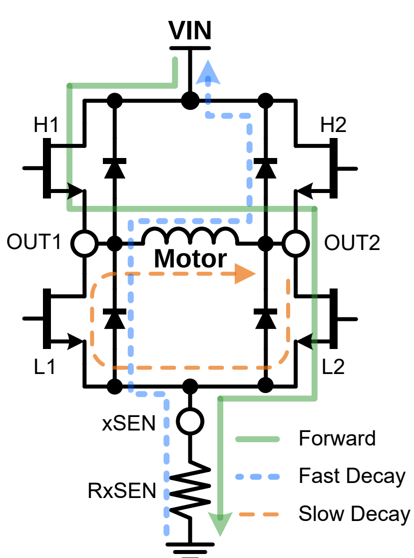


Figure 3: Forward Operation

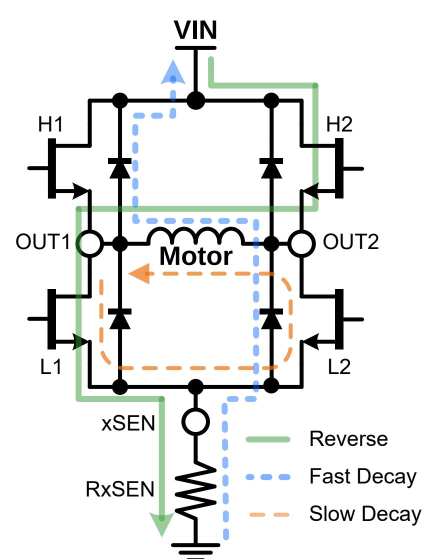


Figure 4: Reverse Operation

EXTERNAL PWM CURRENT CONTROL

The motor current can be controlled by the external PWM signals applying to the AIN1, AIN2, BIN1 and BIN2. The AIN1 and AIN2 input pins control the state of the AOUT1 and AOUT2, the BIN1 and BIN2 input pins control the state of the BOUT1 and BOUT2 identically. The Table 2 shows the correspond logic.

There have two decay mode can implementation by different input logic sequential and please refer to the Table 2.

(1) The PWM signal applies to xIN1 pin only and xIN2 pin staying on logic low state, therefore, the winding charge current is controlled by the xIN1 logic high period. When both input pins becomes logic low state, the winding current will discharged through the body diode of both high and low side MOSFETs, this configuration is called external PWM Fast Decay mode.

(2) If the external PWM signal is applies to the xIN2 pins and xIN1 pins staying on logic high state, therefore, the winding charge current is controlled by the xIN2 logic low period. When both input pins becomes logic high state, the winding current will circulates in both low side MOSFET becomes free-wheeling, this timing sequential is called external PWM Slow Decay mode.

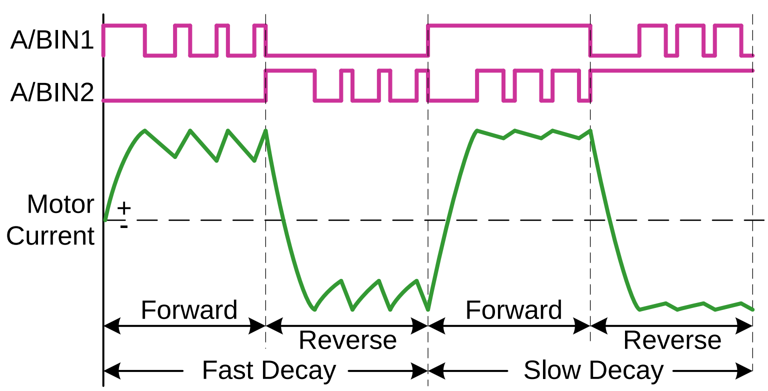


Figure 5: External PWM Current Control Waveform

A/BIN1	A/BIN2	Mode
H (PWM)	L	Forward
L (PWM)	L	Fast Decay
L	H (PWM)	Reverse
L	L (PWM)	Fast Decay
H	L (PWM)	Forward
H	H (PWM)	Slow Decay
L (PWM)	H	Reverse
H (PWM)	H	Slow Decay

Table 2: PWM Control

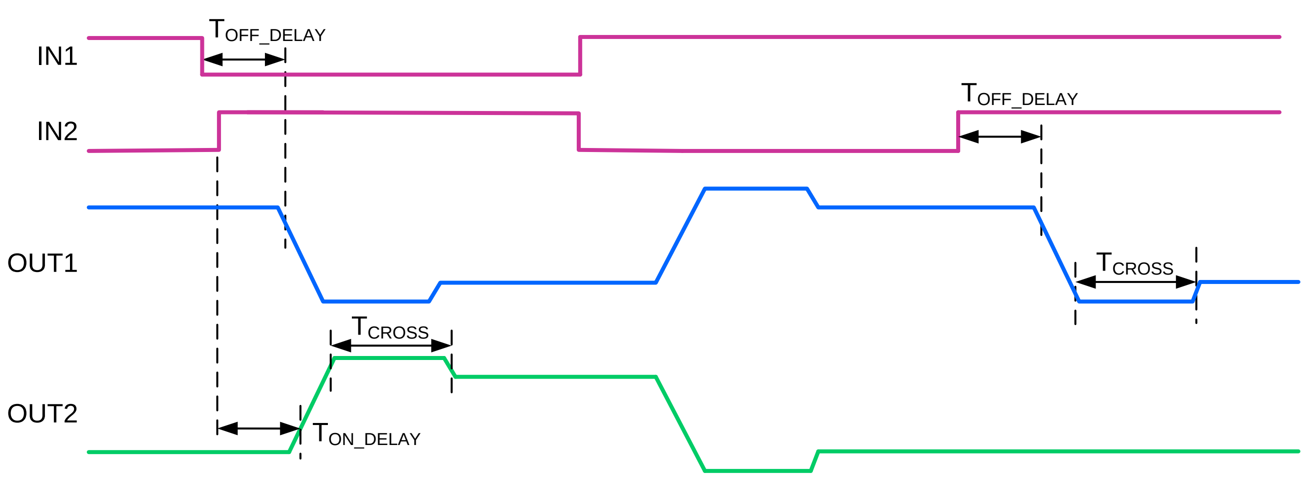


Figure 6. I/O Propagation Delay and Cross Conduction dead time

INPUT LOGIC SEQUENCIAL FOR STEPPING MOTOR

The PT5139 could be configured for both full step and half-step modes by sequentially energizing the two windings. Full-step drive energizes two winding phases at any given time. The stator windings are energized as per the sequence shown in Table 3. There are a total of four steps for one cycle in the sequence: AB→ $\overline{A}$B →$\overline{AB}$→A$\overline{B}$.

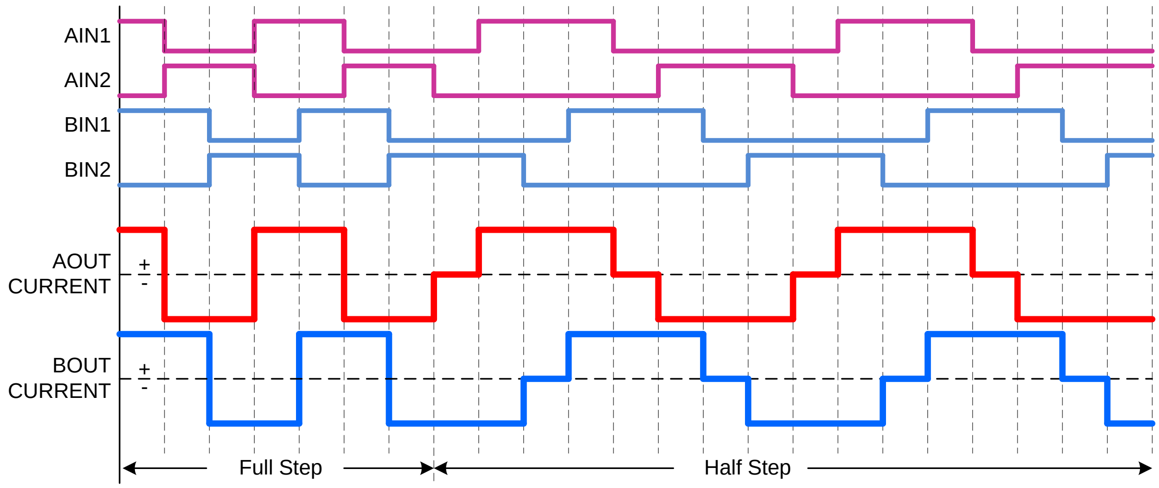


Figure 7: Signal Logic Sequences for Full-Step and Half-Step

Half-step energizes the stator windings as per the sequence shown in Table 4. There are a total of 8 steps for one cycle: AB→B→$\overline{A}$B→$\overline{A}$→$\overline{AB}$→$\overline{B}$→A$\overline{B}$→A.

Sequence(Full Step)	1	2	3	4
A	√			√
B	√	√		
$\overline{A}$		√	√	
$\overline{B}$			√	√

Table 3: Full-Step Drive Sequence

Sequence(Half Step)	1	2	3	4	5	6	7	8
A	√						√	√
B	√	√	√					
$\overline{A}$			√	√	√			
$\overline{B}$					√	√	√	

Table 4: Half-Step Drive Sequence

SLEEP MODE

Pull the SLEPN pin to logic low will force the chip into a low power sleep mode. During sleep mode is active the H-bridges outputs are disabled, and analog circuit such like internal clocks blocks are all stopped. In this mode all inputs are ignored until SLEPN returns to logic high state. When chip is wakes up from the low power sleep mode, the charge pump needs a start-up time (T_{WAKE}, up to 1mS) before the H-bridge output enable.

If the sleep mode is not been uses, connects the SLEPN pin to logic VDD (3~5V) with a 10KΩ pull-up resistor.

BLANKING TIME

An internal blanking time (T_{BLANK}, 4µs) blanks the output of the current sense comparator when the H-bridge outputs are switched, which is also the minimum on time for high-side MOSFET. The current spike is often seen during the switching transition period due to the body diode's reverse-recovery time or the parasitic capacitance and inductance. The blanking time can prevent the irrelevant current spike causes H-bridge shutdown.

OVER CURRENT PROTECTION (OCP)

Overcurrent detection circuit will always monitor all of output pins current during H-bridge is enabled, If any output pin is connected to VIN, GND or across load shorted, the inrush current will be detected by OCP circuit and immediately turns off the H-bridge outputs after OCP deglitch time (T_{OCDG}, 3.7µs) and the FALTN pin will be pull-down to low state. After the OCP retry period (T_{OCP}, up to 1.6ms) the driver will re-enable, and the FALTN pin will be reset to high state. If the OC fault condition is still exists, the OCP action will repeats again. The device will go back to normal operation and the FALTN resets to high state when fault condition be removed.

Over current conditions are detected independently on both high-side FETs and low-side FETs; for examples: a short to ground, a short to power supply, or across the motor winding will all result in an over current protect shutdown. Over current protection does not use the current sense circuitry used for PWM current regulation control, so it functions even without presence of the ASEN and BSEN resistors.

THERMAL SHUTDOWN (TSD)

If the chip temperature exceeds preset 170℃, the H-bridge will be turn off and the FALTN pin will be pull down to low state, an external pull up resistor may needed to detects FALTN logic state by MCU I/O pin. Once the chip temperature is reducing to below hysteresis window (140℃), H-bridge outputs will be enabled again.

UNDERVOLTAGE LOCKOUT (UVLO)

If the VIN pin voltage drops below the under voltage lockout threshold, the H-bridge outputs will be disabled and internal logic state will be reset. Operation will resume when VIN voltage rises above the UVLO threshold.

FAULT INDICATE OUTPUT (FALTN)

This pin will be pulls down to low state during such condition happens: includes over-temperature shutdown (TSD) and over current protection (OCP). The FALTN is an open-drain output, to obtain the logic high state, connects a 10KΩ pull-up resistor to the logic supply voltage is necessary.

POWER SUPPLY AND LAYOUT GUIDE

The inductance between the power supply and the motor drive system limits the rate current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied. The datasheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor. The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

The VIN pin should be bypassed to GND using low-ESR ceramic bypass capacitors with a recommended value of 10µF rated for VIN. This capacitor should be placed as close to the VIN pin as possible with a thick trace or ground plane connection to the device GND pin. The VDD pin needs a 2.2µF ceramic bypassing capacitor. Place this bypass capacitor as close to the pin as possible.

The printed circuit board (PCB) should use a heavy ground-plane. The PT5139 must be soldered directly onto the board for better electrical and thermal performance. The sense resistors should be placed as close as possible to the part for accurate current detection. The PT5139 uses an exposed pad, which provides a path for enhanced thermal dissipation. The thermal pad should be soldered directly to copper on the PCB. Thermal vias are often used to transfer heat to other layers of the PCB.

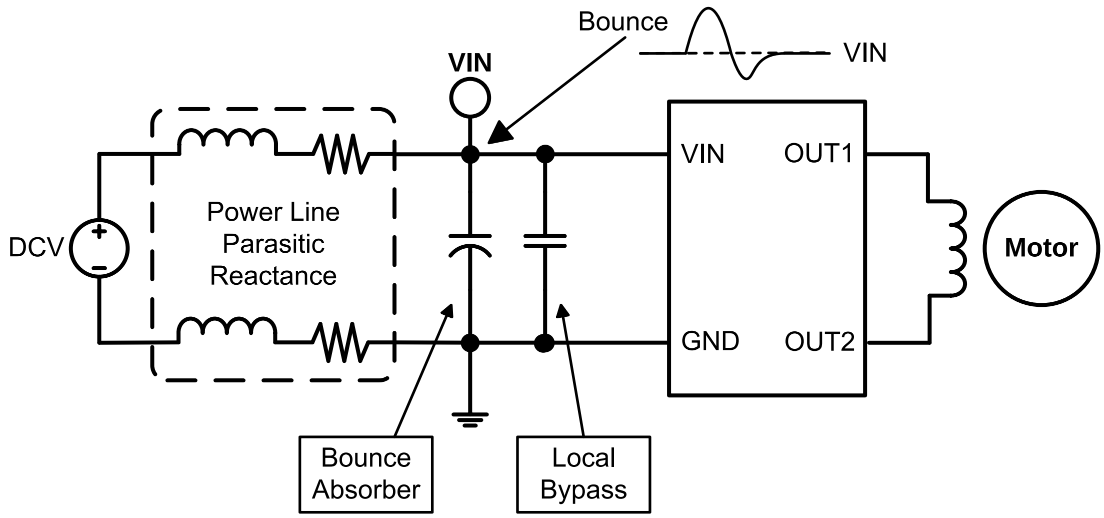
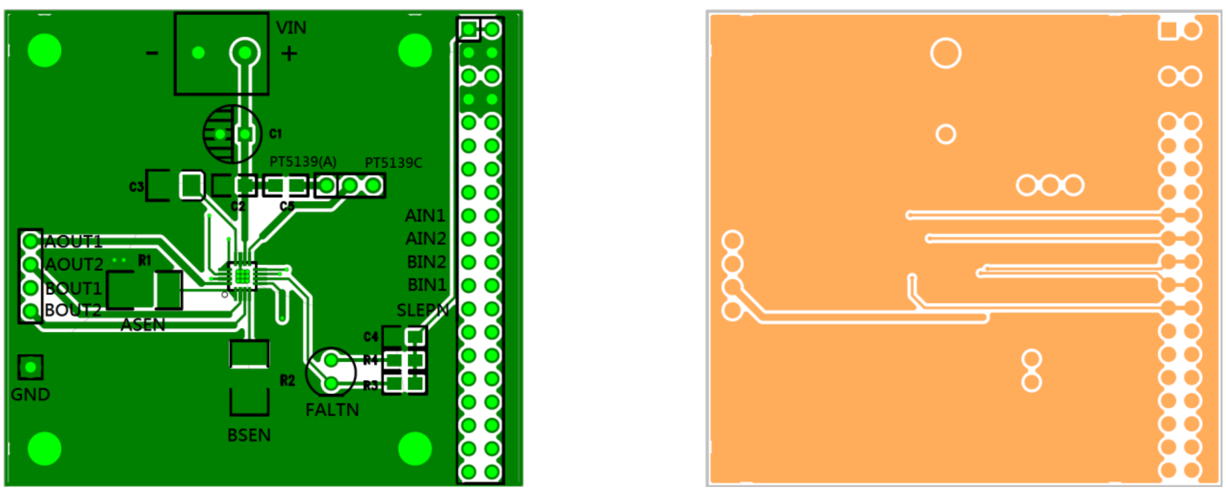
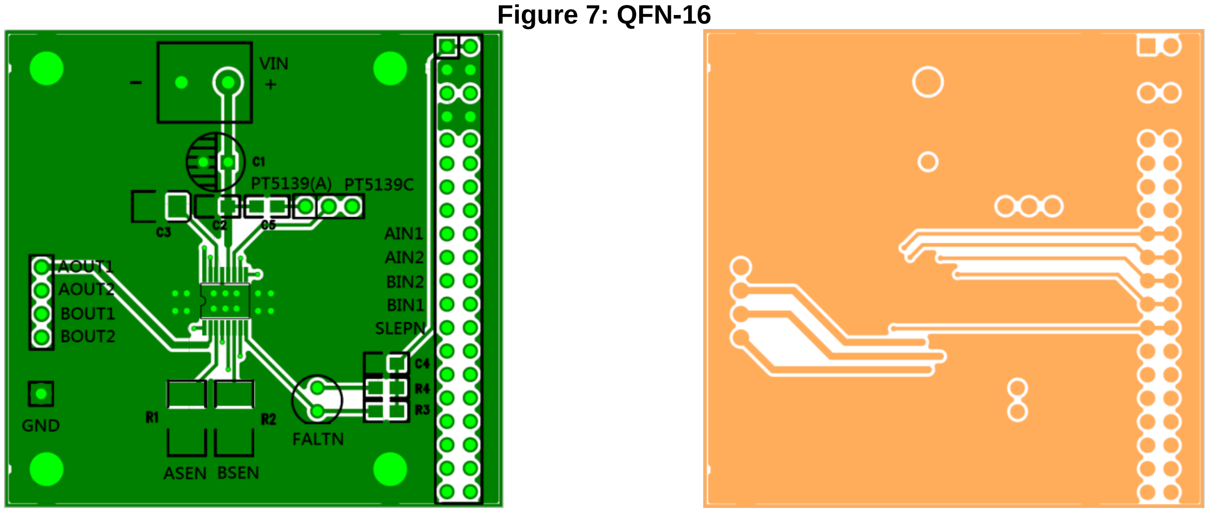


Figure 8 : Example Setup of Motor Drive System with External Power Supply



Top Side **Bottom Side**

Figure 7: QFN-16



Top Side **Bottom Side**

Figure 8: TSSOP-16

DESIGN EXAMPLES

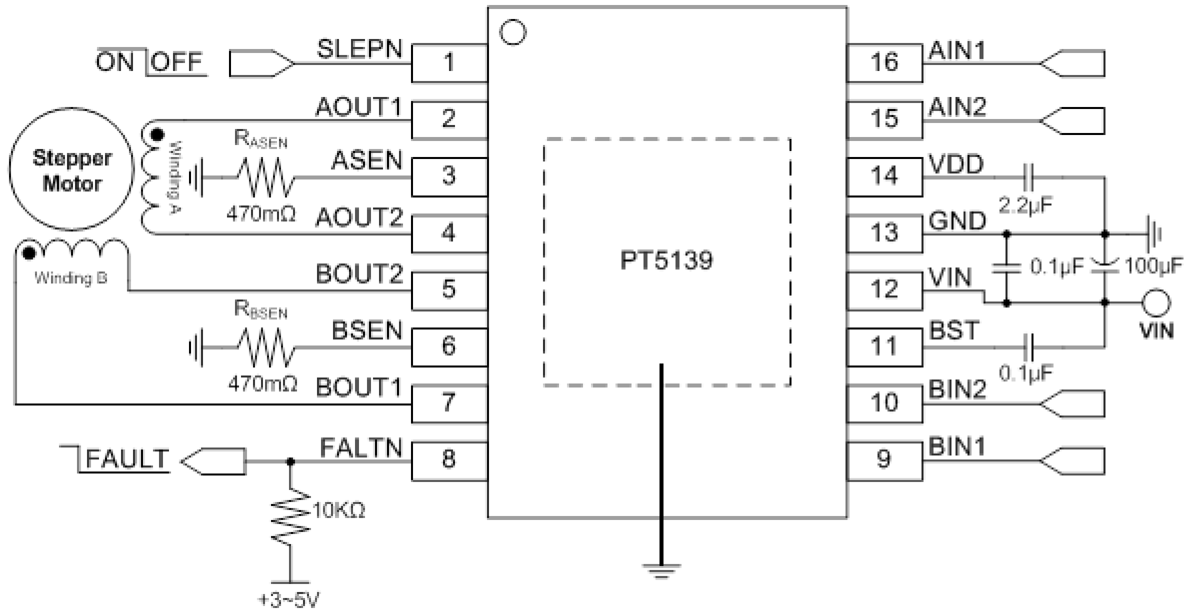


Figure 9: Drives a bipolar stepping motor with internal PWM current regulation

The output current will regulated at 400mA, V_{IN}=2.7~15V.

ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Rating	Unit
Power Supply Voltage	V_{IN}	-0.3 ~ +18	V
AOUTx Voltage	V_{AOUTx}	-0.3 ~ +V_{IN}+1V	V
BOUTx Voltage	V_{BOUTx}	-0.3 ~ +V_{IN}+1V	V
BST Voltage	V_{BST}	-0.3 ~ +V_{IN}+7V	V
Sense Voltage	Vx_{SEN}	-0.3 ~ +0.5	V
All Other Pins	-	-0.3 ~ +6.5	V
Lead Temperature	T_L	260	℃
Operating Junction Temperature	T_J	-40 ~ +150	℃
Storage Temperature	T_{STG}	-40 ~ +150	℃

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Rating			Unit
		Min.	Typ.	Max.	
Supply Voltage	V_{IN}	2.7	-	15	V
Output Current	$I_{A/BOUT}$	-	700	-	mA
Logic Input Level	V_{LI}	0		5.5	V
Operating Junction Temperature	T_{OPR}	-40	-	85	℃
External PWM Signal Frequency	f_{PWM}	0		200	KHz

THERMAL RESISTANCE

Parameter	θ_{JA}	θ_{JC}	Unit
QFN 16 (4mm × 4mm)	46	10	℃/W
HTSSOP 16 (5.0mm ×6.4mm)	45	10	℃/W
TSSOP 16 (5.0mm ×6.4mm)	103	38	℃/W

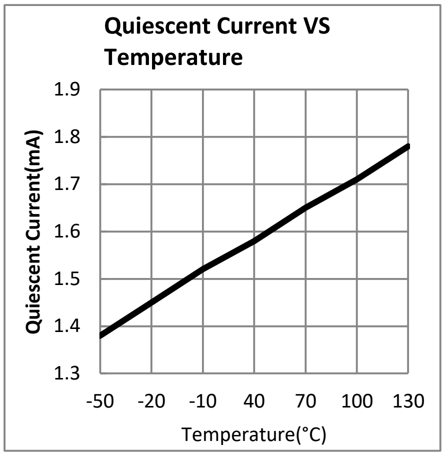
Note: Measure on JESD51-7, 4-layer PCB

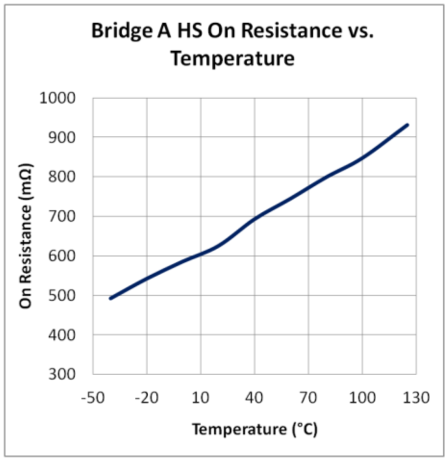
ELECTRICAL CHARATERISTICS

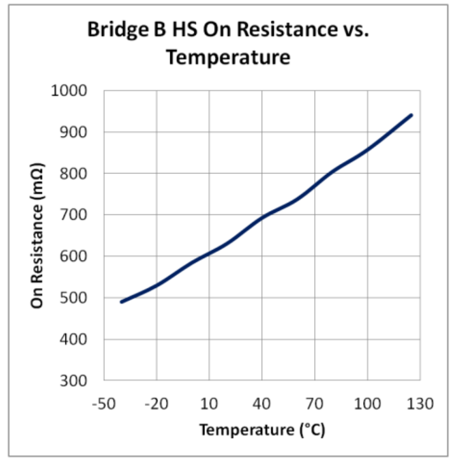
Nominal conditions: V_{IN}=5V, Ta=+25℃

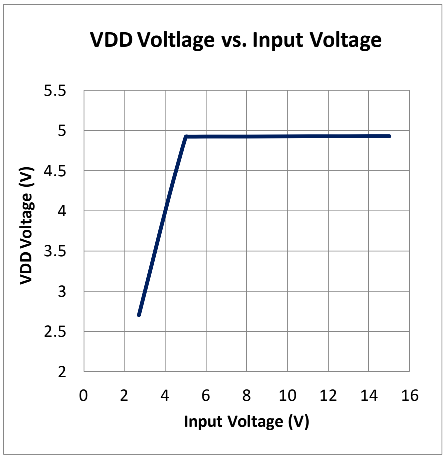
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power Supply						
Input supply voltage	V_{IN}	-	2.7		15	V
UVLO threshold (rising)	V_{IN_RISE}	-		2.2	2.4	V
UVLO hysteresis	V_{HYS}	-		100		mV
Quiescent current	I_{IN}	SLEPN=H, IN1=IN2=L	-	1.5	-	mA
	I_{IN_SLEEP}	SLEPN=L, V_{IN}=5V	-	-	1	μA
H-Bridge MOSFETs						
Body-diode forward voltage	V_F	I_{OUT}=500mA		1	1.3	V
MOSFETs on resistance	R_{HS}	I_{OUT}=500mA,V_{IN}=5V,T_J=25°C		560		mΩ
	R_{LS}	I_{OUT}=500mA,V_{IN}=5V,T_J=25°C		500		mΩ
Off-state output leakage current	I_{OFF}	SLEPN=L			1	μA
PWM current regulation Sense trip voltage	V_{TRIP}	ASEN and BSEN	-	185	-	mV
Control Logic						
Input logic low voltage	V_{IL}	-			0.6	V
Input logic high voltage	V_{IH}	-	2		-	V
SLEPN logic low voltage	V_{SLEEP_L}	-	-		0.4	V
SLEPN logic high voltage	V_{SLEEP_H}	-	2			V
Input pulldown resistance	R_{PD}	SLEPN		330		KΩ
		Logic input pins		200		KΩ
Fault output logic, Low	V_{FAULT_L}	Flag triggered by TSD 1mA sink current			200	mV
FALTN output leakage current	I_{LEAK_FAULT}	Normal operation, V_{FALTN}=5V			1	μA
Internal PWM fixed off time	T_{OFF}	-		25		μs
Propagation delay time (On)	T_{ON_DELAY}	INx high to Outx ON 10mA source current	1.1	1.6	2	μs
Propagation delay time (Off)	T_{OFF_DELAY}	INx low to Outx off	1.1	1.6	2	μs
Cross over delay	T_{CROSS}		200	400	950	ns
Blanking time	T_{BLANK}	Internal PWM current sense		4		μs
Sleep wake-up time	T_{WAKE}	SLEPN high to outputs on		1	1.5	ms
Protection Circuitry						
OCP deglitch time	T_{OCDG}		3.3	3.7	4.1	μs
Over current protection trip level	I_{OCP}		-	1.7	-	A
Over current protection period	T_{OCP}	-	-	1.6	-	ms
Thermal shutdown	TSD	-	-	170	-	°C
Thermal shutdown hysteresis	-	-	-	30	-	°C

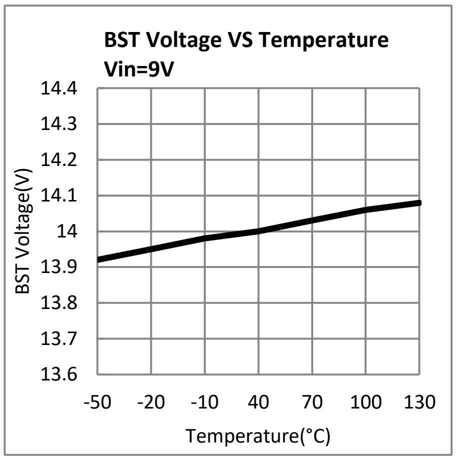
TYPICAL CHARACTERISTICS

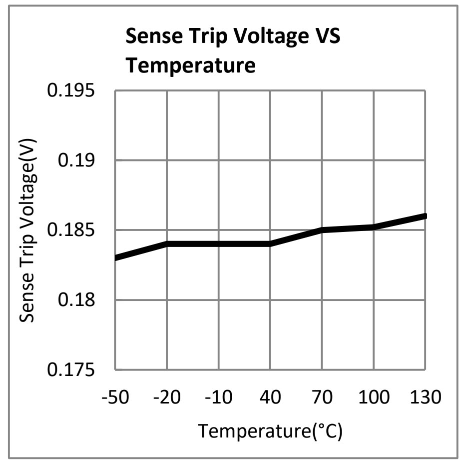


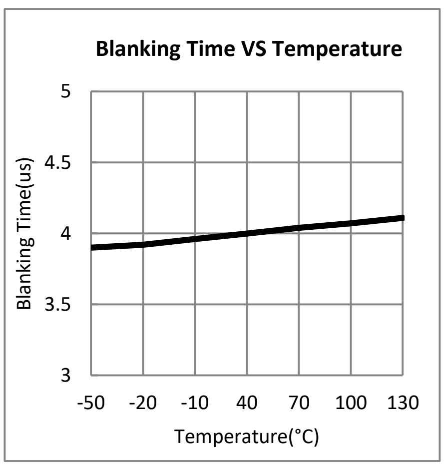








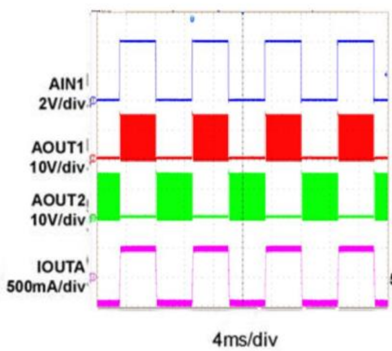




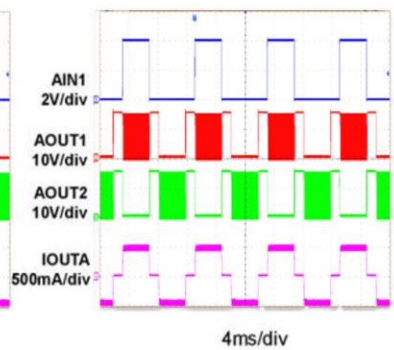
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board of the Design Example section.
IOUT=500mA, FSTEP=100Hz, Stepper Motor: L=2mH, R=10Ω, TA=25°C, unless otherwise noted.

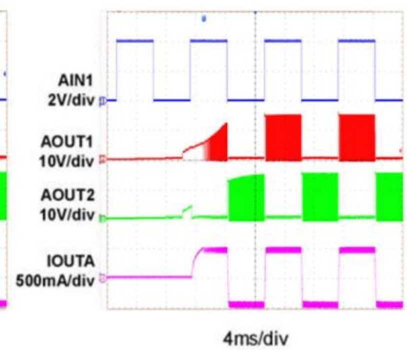
Steady State-Full Step
V_{IN}=15V



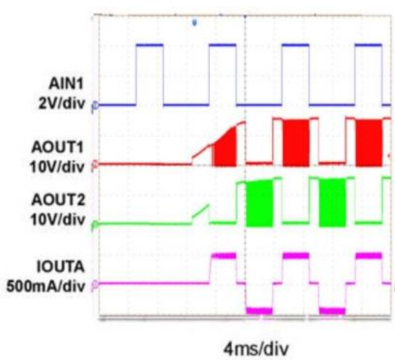
Steady State-Half Step
V_{IN}=15V



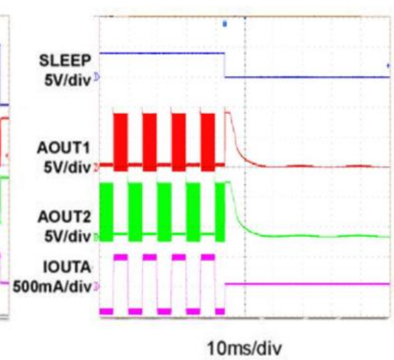
Power Ramp Up-full Step
V_{IN}=15V



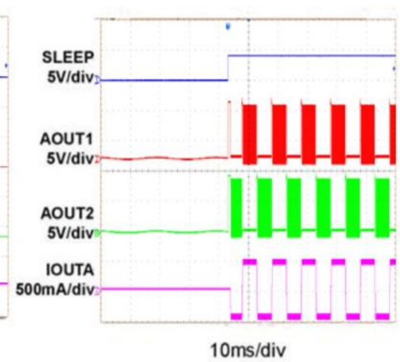
Power Ramp Up-Half Step
V_{IN}=15V



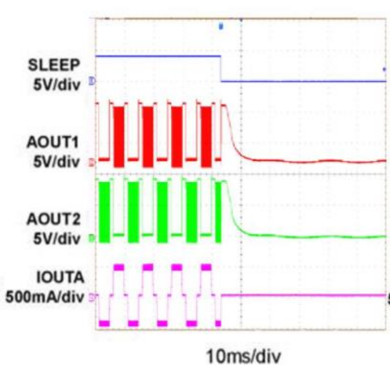
Sleep Entry-Full Step
V_{IN}=9V



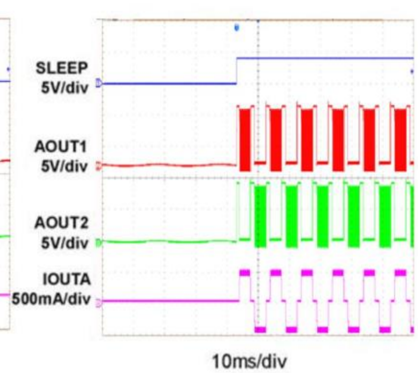
Sleep Recovery-Full Step
V_{IN}=9V



Sleep Entry-Half Step
V_{IN}=9V

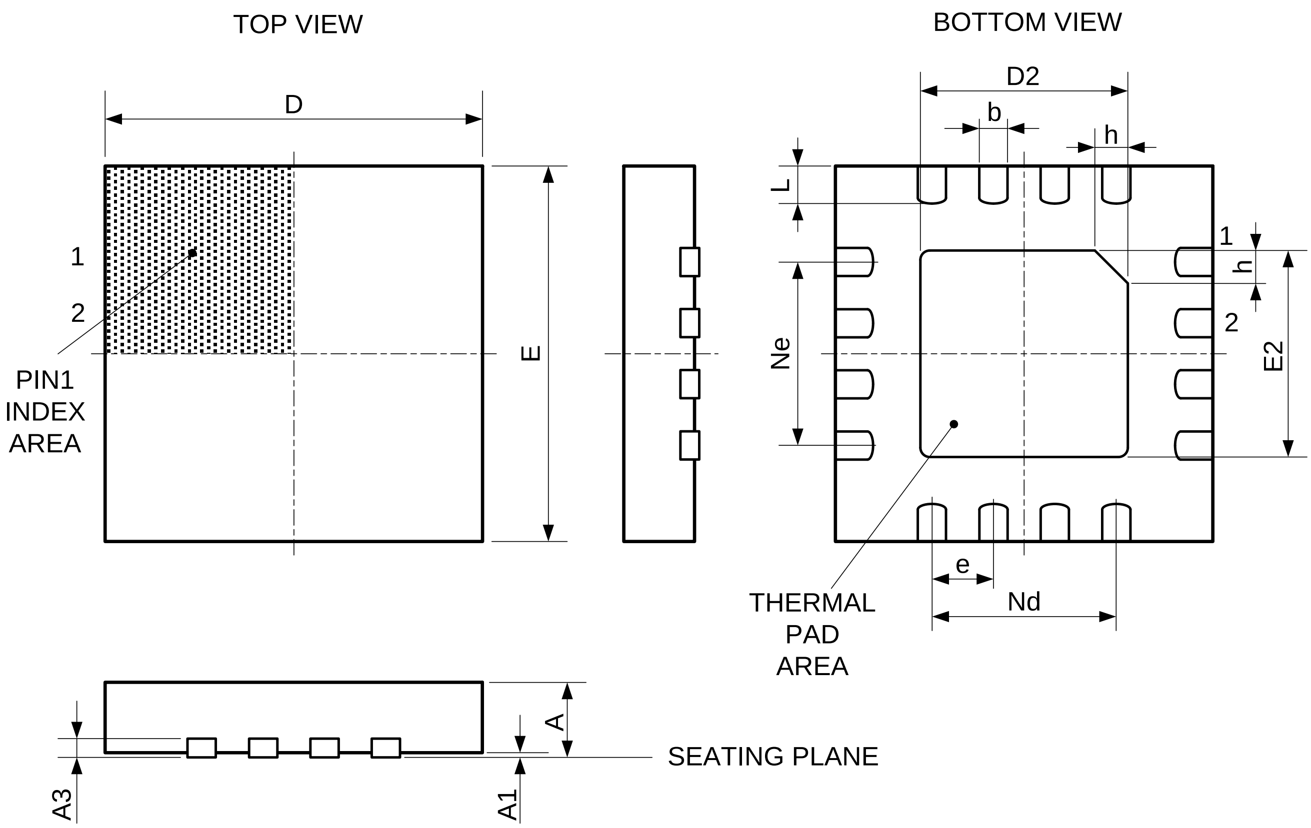


Sleep Recovery-Half Step
V_{IN}=9V



PACKAGE INFORMATION

16 Pins, QFN, BODY SIZE = 4.0mm × 4.0mm

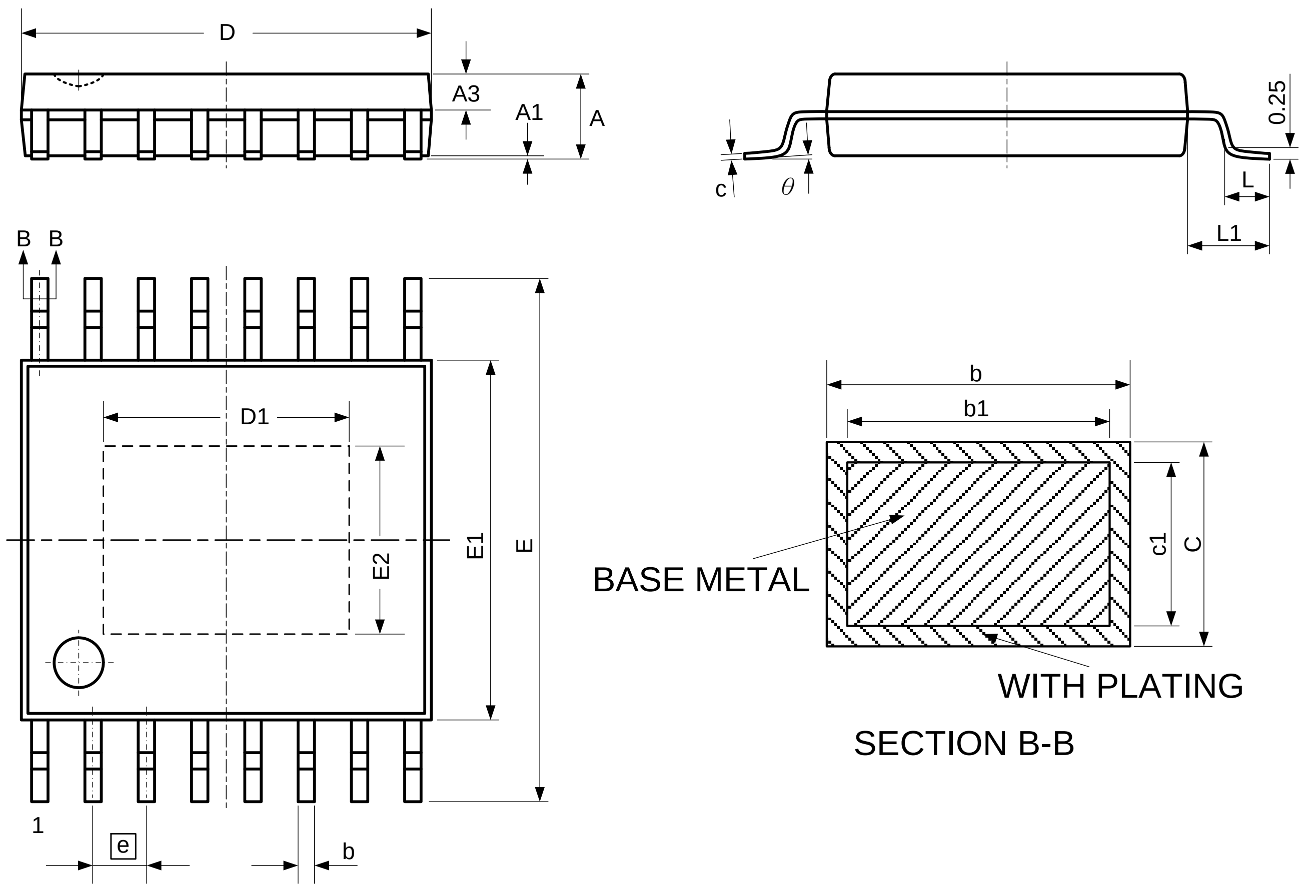


Symbol	QFN, 4mm × 4mm Dimensions		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3	0.20 REF		
b	0.25	0.3	0.35
D	4.0 BSC		
E	4.0 BSC		
D2	2.1	2.2	2.3
E2	2.1	2.2	2.3
e	0.65 BSC		
Nd	1.95 BSC		
Ne	1.95 BSC		
h	0.30	0.35	0.40
L	0.35	0.40	0.45

Notes:

1. Refer to JEDEC MO-220 WGGC
2. Unit: mm

16 Pins, HTSSOP, BODY SIZE = 5.0mm × 6.4mm

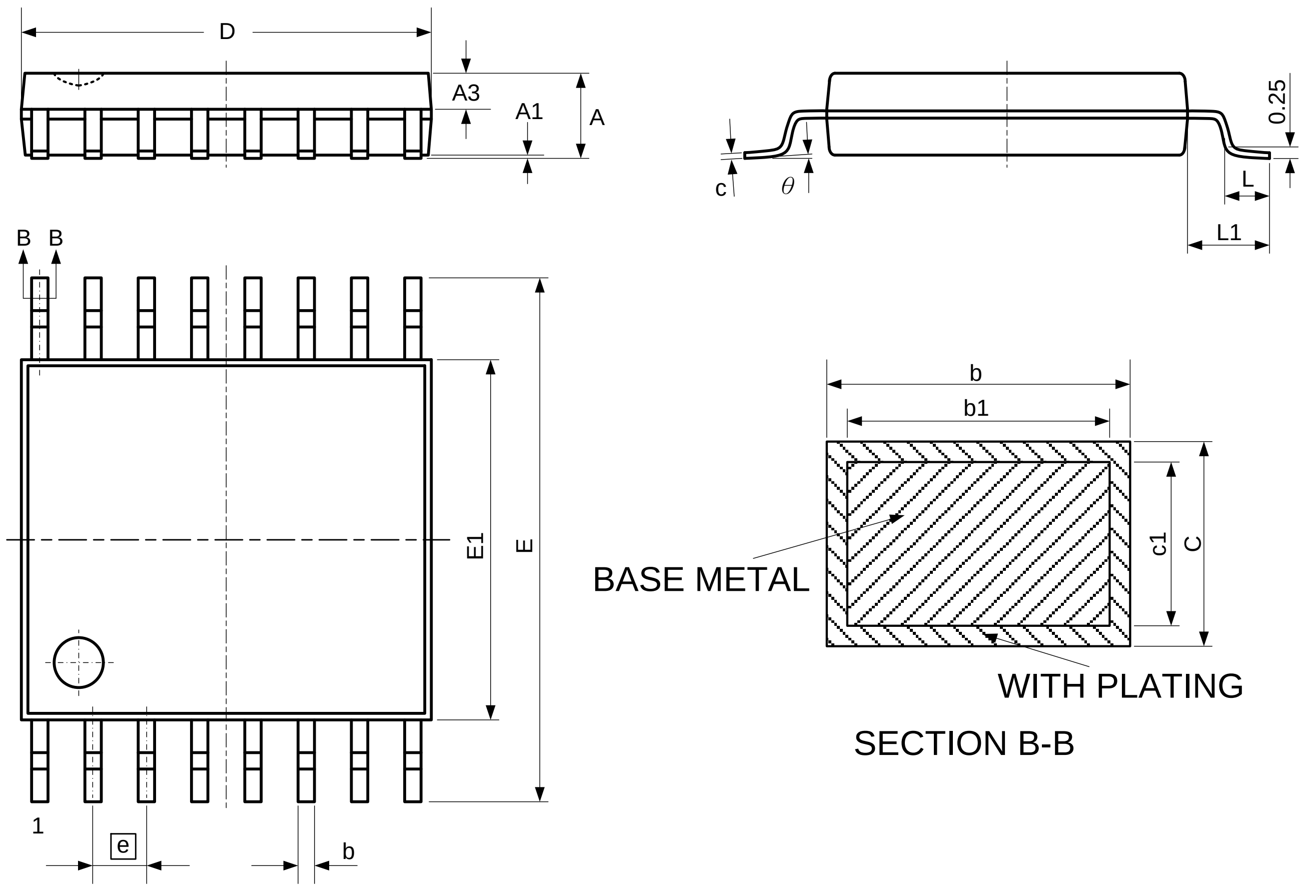


Symbol	Dimensions		
	Min.	Nom.	Max.
A	-	-	1.20
A1	0.05	-	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.19	-	0.30
b1	0.19	0.22	0.25
e	0.65 BSC		
c	0.13	-	0.19
c1	0.12	0.13	0.14
D	4.86	5.0	5.1
D1	2.90	3.00	3.10
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
E2	2.2	2.3	2.4
L	0.45	-	0.75
L1	1.00 BSC		
θ	0	-	8°

Notes:

1. Refer to JEDEC MO-153 ABT.
2. Unit: mm

16 Pins, TSSOP, BODY SIZE = 5.0mm × 6.4mm



Symbol	Dimensions		
	Min.	Nom.	Max.
A	-	-	1.20
A1	0.00	-	0.15
A2	0.90	1.00	1.05
A3	0.39	0.44	0.49
b	0.19	-	0.30
b1	0.19	0.22	0.25
e	0.65 BSC		
c	0.13	-	0.19
c1	0.12	0.13	0.14
D	4.86	5.0	5.1
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
L	0.45	-	0.75
L1	1.00 BSC		
θ	0	-	8°

Notes:

3. Refer to JEDEC MO-153 AB.
4. Unit: mm

IMPORTANT NOTICE

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