DESCRIPTION

The PT5639 is a high-speed power MOSFET driver with three independent high and low side referenced output channels for 3-phase gate driver. Built-in deadtime protection and Shoot-through protection that prevent half-bridge against damage. The UVLO circuits prevent malfunction when VCC and VBS are lower than the specified threshold voltage. Novel high-voltage BCD process and common-mode noise canceling technique provide stable operation of high-side drivers under high-dv/dt noise circumstances and excellent negative transient voltage tolerance. PT5639 also includes a 3.3V/5V 50mA LDO, which saving the BOM cost.

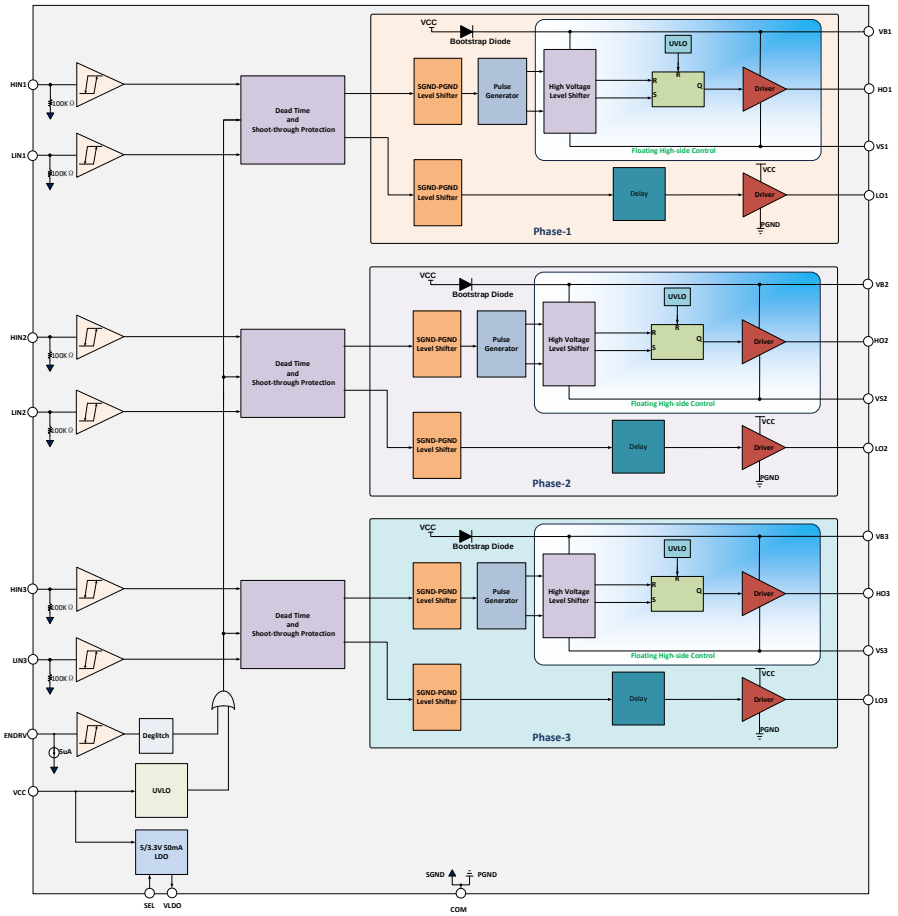
APPLICATION

- 3-phase Motor Driver for E-BIKE, electric power tool
- Mini/micro motor control powered by battery
- General purpose inverter

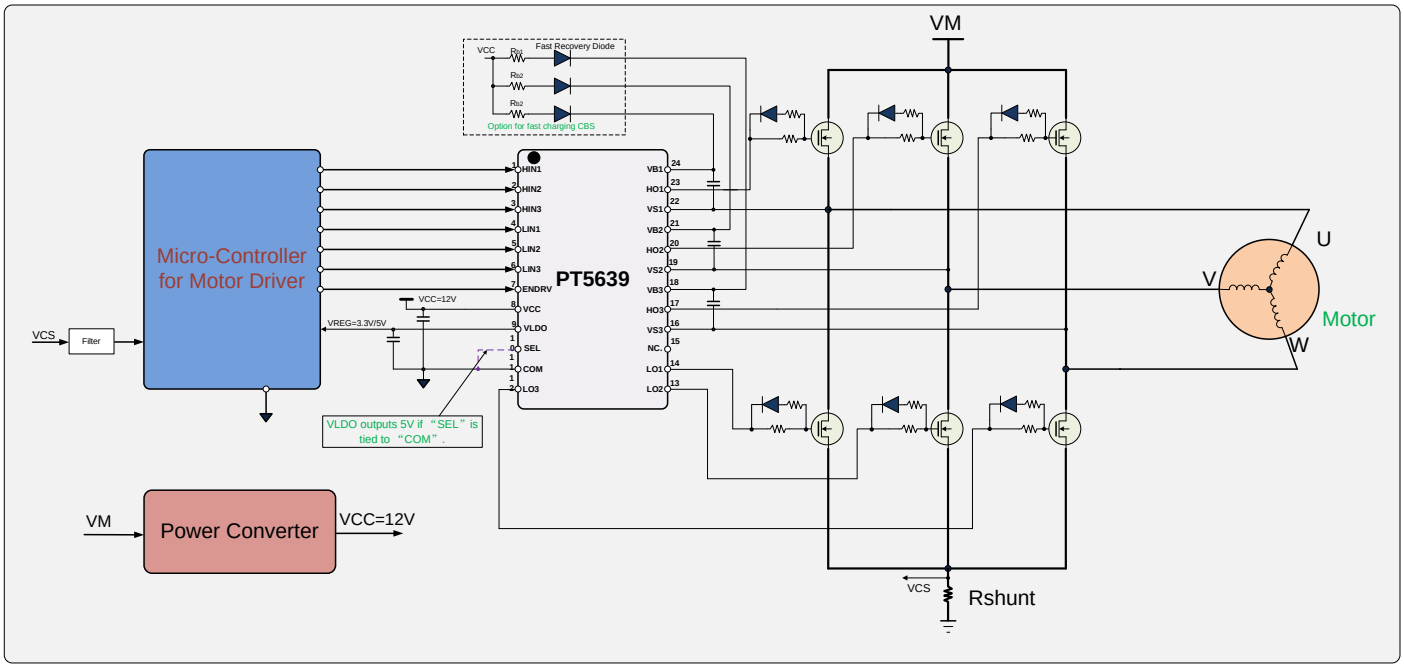
FEATURES

- Integrated 90V half-bridge high side driver
- Driver up to 3-phase half-bridge gates
- Built-in bootstrap diode for each high side channel
- Low standby power dissipation: I_{QVCC}<50uA
- Shoot-through protection
- Under voltage lockout for VCC and VBS
- Low operation voltage 0~5.5V for VCC and VBS
- 3.3V, 5V input logic Compatible
- IO+/IO-: +0.5A/-0.8A@VCC=12V, VBS=12V
- Built-in dead time：0.2us(typ.)
- Built-in 3.3V/5V 50mA LDO
- Common-Mode dv/dt Noise Canceling Circuit
- Tolerant to negative transient voltage
- Low di/dt gate drive for better noised immunity
- -40℃ to 125℃ operating range
- Small footprint package：TSSOP20L/24L,173mil; 4mm*4mm, QFN

BLOCK DIAGRAM



TYPICAL APPLICATION CIRCUIT

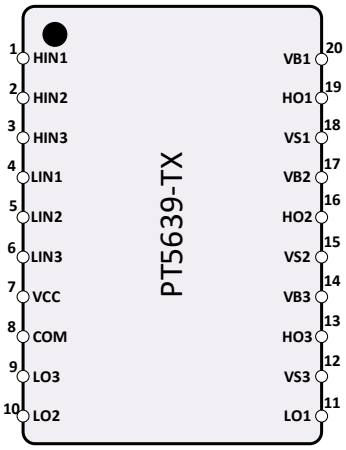


ORDERING INFORMATION

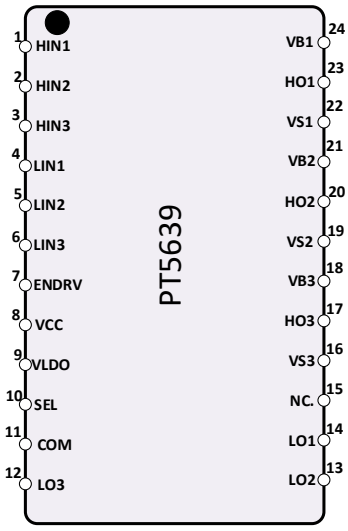
Valid Part Number	Package Type	Top Code
PT5639-TX	20 Pins, TSSOP, 173mil	PT5639-TX
PT5639	24 Pins, TSSOP, 173mil	PT5639
PT5639	24 Pins, QFN, 4mmx4mm	PT5639

PIN CONFIGURATION

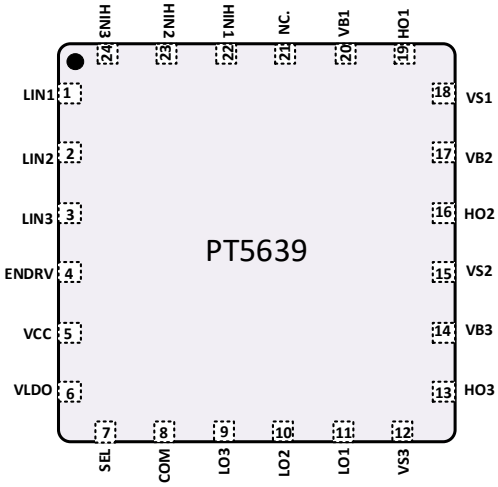
TSSOP20L AND TSSOP24L PACKAGE



TSSOP20L



TSSOP24L



QFN4X4_24L

PIN DESCRIPTION

Pin Name	Description	Pin No.		
		TSSOP20L	TSSOP24L	QFN4X4_24L
HIN1	Logic input for phase-1 high-side gate driver	1	1	22
HIN2	Logic input for phase-2 high-side gate driver	2	2	23
HIN3	Logic input for phase-3 high-side gate driver	3	3	24
LIN1	Logic input for phase-1 low-side gate driver	4	4	1
LIN2	Logic input for phase-2 low-side gate driver	5	5	2
LIN3	Logic input for phase-3 low-side gate driver	6	6	3
ENDRV	Logic input for standby mode control	-	7	4
VCC	Logic and low-side gate drivers power supply voltage	7	8	5
VLDO	3.3/5V LDO output	-	9	6
SEL	LDO's output-voltage selection	-	10	7
COM	Logic ground and low-side gate drivers' ground	8	11	8
LO3	phase-3 Low-side gate driver output	9	12	9
LO2	phase-2 Low-side gate driver output	10	13	10
LO1	phase-1 Low-side gate driver output	11	14	11
NC.	Not Connected	-	15	21
VS3	phase-3 High-side driver floating supply offset voltage	12	16	12
HO3	phase-3 High-side driver output	13	17	13
VB3	phase-3 High-side driver floating supply	14	18	14
VS2	phase-2 High-side driver floating supply offset voltage	15	19	15
HO2	phase-2 High-side driver output	16	20	16
VB2	phase-2 High-side driver floating supply	17	21	17
VS1	phase-1 High-side driver floating supply offset voltage	18	22	18
HO1	phase-1High-side driver output	19	23	19
VB1	phase-1High-side driver floating supply	20	24	20

FUNCTION DESCRIPTION

LOW SIDE POWER SUPPLY: VCC AND LDO

VCC is the low side supply and it provides power to both input logic and low side output power stage. The built-in under-voltage lockout circuit enables the device to operate at sufficient power when a typical VCC supply voltage higher than V_{CCUV+} =4.2V is present, shown as FIG1. The IC shuts down all the gate driver outputs, when the VCC supply voltage is below V_{CCUV-} =3.8 V, shown as FIG1. This prevents the external power devices against extremely low gate voltage levels during on-state and therefore against excessive power dissipation.

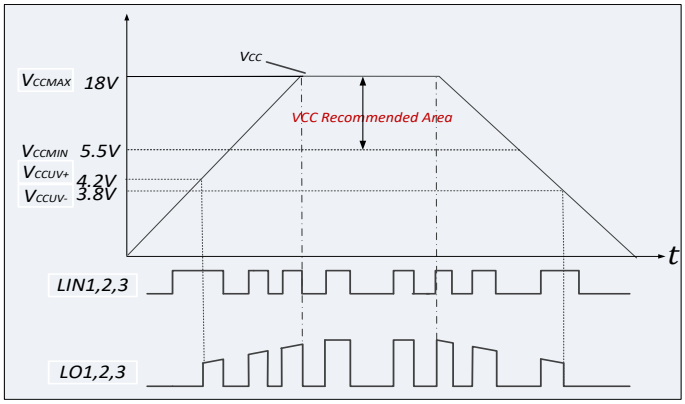


FIG.1 VCC supply UVLO operating area

A low voltage-dropout regulator (LDO) is integrated into this IC and powered by VCC. This LDO can supply the controller with a capability of 50mA. The PIN “SEL” can set the LDO’s output (PIN “VLDO”) voltage. When “SEL” floats, the PIN “VLDO” outputs a default 3.3V. If “SEL” is pulled down to COM, VLDO voltage is programmed to 5V.

HIGH SIDE POWER SUPPLY: VBS (VB1-VS1, VB2-VS2, VB3-VS3)

VBS is the high side supply voltage. The totally high side circuitry can float with respect to COM following the external high side power device emitter/source voltage. Due to the internally low power consumption, the whole high side circuitry can be supplied by bootstrap topology connected to VCC, and it can be powered with small bootstrap capacitors.
The device operating area as a function of the supply voltage is given in Figure2. In order to power the bootstrap capacitors, a built-in bootstrap diode connects VCC and VBS of each high side circuitry, which shown as the BLOCK DIAGRAM above.

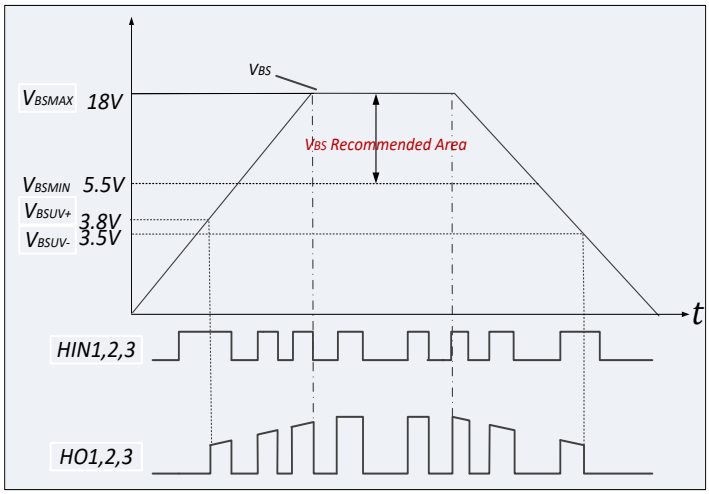


FIG.2 VBS supply UVLO operating area

LOW SIDE AND HIGH CONTROL INPUT LOGIC: HIN&LIN (HIN1,2,3/LIN1,2,3)

The Schmitt trigger threshold of each input is designed enough low such to guarantee LSTTL and CMOS compatibility down to 3.3 V controller outputs. An internal pull-down resistor of about 100kΩ (positive logic) pre-biases each input during VCC supply start-up state. It is anyway recommended for proper work of the driver not to provide input pulse-width lower than 300ns.

SHOOT-THROUGH PREVENTION

The IC is equipped with shoot-through prevention circuitry (also known as cross conduction prevention circuitry). Figure 3 shows how this prevention circuitry prevents both the high- and low-side power switches from conducting at the same time. During the inputs controlling high side driver and low side driver are both “high”, the both driver outputs are pulled down “low” to shut down two power devices in the same bridge. If one input is changed to “low”, the power switch corresponding to the “high” input turns on after a deadtime (DT).

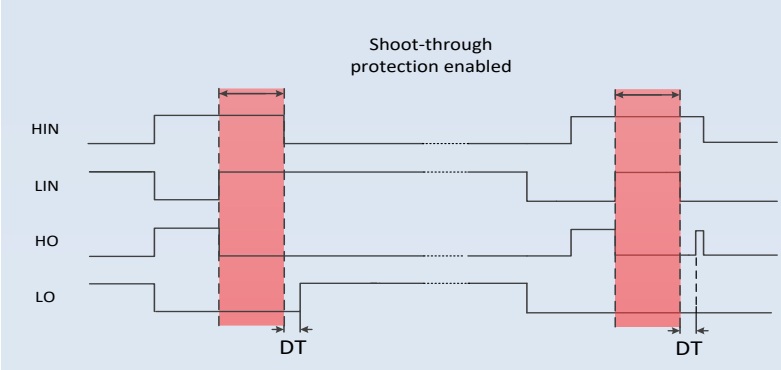


FIG.3 Shoot-through prevention

DEAD TIME

The IC features integrated a fixed dead-time protection circuitry. The dead time feature inserts a time (a minimum dead time) in which both the high- and low-side power switches are held off; this is done to ensure that the power switch has fully turned off before the second power switch is turned on. This minimum dead time is automatically inserted whenever the external dead time is shorter than DT; external dead times larger than DT are not modified by the gate driver. Figure 4 illustrates the dead-time period and the relationship between the output gate signals.

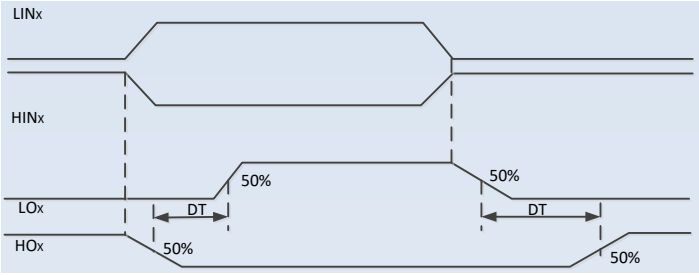


FIG.4 Dead Time

GATE DRIVER (HO1,2,3/ LO1,2,3)

Low side and high side driver outputs are specifically designed for pulse operation and dedicated to drive the power switches such as IGBT and MOSFET. Low side outputs (i.e. LO1,2,3) are state triggered by the respective inputs, while high side outputs (i.e. HO1,2,3) are only changed at the edge of the respective inputs. In practically, after releasing from an under-voltage condition of the VBS supply, a new turn-on signal (edge) is necessary to activate the respective high side output, while after releasing from a under voltage condition of the VCC supply, the low side outputs can directly switch to the state of their respective inputs and don’t suffer from the trouble as high side driver.

STANDBY MODE

This device packed in TSSOP24L provides a featured pin, ENDRV, to enable that it can work into low current dissipation state. ENDRV is compatible with 5V/3.3V logic level. If ENDRV is pulled down to “low” level, this device is forced into standby mode. when all gate driver output is locked into “low” level and a < 50uA current is dissipated by VCC. If ENDRV goes up to “high” level, and waits a deglitch time about 2us (typ.), this device can be released from standby mode, and all outputs are enabled. In order to lowering the bias current, a 5ua current pulls down this PIN. When this PIN keeps “low” or floating, the IC enters standby mode after powering up. If standby mode is needed, all PWM inputs going to “low” are recommended.

ABSOLUTE MAXIMUM RATINGS

Stresses exceeding the absolute maximum ratings may damage the device or make the function abnormal. All the voltage parameters are absolute voltages referenced to IC COM unless otherwise stated in the table.

Parameter	Symbol	Min.	Max.	Units
High-side floating supply voltage	$V_{B1,2,3}$	-0.3	105	V
High-side offset voltage	$V_{S1,2,3}$	$V_{B1,2,3}$-20	$V_{B1,2,3}$+0.3	
High-side gate driver output voltage	$V_{HO1,2,3}$	$V_{S1,2,3}$-0.3	$V_{B1,2,3}$+0.3	
Low-side gate driver output voltage	$V_{LO1,2,3}$	COM-0.3	V_{CC}+0.3	
Logic input voltage	$V_{HIN1,2,3}$ $V_{LIN1,2,3}$ ENDRV	-0.3	7	
Low-side supply voltage	V_{CC}	-0.3	20	
Package power dissipation @ TA≤25°C ①	P_D	—	TSSOP20:1.2 TSSOP24:1.3 QFN4X4_24: 2.8	W
Thermal resistance，junction to ambient ①	Rth_{JA}	—	TSSOP20:100 TSSOP24:94 QFN4X4_24: 42	°C /W
Allowable Offset Voltage Slew Rate	dV/dt	—	50	V/ns
Junction temperature	T_J	-40	+150	°C
Storage temperature	T_S	-40	+150	
Soldering lead temperature (duration 10s)	TL	—	260	°C

Operation outside the Absolute Maximum Ratings may cause permanent device damage. These ratings are stress limits only, and functional operation of the device at these or any other conditions beyond those specified under Recommended Operating Conditions is not guaranteed. Operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings may impair device functionality, reliability, or longevity.

Note:
①: P_D and Rth_{JA} are only guaranteed by design.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Units
Low-side supply voltage	V_{CC}	5.5	—	15	V
High-side Floating Supply Offset Voltage②	$V_{S1,2,3}$	COM-6	—	90	
High-side Floating Supply Voltage	$V_{B1,2,3}$	$V_{S1,2,3}$+5.5	—	$V_{S1,2,3}$+15	
High-side gate driver output voltage	$V_{HO1,2,3}$	V_S	—	V_B	
Low-side gate driver output voltage	$V_{LO1,2,3}$	COM	—	V_{CC}	
Logic input voltage	$V_{HIN1,2,3}$ $V_{LIN1,2,3}$ ENDRV	0	—	5	
3.3V/5V LDO output current	I_{VLDO}	-	-	50	mA
IC operating Junction temperature	T_J	-40	—	+125	°C

Functional operation is guaranteed only within the Recommended Operating Conditions. Operation outside this range may result in degraded performance, reduced reliability, or shortened lifetime of the device.

②: For V_{BS}=12V, normal Logic operation for V_S of COM–6V to 90V. High-side circuitry will sustain current state if VS is of COM-6 to COM-V_{BS}. The parameter is only guaranteed by design.

STATIC ELECTRICAL CHARACTERISTICS

（V_{CC}-COM）=(V_B-V_S)=12V. Ambient temperature T_A=25℃ unless otherwise specified. The $V_{IN,TH}$, V_I, and I_{IN} Parameters are reference to COM and are applicable to all channels. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads. The V_{CCUV} parameters are referenced to COM. The V_{BSUV} parameters are referenced to V_S.

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Low Side Power Supply Characteristics						
Quiescent VCC supply current	I_{QVCC1}	$V_{HIN1,2,3}$ =$V_{LIN1,2,3}$=0 or 5V, V_{ENDRV}=5	100	177	280	μA
Quiescent VCC supply current in standby mode	I_{QVCC2}	$V_{HIN1,2,3}$ =$V_{LIN1,2,3}$=0 or 5V, $V_{S1,2,3}$ floats, LDO normally output	—	36	50	
VCC supply under-voltage positive going threshold	V_{CCUV+}	—	2.9	4.2	5.5	V
VCC supply under-voltage negative going threshold	V_{CCUV-}	—	2.5	3.8	5.1	
VCC supply under-voltage lockout hysteresis	V_{CCHYS}	—	—	0.4	—	
LDO Characteristics						
LDO output voltage	V_{LDO}	VCC=12V, Iload=25mA “SEL” floats	3.135	3.3	3.465	V
		VCC=12V, Iload=25mA SEL tied to COM	4.75	5	5.25	
LDO output voltage-dropout	V_{drop}	VCC=5.5V, Iload=30mA “SEL” floats	—	0.5	—	
High Side Floating Power Supply Characteristics						
High side VBS supply under-voltage positive going threshold	V_{BSUV+}	—	2.6	3.8	5	V
High side VBS supply under-voltage negative going threshold	V_{BSUV-}	—	2.3	3.5	4.7	
High side VBS supply under-voltage lockout hysteresis	$V_{BSUVHYS}$	—	—	0.3	—	
High side quiescent VBS supply current	I_{QBS}	V_{BS}=12V	5	10	15	μA
Offset supply leakage current	I_{LK}	V_B=V_S=100V V_{CC}=0V	—	—	10	
Bootstrap diode internal resistance	RBS	-	-	100	-	Ω
Logic Input Section						
Logic”1” Input voltage HIN1,2,3, LIN1,2,3 and ENDRV	V_{IH}	—	2.2	—	—	V
Logic”0” Input voltage HIN1,2,3, LIN1,2,3 and ENDRV	V_{IL}	—	—	—	0.8	
Input positive going threshold	$V_{IN,TH+}$	—	—	1.7	—	
Input negative going threshold	$V_{IN,TH-}$	—	—	1.3	—	
Logic “1” Input bias current	I_{IN+}	V_{IN}=5V	—	50	70	uA
Logic “0” Input bias current	I_{IN-}	V_{IN}=0	-1	0	1	
ENDRV pull-down current	I_{endrv}	V_{ENDRV}=5	—	5	10	
Gate Driver Output Section						
High Side Output High Short-Circuit Pulse Current	I_{HO+}	V_{HO}=V_S=0	—	0.5	—	A
High Side Output Low Short-Circuit Pulse Current	I_{HO-}	V_{HO}=V_B=12V	—	0.8	—	
Low Side Output High Short-Circuit Pulse Current	I_{LO+}	V_{LO}=0	—	0.5	—	
Low Side Output Low Short-Circuit Pulse Current	I_{LO-}	V_{LO}=V_{CC}=12V	—	0.8	—	

Allowable Negative VS Voltage for HIN1,2,3 Signal Propagation to HO1,2,3	V_{SN}	V_{BS}=12V	—	-6	-	V

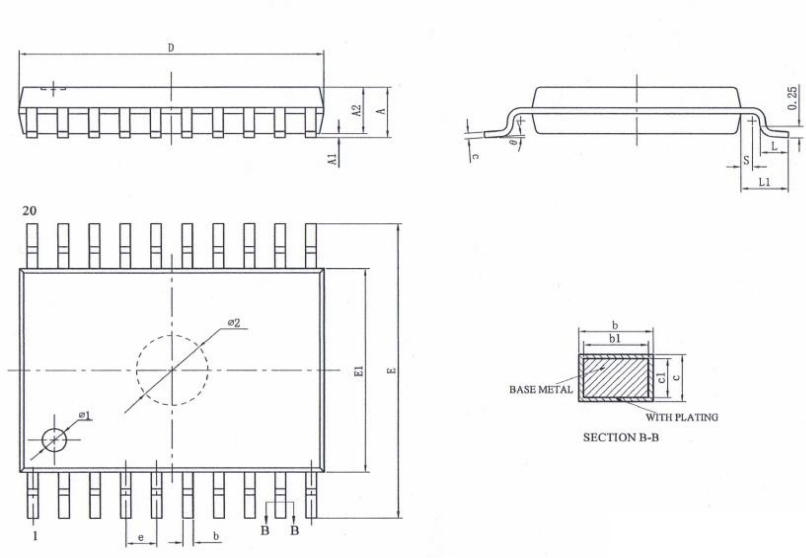
DYNAMIC ELECTRICAL CHARACTERISTICS

（VCC-COM）=(VB-VS)=12V ,$V_{S1,2,3}$=COM, and C_{load}=2.2nF unless otherwise specified, ambient temperature T_A=25℃.

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Operating VCC supply current	I_{VCCOP}	$f_{LIN1,2,3}$=20KHz, $f_{HIN1,2,3}$=20KHz, no Cload, VSx=0	—	1200	—	uA
Turn-On propagation delay	t_{on}	$V_{HIN1,2,3}$ or $V_{LIN1,2,3}$=5V, $V_{S1,2,3}$=0	—	100	200	ns
Turn-Off Propagation delay	t_{off}	$V_{HIN1,2,3}$ or $V_{LIN1,2,3}$=0, $V_{S1,2,3}$=90V	—	100	200	
Turn-On Rise time	t_r	$V_{HIN1,2,3}$ or $V_{LIN1,2,3}$=5V, $V_{S1,2,3}$=0	—	70	—	
Turn-Off Fall time	t_f	$V_{HIN1,2,3}$ or $V_{LIN1,2,3}$=0, $V_{S1,2,3}$=0	—	40	—	
Dead Time	DT	$V_{HIN1,2,3}$ or $V_{LIN1,2,3}$=0 &5V, Without External dead time	120	200	280	
Dead-Time Matching(All Six Channels)	MDT	Without External dead time	—	—	50	
Delay Matching(All Six Channels)	MT	External dead time >1000ns	—	—	50	
Output Pulse-Width Matching	PM	External dead time > 1000ns, PW_{IN}=10us,PM=PW_{OUT}-PW_{IN}	—	—	50	
ENDRV input deglitch time	t_{dglt}	-	—	2	—	us

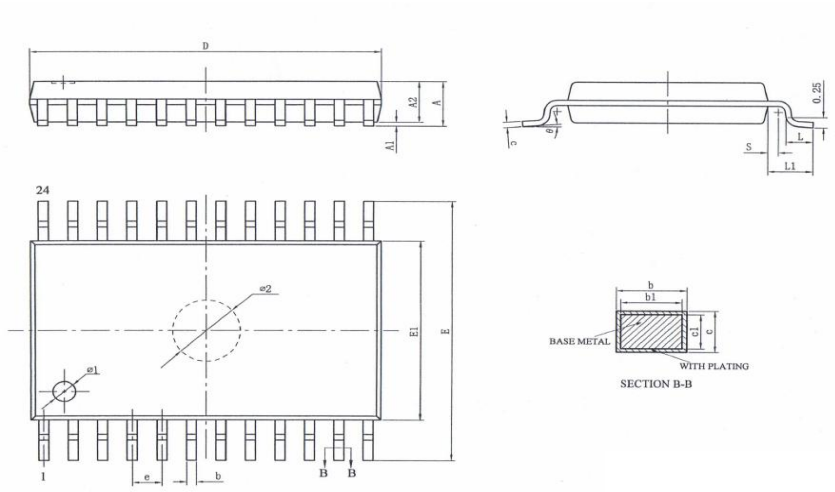
PACKAGE INFORMATION

20 PINS, TSSOP, 173MIL



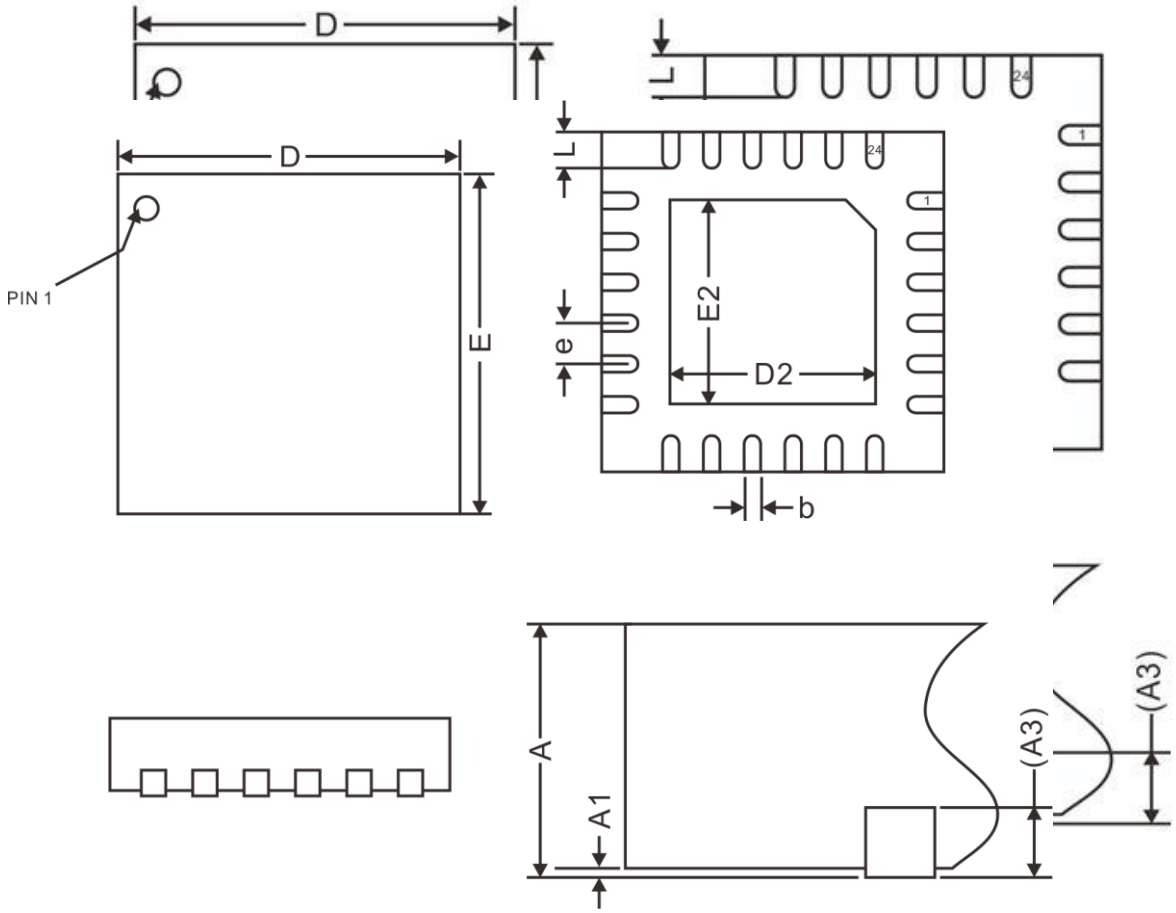
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0. 80	1. 00	1. 05
b	0.19	—	0.30
b1	0.19	0.22	0.25
c	0.09	—	0.20
c1	0.09	—	0.16
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65BSC		
L	0. 45	0. 60	0. 75
L1	1.00BSC		
S	0.20	—	—
Ø1	Ø0.8X0. 05~0. 10DP		
Ø2	Ø1.50X0.05~0.15DP		
θ	0	—	8°
L/F載体尺寸 (mil)	118*165 (C)		

24 PINS, TSSOP, 173MIL



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.05	—	0.15
A2	0. 80	1. 00	1. 05
b	0.19	—	0.30
b1	0.19	0.22	0.25
c	0.09	—	0.20
c1	0.09	—	0.16
D	7.70	7.80	7.90
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e	0.65BSC		
L	0. 45	0. 60	0. 75
L1	1.00BSC		
S	0.20	—	—
Ø1	Ø0.8X0. 05~0. 10DP		
Ø2	Ø1.50X0.05~0.15DP		
θ	0	—	8°
L/F載体尺寸 (mil)	118*165 (C)	122*190 (C)	

QFN, 24 PINS



Symbol	Dimensions		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF.	
b	0.18	0.25	0.30
D		4.00BSC	
E		4.00BSC	
D2	2.50	2.65	2.80
E2	2.50	2.65	2.80
e		0.50 BSC	
L	0.35	0.40	0.45

Notes:
1. All dimensions refer to JEDEC MO-220 VGGD-6
2. All dimensions are in millimeter.

IMPORTANT NOTICE

Princeton Technology Corporation (PTC) reserves the right to make corrections, modifications, enhancements, improvements, and other changes to its products and to discontinue any product without notice at any time.
PTC cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a PTC product. No circuit patent licenses are implied.

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